Ultra Fast Fixed-Frequency Hysteretic Buck Converter With Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications

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***Abstract*—An integrated DC–DC hysteretic buck converter with ultrafast adaptive output transient response for reference tracking is presented. To achieve the fastest up-tracking speed, the maximum charging current control is introduced to charge up the output voltage with the maximum designed current. For down-tracking, the output is discharged by the load only to save energy. Although the converter works with hysteretic voltage mode control, an adaptive delay compensation scheme is employed to keep the switching frequency constant at 850 kHz to within $\pm 2.5\%$ across the whole operation range. The integrated buck converter was fabricated using a 0.35 μm CMOS process. With an input voltage of 3 V, the output voltage can be regulated between 0.5 and 2.5 V. With a load resistor of 10 Ω, the up-tracking speed of the maximum reference step (0.5 to 2.5 V) is 12.5 $\mu s/V$. All design features are verified by extensive measurements.**

***Index Terms*—Adaptive delay compensation, adaptive output, current sensor, dynamic voltage scheduling (DVS), maximum charging current control, pseudocontinuous conduction mode (PCCM), rail-to-rail comparator, reference tracking.**

I. Introduction

DYNAMIC voltage and frequency scheduling (DVFS) is one of the effective solutions for reducing the power consumption of digital systems [1]–[3]. Depending on the workload of the task and the slack available from the system, the clock frequency of executing a task and the corresponding supply voltage are varied during run-time in order to optimize the dynamic and leakage power consumption while still satisfying the deadline requirement. A critical component for implementing DVFS is the adaptive power converter that could provide variable supply voltage with fast tracking speed. It is usually implemented by a switching converter due to its high efficiency [4]–[8]. A switching converter with variable output voltage for DVFS applications should have the following characteristics.

1) It should attain system stability across the whole operation range.
2) It should have a fast tracking speed to minimize latency and losses when switching between different voltage levels. This provides higher flexibility for the system to optimize the voltage scheduling. Tracking time of the order of 10 μs or shorter are preferred, which are much faster than most of the state-of-the-art designs.
3) Reverse current from the output capacitor back to the input supply or ground should be avoided to reduce power loss.
4) It is advisable to maintain a constant switching frequency so that electromagnetic interference (EMI) noise spectrum is known and conform to common practice in the industry.

In this paper, an integrated DC–DC buck (step-down) converter that has the above characteristics for DVFS applications is presented. In Section II, a simple and effective reference tracking scheme, denoted as maximum charging current (MCC, or MC^2) control, is proposed. Here, the output voltage of the converter up-tracks the reference voltage using the maximum allowable current within the safe limit of the chip. For down-tracking, to reduce the power loss, the inductor stops to supply power to the output capacitor and the output capacitor is discharged by the load current only. Section III presents the system architecture of the converter that operates in hysteretic voltage-mode control to ensure stability. Section IV discusses the detailed circuit implementation that includes two integrated on-chip current sensors and the adaptive delay compensation (ADC) circuitry. The ADC includes a frequency-error detector and a voltage-controlled delay unit to keep the switching frequency at 850 kHz to within $\pm 2.5\%$ across the whole operation range. Section V presents and discusses experimental results, and Section VI summarizes our research efforts with some concluding remarks.

II. MCC Control

A switching converter implementing DVFS requires fast reference tracking. For up-tracking, the output voltage $V_{\rm o}$ is changed from a lower voltage $V_{\rm o1}$ to a higher voltage $V_{\rm o2}$ with a scheduled change in the reference voltage $V_{\rm ref}$. To achieve a fast reference tracking speed, a large current is needed to charge or discharge the output capacitor $C_{\rm o}$. To alleviate the metal electromigration effect, there is a current density limit for the on-chip metal rails, which is usually of the order of 1 mA/μm [9]. At the same time, the metal rails cannot be exceedingly wide in order to keep the cost down. Thus, there is a maximum current $I_{\rm max}$ that the design can handle. Hence, the fastest way to charge up $C_{\rm o}$ from $V_{\rm o1}$ to $V_{\rm o2}$ is to keep the charging current at $I_{\rm max}$ all the time. The up-tracking time $T_{\uparrow \rm min,}$ is thus equal

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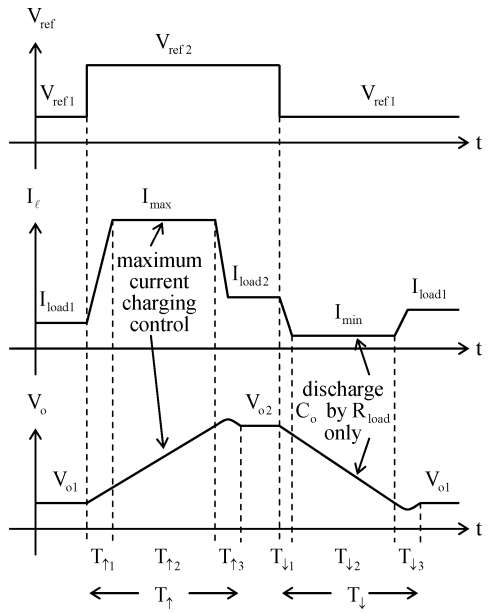

Fig. 1. Fast reference tracking strategy.

to $C_{\rm o}(V_{\rm o2}-V_{\rm o1})/I_{\rm max}$. $T_{\uparrow \rm min}$ is the theoretical minimum and is not attainable in practice, because: 1) the inductor current I_ℓ has to ramp up from a lower steady-state value and cannot become $I_{\rm max}$ instantaneously and 2) $I_{\rm max}$ has to supply the load current $I_{\rm load}$ also, reducing the effective charging current for $C_{\rm o}$.

Here, we propose a fast reference-tracking scheme. The up-tracking process can be divided into the following three phases as shown in Fig. 1.

1) Inductor current ramp up phase ($T_{\uparrow 1}$): During $T_{\uparrow 1}$, the inductor current ramps up from the output (load) current $I_{\rm load1}$ to the maximum allowable current $I_{\rm max}$ with full duty cycle. $T_{\uparrow 1}$ can be calculated as

$$T_{\uparrow 1}=\frac{L(I_{\rm max}-I_{\rm load1})}{(V_{\rm dd}-V_{\rm o1})}. \tag{1}$$

Note that the controller should be able to produce full duty ratio if $T_{\uparrow 1}$ is larger than the switching period.

2) Maximum current charging phase ($T_{\uparrow 2}$): During $T_{\uparrow 2}$, the inductor current switches between two predefined levels $I_{\rm P\,max}$ and $I_{\rm N\,min}$ (the details will be discussed in Section III) such that the average inductor current is kept at $I_{\rm max}=(I_{\rm P\,max}+I_{\rm N\,min})/2$. The maximum current is charging the output capacitor at full speed until the capacitor voltage reaches the predefined value $V_{\rm o2}$. $T_{\uparrow 2}$ is then given by

$$T_{\uparrow 2}=\frac{C_{\rm o}(V_{\rm o2}-V_{\rm o1})}{I_{\rm max}}. \tag{2}$$

3) Inductor current ramp down phase ($T_{\uparrow 3}$): When the output voltage reaches the predefined value, the inductor current is then decreased to the new output current $I_{\rm load2}$. The load transient time $T_{\uparrow 3}$ depends on the control methodology of the converter. The total up-tracking time is

$$T_{\uparrow}=T_{\uparrow 1}+T_{\uparrow 2}+T_{\uparrow 3}. \tag{3}$$

For down-tracking, if the system allows reversion current flow from the output capacitor back to the input voltage source or to ground, a similar control strategy as the up-tracking case can be applied, where the maximum charging current is replaced by the maximum discharging current (and the inductor current is negative). However, to reduce the DVFS overhead and to achieve more energy saving, reversion current should be avoided. In this case, the output is discharged by the load current only during this period, and the down-tracking speed is then dominated by $T_{\downarrow 2}$ that could be quite long under light load conditions. A long $T_{\downarrow 2}$ is not important for DVFS applications as a higher power supply voltage supports a higher switching frequency, and the task is guaranteed to be completed before deadline.

From the above discussion, it is clear that in order to obtain a tracking time close to the theoretical minimum the converter should have the following capabilities:

- The converter should be able to apply full or zero duty cycles to increase or decrease the inductor current to minimize $T_{\uparrow 1}$ and $T_{\downarrow 1}$.
- The converter should have fast response, even for a large current change, to minimize $T_{\uparrow 3}$ and $T_{\downarrow 3}$.
- The converter should have a current limiting circuit to prevent the charging current from going beyond $I_{\rm max}$ of the system and a reversion control circuit to prevent reversion current from flowing back to the input source.

III. System Architecture

Hysteretic voltage-mode control, also known as band-band control or ripple voltage control, is well known for its fast response for line and load transients. Moreover, hysteretic switching converters have been shown to have unconditional stability under all operation conditions [10], [11]. We discuss stability from the operation of the converter here rather than using state plane analysis. We use Fig. 2 for the illustration. Without loss of generality, continuous conduction mode (CCM) is assumed. If the output voltage $V_{\rm o}$ is lower than the low-voltage limit $V_{\rm oL}$, the hysteretic comparator turns on the pMOS power switch $\rm M_P$, charging up the output capacitor $C_{\rm o}$ through the inductor L, and the output voltage $V_{\rm o}$ increases. The voltage across the inductor is $V_\ell=V_{\rm dd}-V_{\rm o}>0$. Eventually, $V_{\rm o}$ will be higher than the preset high-voltage limit $V_{\rm oH}$. Due to delay in the loop, the gate drive $V_{\rm g}$ switches from $V_{\rm gnd}$ (0 V) to $V_{\rm dd}$ after $t_{\rm dly2}$ as shown in Fig. 2(b), turning off $\rm M_P$, turning on the nMOS power switch $\rm M_N$, and allowing the inductor current I_ℓ to flow from ground to charge up $C_{\rm o}$. The inductor voltage is then $V_\ell=-V_{\rm o}<0$ and I_ℓ ramps down. When I_ℓ ramps below the average inductor current, $V_{\rm o}$ decreases and eventually the load current $I_{\rm load}$ drains the output capacitor $C_{\rm o}$ until $V_{\rm o}$ drops below the low-voltage limit $V_{\rm oL}$ again. If a change in the input voltage or the output current causes $V_{\rm o}$ to be outside the band limited by $V_{\rm oL}$ and $V_{\rm oH}$, the hysteretic comparator will issue gate drive signals to charge or discharge $C_{\rm o}$ continuously (that is, full or zero duty cycle) to steer $V_{\rm o}$ back to within the band as quickly as possible. Thus, the output voltage is corrected as fast as the output power filter (L and $C_{\rm o}$) allows and, incidentally, the converter is unconditionally stable. The propagation delays $t_{\rm dly1}$ and $t_{\rm dly2}$ shown in Fig. 2 depend on the delay of the

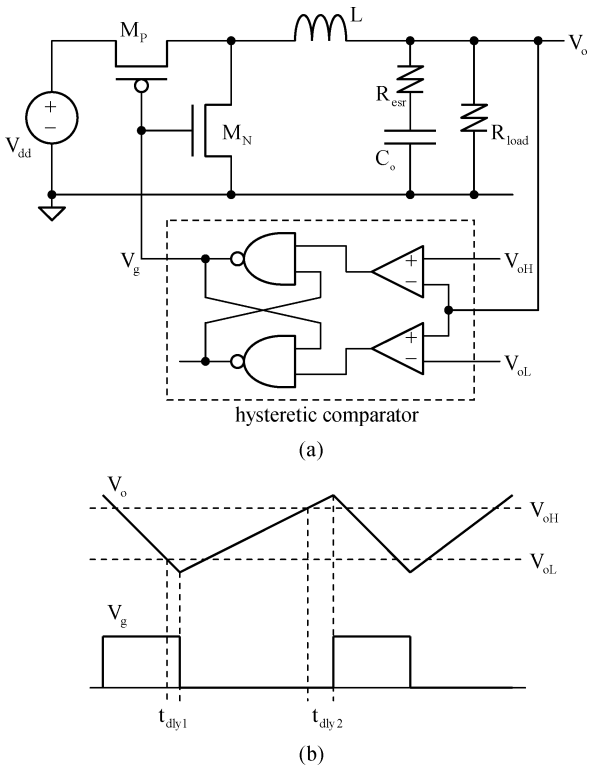

Fig. 2. Conventional hysteretic voltage-mode control of buck converter. (a) System architecture. (b) Waveforms of $V_{\rm o}$ and $V_{\rm g}$.

hysteretic comparator and the latch. In practice, any functional block in the loop, such as the nonoverlapping circuit or the gate drive buffers, would all contribute to the propagation delays.

The hysteretic converter has two main disadvantages. First, as the control loop allows full and zero duty cycles, the inductor current could rise beyond the current limit of the power switches during large signal transient responses, for example, during the start-up period. Second, the switching frequency $f_{\rm s}$ varies with all of the design parameters of the converter, such as $V_{\rm dd}$, $V_{\rm o}$, L, $C_{\rm o}$, etc. [12]. We use $V_{\rm oH}$ and $V_{\rm oL}$ as an example. If $V_{\rm oH}V_{\rm oL}$ is smaller, then $f_{\rm s}$ is higher. However, even when $V_{\rm oH} = V_{\rm oL}$, $f_{\rm s}$ is not infinitely high, because the control loop has delay. In this research, we use $V_{\rm oH} = V_{\rm oL}$ so that only one comparator is needed. At the same time, in order to achieve a fixed switching frequency, we propose an adaptive delay compensation scheme. The overall system architecture of the proposed converter, which implements both the maximum charging control and the hysteretic control, is shown in Fig. 3.

The proposed hysteretic buck converter uses only one reference voltage $V_{\rm ref}$ (instead of $V_{\rm oH}$ and $V_{\rm oL}$) to define the output voltage $V_{\rm o}$. An adaptive delay compensator (ADC) is used to regulate the switching frequency to a preset value. The ADC has two subblocks, a frequency-error detector (FED), and a voltage-controlled delay (VCD). The switching frequency is determined by the preset voltage $V_{\rm F}$. The FED detects the error between $V_{\rm F}$ and $V_{\rm cmp}$ and generates a control signal $V_{\rm ctrl}$ to drive the VCD to regulate the switching frequency. Synchronous rectification is implemented by the switches $\rm M_P$ and $\rm M_N$, and both the "switch" current of $\rm M_P$ and the "diode" current of $\rm M_N$ are monitored by on-chip current sensors [13], [14] to produce voltages $V_{\rm P}$ and $V_{\rm N}$ for the maximum charging current control. The converter is designed to operate in pseudocontinuous conduction mode (PCCM) in the steady state [15], [16]. The voltage $V_{\rm pccm}$ that corresponds to the current level $I_{\rm pccm}$ determines the valley inductor current, and, as shown in Fig. 4, if $I_{\rm pccm}$ is set to zero, the converter then works in discontinuous conduction mode (DCM). Whether the converter works in PCCM or DCM, the freewheel switches $\rm M_{FWp}$ and $\rm M_{FWn}$ are turned on when the sensed "diode" current reaches $I_{\rm pccm}$. In any case, $I_{\rm pccm}$ is set to be very low, such that both $\rm M_{FWp}$ and $\rm M_{FWn}$ are small switches. In fact, we may use only $\rm M_{FWp}$ or $\rm M_{FWn}$ to simplify the control.

As shown in Fig. 1, during the up-tracking period when $V_{\rm ref}$ is changed from $V_{\rm o1}$ to $V_{\rm o2}$, in-rush current is needed to charge up the output capacitor quickly, so that the output voltage could track the reference voltage as quickly as the system allows under safe conditions. Voltage levels $V_{\rm H}$ and V_L define the high and low limits of the inductor current during tracking transients, respectively. When $V_{\rm o}$ is lower than $V_{\rm o2}$, the power transistor $\rm M_P$ is turned on, and $V_{\rm dd}$ then charges up the inductor L, and the inductor current ramps up. $\rm M_P$ will be turned off when $I_\ell = I_{\rm P\,max}$, which is manifested as $V_{\rm P} = V_{\rm H}$. At the same time, $\rm M_N$ is turned on to discharge I_ℓ until the current of $\rm M_N$ is lower than $I_{\rm N\,min}$ (manifested as V_L) and then $\rm M_P$ will be turned on again. The swing of the inductor current is around 200 mA in this design. As $V_{\rm o}$ has not reached $V_{\rm o2}$ yet, the converter undergoes switching activities, turning on and off $\rm M_P$ and $\rm M_N$ alternately. As $I_{\rm P\,max}$ is higher than $I_{\rm load}$, $V_{\rm o}$ will eventually be charged up to $V_{\rm o2}$, and I_ℓ is then allowed to discharge all the way to $I_{\rm load}$ and steady state is reached again. Note that, for a switching converter, the inductor current cannot be a constant during switching, and the maximum charging current should be considered as $I_{\rm max} = (I_{\rm P\,max} + I_{\rm N\,min})/2$. Consequently, the converter achieves the fastest practical up-tracking speed subject to the limitation of the charging constraints discussed above. When the output voltage is changed from a higher $V_{\rm o2}$ to a lower $V_{\rm o1}$, we do not want to have reversion current to flow back to the input supply or to the ground, thus the fastest way is to use the load current to discharge $C_{\rm o}$, and $T_{\rm min\downarrow} = C_{\rm o}(V_{\rm o2} - V_{\rm o1})/I_{\rm load}$. Hence, when $V_{\rm ref}$ is changed from $V_{\rm o2}$ to $V_{\rm o1}$, both $\rm M_P$ and $\rm M_N$ are turned off until $V_{\rm o} = V_{\rm o1}$, and the steady state is reached.

For applications where the tracking speed is more important than power efficiency, the up-tracking response could be enhanced by adding a direct charging path (DCP), as shown in Fig. 3, to charge the output directly with the supply voltage through a switch. It is activated only when the inductor current I_ℓ has ramped up to the predefined maximum current level $I_{\rm P\,max}(V_{\rm p} > V_{\rm H})$ and $V_{\rm max}$ switches from "0" to "1." The maximum charging control mechanism remains operative and the output capacitor is charged up by both the inductor current and the supply voltage. When the output voltage rises above $V_{\rm ref}$, triggering $V_{\rm cmp}$ to switch from "0" to "1," the DCP switch is then turned off immediately. Similarly, a direct discharging path (DDP) could be added to sink current from the output to ground directly to improve the down-tracking response. Note that both the DCP and DDP switches are lossy, and they could be disabled if efficiency is a major concern. Unlike $\rm M_P$ or $\rm M_N$, these

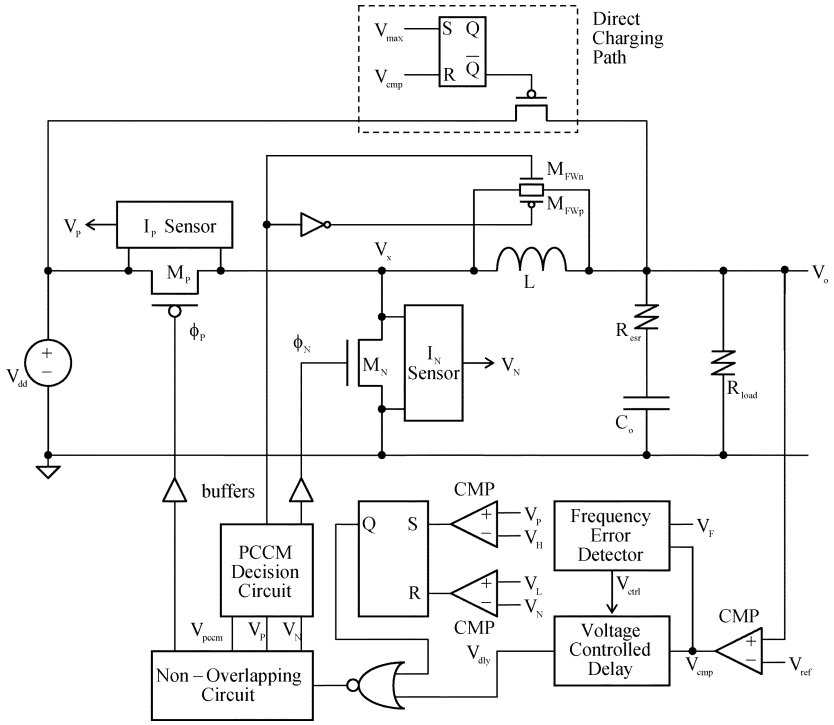

Fig. 3. System architecture of the proposed hysteretic buck converter.

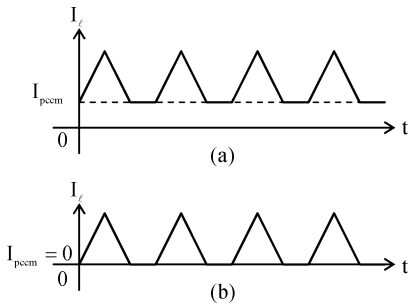

Fig. 4. Inductor current in (a) PCCM and (b) DCM.

switches could be very small, as their own resistance is designed to limit the charging current to within a safe limit.

As discussed above, the conventional hysteretic buck converter is unconditionally stable [10], [11]. However, our proposed design has an additional loop for compensating the loop delay and regulating the switching frequency to a constant. An immediate question is thus: Is the modified buck converter still unconditionally stable? Clearly, if the delay of the adaptive delay compensator is fixed (or the control signal $V_{\rm ctrl}$ is fixed), then our proposed converter resembles a regular hysteretic buck converter and is thus unconditionally stable. It implies that, if the bandwidth of the delay compensation loop is much slower than the voltage regulation loop, the stability of the buck converter will not be affected. Hence, we design the delay compensation loop such that its bandwidth is much smaller than that of the voltage regulator loop.

IV. Circuit Implementation of the Hysteretic Buck Converter

A. Integrated On-Chip Current Sensors

Fig. 5(a) and (b) shows the on-chip CMOS current sensors for $\mathrm{M_P}$ and $\mathrm{M_N}$, respectively. They are based on the matched current source technique proposed in [13]. More accurate current sensors such as those proposed in [14] can also be used. As the two current sensors operate in a similar fashion, we only use the current sensor of $\mathrm{M_N}$ as an example to illustrate the operation principle. The sensing nMOS $\mathrm{M_{Ns}}$ and the power nMOS $\mathrm{M_N}$ have the same gate, source, and bulk connections, and the W/L ratio of $\mathrm{M_{Ns}}$ to $\mathrm{M_N}$ is 1/1500. When $\phi_{\rm N} = V_{\rm dd}$, $\mathrm{M_N}$ and $\mathrm{M_{Ns}}$ are turned on. The transistors $\mathrm{M_1}$ to $\mathrm{M_4}$ form a differential common-gate amplifier with the drain voltages of $\mathrm{M_N}$ and $\mathrm{M_{Ns}}$ ($V_{\rm gnd}$ and $V_{\rm s}$, respectively) as inputs. Ideally, $\mathrm{M_1}$ and $\mathrm{M_2}$ supply the bias currents $I_{\rm b}$ and $\mathrm{M_5}$ supplies the sensed current $I_{\rm Ns}$. As $I_{\rm Ns}$ is very small, the gate voltages of $\mathrm{M_5}$ and $\mathrm{M_2}$ differ by a few hundred millivolts at most, providing a good matching between the pairs $(\mathrm{M_1}, \mathrm{M_2})$ and $(\mathrm{M_3}, \mathrm{M_4})$, and forcing $V_{\rm s}$ to be equal to $V_{\rm gnd}$. Therefore, the sensed current $I_{\rm Ns}$ is equal to $(1/1500)I_{\rm N}$ and is mirrored to $R_{\rm N}$ to give $V_{\rm N}$ for control. The scaling of 1:1500 is rather accurate when $I_{\rm N}$ is large, for example, of the order of 100 mA.

B. Frequency Error Detector (FED)

The ADC consists of the FED and the VCD, as shown in Figs. 6 and 8, respectively. The voltage $V_{\rm cmp}$ in Fig. 6 is the output of the comparator that compares $V_{\rm ref}$ and $V_{\rm o}$ of the converter shown in Fig. 3. The switching period of $V_{\rm cmp}$ is $\mathrm{T_{cmp}}$, which is also the switching period of the converter. The FED

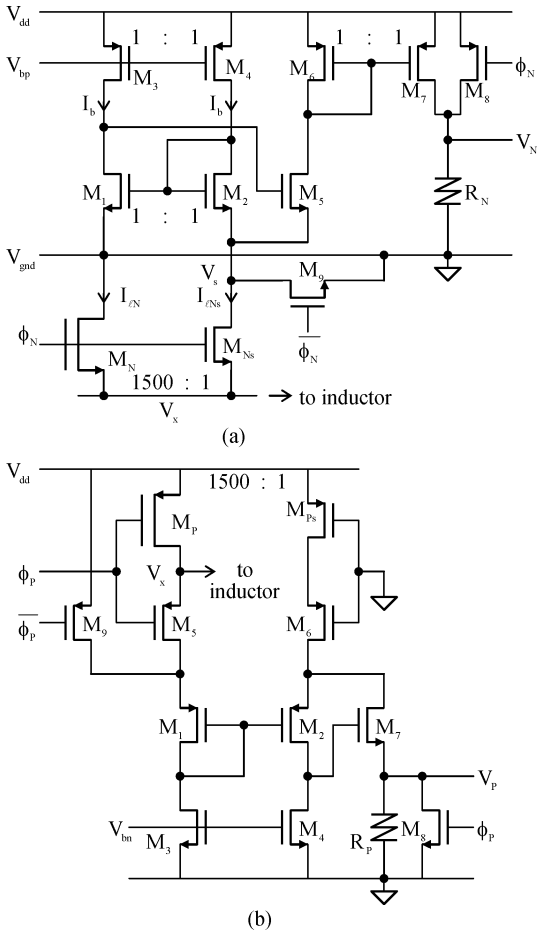

Fig. 5. Current sensor for (a) $\mathrm{M_N}$ and (b) $\mathrm{M_P}$.

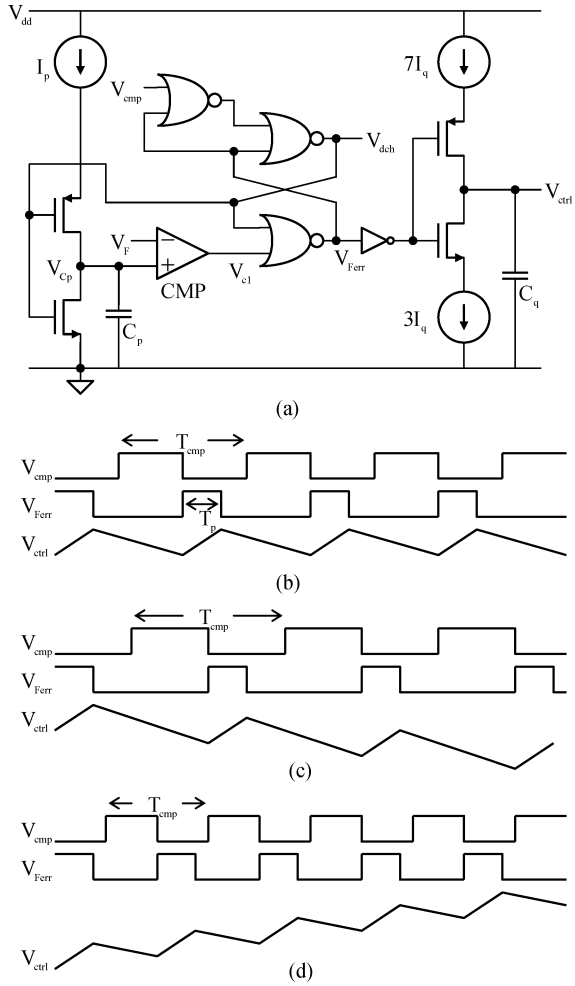

Fig. 6. (a) FED. (b) $T_{\mathrm{cmp}}/T_{\mathrm{p}} = 10/3$. (c) $T_{\mathrm{cmp}}/T_{\mathrm{p}} > 10/3$. (d) $T_{\mathrm{cmp}}/T_{\mathrm{p}} < 10/3$.

detects the frequency error (V_{Ferr}) between $1/\mathrm{T_{cmp}}$ and the switching frequency f_{s} defined by V_{F} and converts the error signal V_{Ferr} into the control signal V_{ctrl}, which is fed to the VCD for adjusting the delay.

Fig. 6(a) shows the detailed implementation of the FED. Initially, the timing capacitor C_{p} is discharged ($V_{\mathrm{dch}} =$ "1"), the output of the FED comparator V_{c1} is "0", and V_{Ferr} is "0". When V_{o} falls below V_{ref}, V_{cmp} switches from "1" to "0", the FED latch then switches to give $V_{\mathrm{dch}} =$ "0", turning on the current source I_{p} to charge up C_{p}, and setting V_{Ferr} to "1". When the voltage V_{Cp} reaches V_{F}, V_{Ferr} is reset to "0", shutting off I_{p} and discharging C_{p} back to GND. The duration for $V_{\mathrm{Ferr}} =$ "1" is $\mathrm{T_p} = V_{\mathrm{F}}C_{\mathrm{p}}/I_{\mathrm{p}}$. Hence, every time V_{cmp} falls to "0", a pulse of length T_{p} is generated at V_{Ferr}. This pulse train is then filtered by a subsequent charge pump with a charging current I_{ch} of $7I_{\mathrm{q}}$ and a discharging current I_{dch} of $3I_{\mathrm{q}}$ such that the filtered signal V_{ctrl} will finally be settled down when $T_{\mathrm{cmp}} = 10T_{\mathrm{p}}/3 = T$, as shown in Fig. 6(b). If $T_{\mathrm{cmp}} > T$, as shown in Fig. 6(c), V_{ctrl} will fall, shortening the delay. Similarly, if $T_{\mathrm{cmp}} < T$, as shown in Fig. 6(d), V_{ctrl} will rise, lengthening the delay from the VCD block. Hence, the delay is adaptively adjusted to regulate T_{cmp} to be T.

The ratio of the charging current I_{ch} to the discharging current I_{dch} has to be larger than 1 (7/3 in this case) to avoid ambiguity in delay compensation. If the ratio is smaller than 1, when

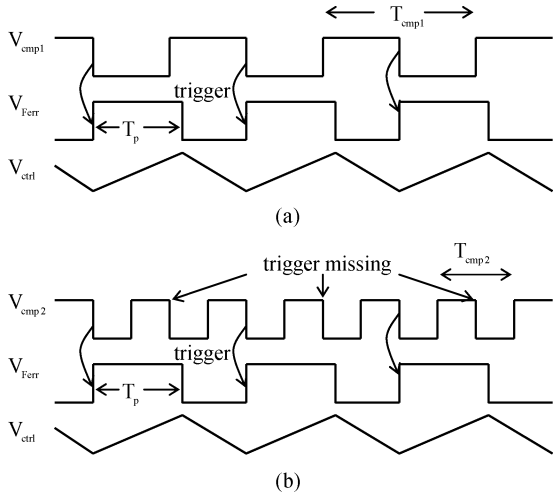

Fig. 7. Demonstrating ambiguity in delay compensation.

V_{ctrl} reaches the steady state, its duty cycle must be larger than 0.5. For example, assuming that $I_{\mathrm{ch}}/I_{\mathrm{dch}} = 0.5$ as shown in Fig. 7(a) and (b), and the duty cycle of V_{Ferr} is 2/3 in the steady state. In the frequency error detector, the falling edge of V_{cmp} will trigger V_{Ferr} with a pulse T_{p} wide only when V_{Ferr} is "0."

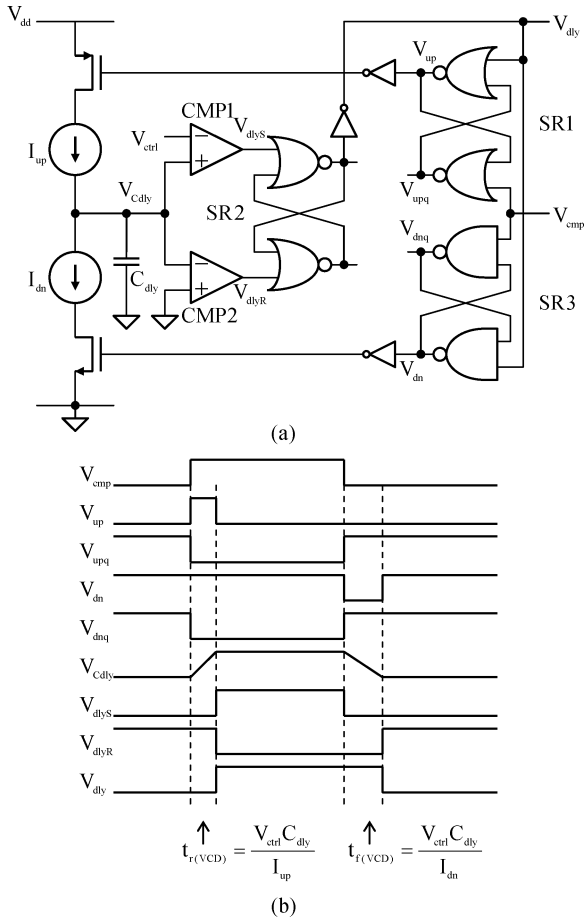

Fig. 8. (a) VCD. (b) Waveforms of various nodes.

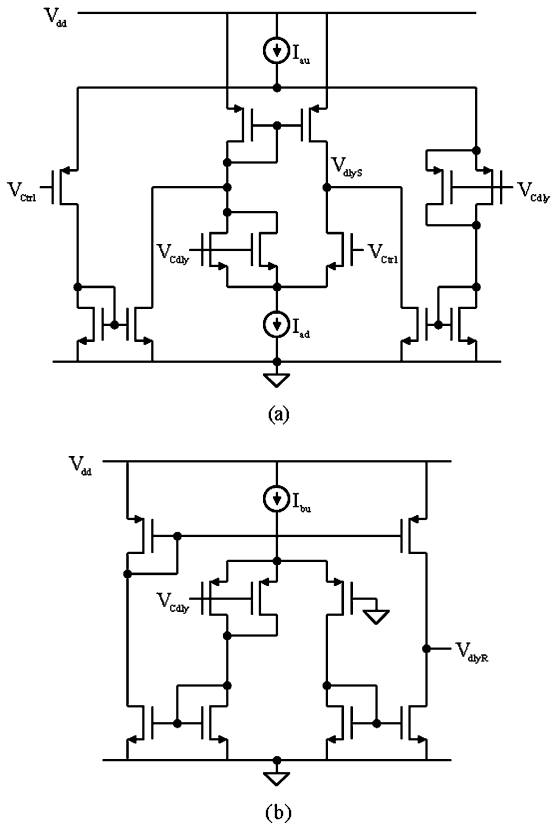

Fig. 9. Comparators for VCD: (a) CMPa and (b) CMPb.

During the $T_{\rm p}$ period, $V_{\rm Ferr}$ = "1" and any new coming triggering signals will be missed out. As shown in Fig. 7(b), $V_{\rm cmp2}$ misses one trigger every two periods. Compared with Fig. 7(a), for the same $V_{\rm ctrl}$ and $V_{\rm Ferr}$ waveforms, $2T_{\rm cmp2} = T_{\rm cmp1} = T$, and both $1/T$ and $1/2T$ could be the switching frequency of the system, causing ambiguity. If $I_{\rm ch}/I_{\rm dch} > 1$, then the duty cycle of $V_{\rm Ferr}$ in the steady state must be less than 0.5, which guarantees no trigger will be missed when $V_{\rm ctrl}$ settles in the steady state, avoiding ambiguity. It should be noted that the matching accuracy between $I_{\rm ch}$ and $I_{\rm dch}$ (7:3 in this case) is not critical as long as the ratio is larger than 1.

C. Voltage Controlled Delay (VCD)

Fig. 8(a) shows the implementation of the VCD. The input signal of VCD is $V_{\rm cmp}$, which is the output of the comparator that compares $V_{\rm ref}$ and $V_{\rm o}$. The output signal is $V_{\rm dly}$, and is the delayed version of $V_{\rm cmp}$. When $V_{\rm cmp}$ changes from "0" to "1," the charging current $I_{\rm up}$ is directed to charge $C_{\rm dly}$ from 0 V to $V_{\rm ctrl}$. After a delay of $t_{\rm r(VCD)} = V_{\rm crtl} \times C_{\rm dly}/I_{\rm up}$, the output signal $V_{\rm dly}$ jumps from "0" to "1" [Fig. 8(b)]. Similarly, when $V_{\rm cmp}$ changes from "1" to "0," the discharging current $I_{\rm dn}$ is directed to discharge $C_{\rm dly}$ from $V_{\rm ctrl}$ to 0 V. After a delay of $t_{\rm f(VCD)} = V_{\rm crtl} \times C_{\rm dly}/I_{\rm dn}$, the output signal $V_{\rm dly}$ jumps from "1" to "0." Hence, $V_{\rm dly}$ is the delayed version of $V_{\rm cmp}$, with a rising edge delay of $t_{\rm r(VCD)}$ and a falling edge delay of $t_{\rm f(VCD)}$. Some of the crucial waveforms of the VCD are shown in Fig. 8(b). The exact description of the action of the three latches is tedious but straightforward, and is not provided. However, we want to mention that in order to obtain the correct signals, $\rm SR_1$ and $\rm SR_2$ are NOR latches and $\rm SR_3$ is a NAND latch. Due to forbidden states, the outputs of an SR latch are not complementary signals and, therefore, inverters are used to convert $V_{\rm up}$ and $V_{\rm dn}$ correctly to drive the switches for $I_{\rm up}$ and $I_{\rm dn}$, respectively.

The comparator CMPa should have a rail-to-rail input stage to accommodate for the wide voltage ranges of $V_{\rm Cdly}$ and $V_{\rm ctrl}$, and the comparator CMPb should be ground sensing. Fig. 9(a) shows the schematic of CMPa, which consists of a p-input amplifier and an n-input amplifier. When the inputs are close to $V_{\rm dd}$, the p-input amplifier is shut off, and when the inputs are close to ground, the n-input amplifier is shut off. Hence, the gain of the comparator changes with the input signals. As long as the gain is high enough, the comparator could function as designed. Fig. 9(b) shows the schematic of CMPb. For both comparators, built-in offset voltages are introduced by assigning different sizes to the input transistors. For example, a positive offset voltage $V_{\rm osB}$ is introduced at the positive input terminal of CMPb, such that the signal $V_{\rm dlyR}$ switches from "0" to "1" as soon as $V_{\rm Cdly}$ is discharged below $V_{\rm osB}$ instead of 0 V. The offset voltages for other comparators are introduced similarly, and clearly, the delays $t_{\rm r(VCD)}$ and $t_{\rm f(VCD)}$ have to be adjusted accordingly.

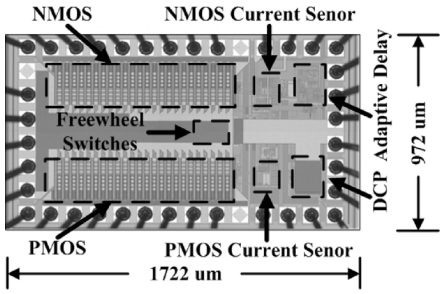

Fig. 10. Micrograph of fabricated chip.

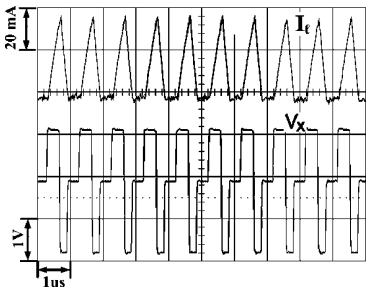

Fig. 11. Typical profiles of I_ℓ and $V_{\rm X}$ in the steady state.

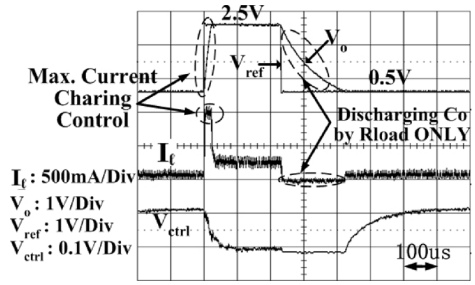

Fig. 12. Typical reference tracking response.

V. Measurement Results

The converter was fabricated in a 0.35 μm CMOS process, and the micrograph is shown in Fig. 10. The freewheel switch is very small as it only needs to conduct a current of 10 mA. Fig. 11 shows the inductor current I_ℓ and the switching node voltage $V_{\rm x}$ when the converter is operating in PCCM in the steady state. The adaptive delay compensator regulates the switching frequency at 850 kHz. With the load current $I_{\rm load} = 50$ mA and the freewheel current $I_{\rm pccm} = 10$ mA, the control loop gives the peak inductor current as 135 mA. Fig. 12 shows a typical reference tracking response for a switching of the reference voltage between 0.5 and 2.5 V with a fixed $R_{\rm load} = 10\ \Omega$. For the up-tracking case, the maximum current charging control worked as expected, limiting the inductor current to within the bounds of $I_{\rm Pmax} = 1$ A and $I_{\rm Nmin} = 0.8$ A. The up-tracking speed is 12.5 μs/V (the ideal up-tracking speed is 11 μs/V, where $t_{\rm ideal} = C_{\rm o}(V_2 - V_1)/(I_{\rm Pmax} - I_{\rm load})$). For down-tracking, $C_{\rm o}$ (10 μF) is discharged by $R_{\rm load}$ only, and the output settled in 200 μs. The ADC controlling voltage $V_{\rm ctrl}$ (which is the output voltage of the frequency error detector) settled within 200 μs for both the up- and down-tracking cases. Fig. 13 shows the tracking responses under different $I_{\rm load}$, with a step change in the reference voltage of 0.5 V. Obviously, a heavy output load current makes the up-tracking time longer and the down-tracking time shorter. Fig. 14 shows the tracking responses when the direct charging path is activated. For a load current of 500 mA, the up-tracking speed is 5 μs/0.5 V with DCP [Fig. 14(a)], compared with 30 μs/0.5 V without DCP [Fig. 14(b)]. Fig. 15 shows the converter switching frequency

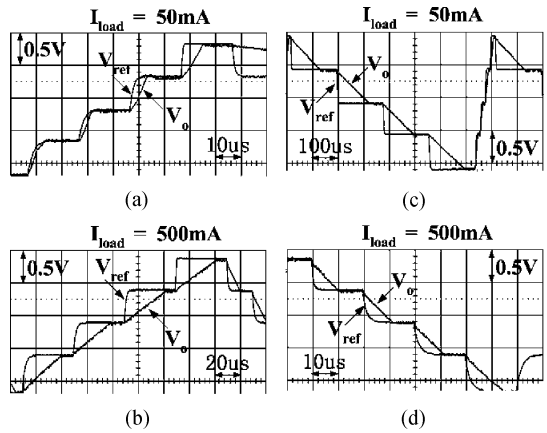

Fig. 13. Reference tracking responses under different $I_{\rm load}$. (a) Up-tracking from 0.5 V to 2.5 V with $I_{\rm load} = 50$ mA. (b) Up-tracking from 0.5 V to 2.5 V with $I_{\rm load} = 500$ mA. (c) Down-tracking from 2.5 V to 0.5 V with $I_{\rm load} = 50$ mA. (d) Down-tracking from 2.5 V to 0.5 V with $I_{\rm load} = 500$ mA.

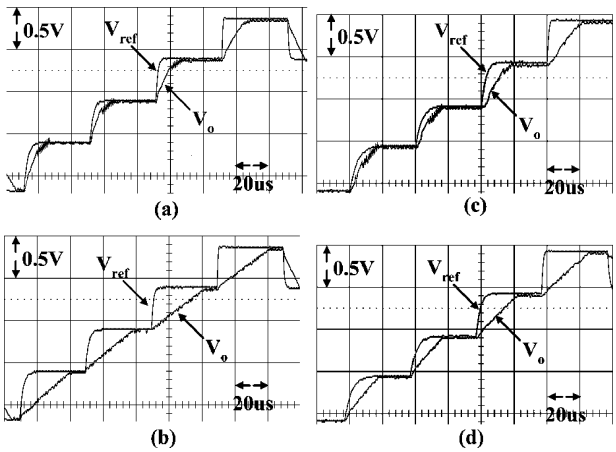

Fig. 14. Reference tracking responses with and without DCP. (a) Up-tracking from 0.5 V to 2.5 V with DCP at $I_{\rm load} = 500$ mA. (b) Up-tracking from 0.5 V to 2.5 V without DCP at $I_{\rm load} = 500$ mA. (c) Up-tracking from 0.5 to 2.5 V with DCP at $R_{\rm load} = 10\ \Omega$. (d) Up-tracking from 0.5 to 2.5 V without DCP at $R_{\rm load} = 10\ \Omega$.

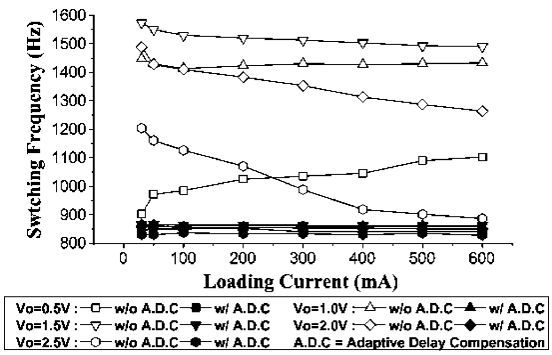

Fig. 15. Switching frequency with and without ADC.

TABLE I
SUMMERY OF FABRICATED CHIP

Fabrication Process	AMS 0.35μm 2P4M
Chip Area	1.674mm^2 (972 μm x 1722 μm)
Supply Voltage V_{dd}	3V
Output Voltage V_{out}	0.5V ~ 2.5V
Loading Current I_{load}	30mA ~ 500mA
Power Efficiency η	88% ~ 94.5% @ V_{out} = 1.5V
Inductor / Capacitor	L = 4.7u; C_o=10u
Switching Frequency f_s	850kHz to within ±2.5% error @ V_{dd}=3V
Maximum Charging Current	I_H = 1A ; I_L = 800mA
Reference Tracking Speed (without DCP)	25μs for 0.5V → 2.5V with R_{load} = 10 Ω
	200μs for 2.5V → 0.5V with R_{load} = 10 Ω
Reference Tracking Speed (with DCP)	12μs for 0.5V → 2.5V with R_{load} = 10 Ω
	200μs for 2.5V → 0.5V with R_{load} = 10 Ω

with and without adaptive delay compensation. With no delay compensation, for $V_{\rm dd} = 3.0$ V, the switching frequency changes from 886 kHz to 1.57 MHz, a change of ±28% w.r.t. the average frequency of 1.23 MHz. With delay compensation, the range is from 828 to 866 kHz, which is a minute change of only ±2.2% and is within 5% of the target frequency of 850 kHz. Table I summarizes the design parameters and the measurement results.

VI. CONCLUSION

We proposed, fabricated, and tested an integrated hysteretic buck converter with maximum charging current control to achieve fast reference tracking. The measured up-tracking speed was close to the ideal tracking speed as discussed in Section II. The variable frequency nature usually associated with hysteretic converters was corrected by introducing an adaptive delay compensator, and a fixed frequency converter was achieved. Measurement results cope well with the theoretical analysis and simulation results (not shown), and we conclude that maximum charging current control is suitable for power management implementing dynamic voltage scheduling.

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