

Widely Tunable 4th Order Switched G_m -C Band-Pass Filter Based on N-Path Filters

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Abstract—A widely tunable 4th order BPF based on the subtraction of two 2nd order 4-path passive-mixer filters with slightly different center frequencies is proposed. The center frequency of each 4-path filter is slightly shifted relative to its clock frequency (one upward and the other one downward) by a g_m -C technique. Capacitive splitting of the input signal is used to reduce the mutual loading of the two 4-path BPFs and increase their quality factors. The filter is tunable from 0.4 GHz to 1.2 GHz with approximately constant bandwidth of 21 MHz. The in-band 1-dB compression point of the filter is -4.4 dBm while the in-band IIP₃ of the filter is $+9$ dBm and the out-of-band IIP₃ is $+29$ dBm ($\Delta f = +50$ MHz). The ultimate rejection of the filter is >55 dB and the NF of the filter is 10 dB. The static and dynamic current consumption of the filter are 2.8 mA from 2.5 V and 12 mA from 1.2 V, respectively (at 1 GHz). The LO leakage power to the input port is <-60 dBm. The filter has been fabricated in CMOS LP 65 nm technology and the active area is 0.127 mm^2 .

Index Terms—Bandpass filter (BPF), N-path, tunable, subtraction, g_m -C, complex baseband impedance, high-Q, shifting the center frequency, impedance transformation, passive mixer.

I. INTRODUCTION

THE trend towards reconfigurable radio transceiver architectures asks for band-pass filters with good selectivity and a flexibly tunable center frequency. The off-chip available solution is to use an array of dedicated, bulky, off-chip and non-tunable filters such as SAW filters. Although BAW filters [1], [2] have been introduced as a system in package solutions, their center frequency is sensitive to the thickness variation of the piezoelectric material and the achievable tunability is quite limited [1], [2]. If they are used for reconfigurable receivers, an array of them is necessary which again leads to the usage of a considerable amount of area. On the other hand, there are several techniques to make integrated RF band-pass filters such as LC filters [3]–[5], often with Q-enhancement techniques, g_m -C filters [5]–[7], N-path and pseudo N-path filters [8]–[14]. LC filters have several disadvantages such as high area consumption due to inductors which do not obey process scaling and have low quality factor, limited tunability and poor dynamic range [3]–[5]. The main drawbacks of g_m -C filters are the tradeoffs

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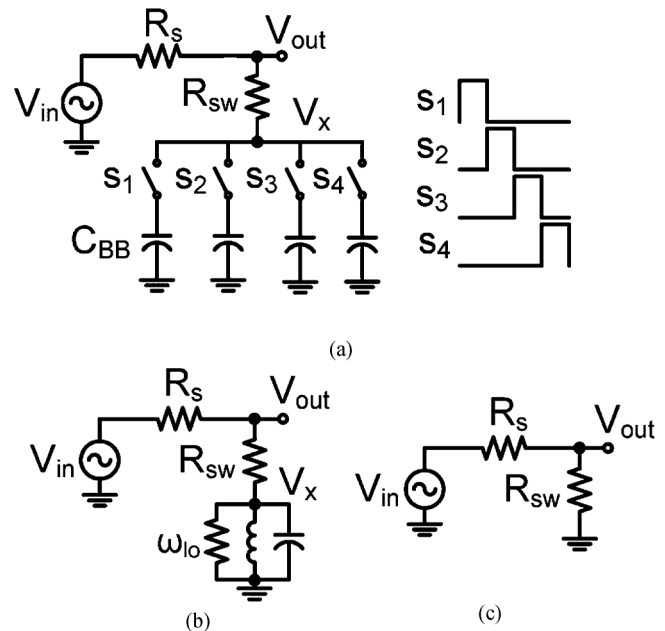


Fig. 1. (a) A conventional 4-path filter (b) its LTI equivalent around f_{lo} and (c) equivalent circuit for evaluating the ultimate rejection.

among power consumption, quality factor, center frequency and dynamic range and the need for tuning circuitry [5], [7], [15].

Recently there has been renewed interest in the translational impedance conversion of N-path filters [14], [16]–[20]. Due to the “transparency” of the passive mixer, the baseband impedance is translated to frequencies around the clock frequency f_{lo} [8]–[10]. Interesting features of these filters are their direct tunability with f_{lo} , potentially higher quality factor compared to on-chip CMOS LC filters, high linearity and graceful scaling with process. N-path filters with capacitive baseband impedances can imitate an RLC tank whose center frequency can be tuned by changing its clock frequency f_{lo} [8], [14], [21]. A 4-path filter with capacitive baseband impedances and its LTI (Linear Time Invariant) equivalent around f_{lo} are depicted in Fig. 1(a) and (b), respectively [14], [16]–[19], [21]. At frequencies far from f_{lo} , the baseband capacitors will be shorted to ground and thus the filter will be simplified to a simple resistive division between source resistance R_s and switch resistance R_{sw} [16] (Fig. 1(c)).

N-path filters [21] have two main limitations: 1) The switch resistance R_{sw} limits the ultimate rejection to $R_{sw}/(R_{sw} + R_s)$ where R_s is the source impedance (16 dB for $R_s = 50 \Omega$ and $R_{sw} = 10 \Omega$) [14], [16], [20]; 2) Recently published N-path filters have only second order filtering, and higher orders have

only been achieved by cascading [13], still rendering a “round” band-pass filter shape.

In [22] a new method to increase the order of the band-pass filter while having a better pass-band shape compared to [13], [21] has been proposed. It [22] also weakens the effect of the switch-resistance on the ultimate rejection obtaining >55 dB ultimate rejection in a 65 nm CMOS chip. This paper analyzes the filter properties, especially its transfer function, noise figure and the effect of signal splitting. Furthermore, it compares practically achieved results with theory and simulation.

The outline of the paper is as follows: In Section II, the idea of subtraction as a method to obtain a 4th order BPF from two 2nd order BPFs with different center frequencies will be introduced. Subsequently, in Section III the idea of shifting the center frequency of a 4-path filter upward and downward exploiting a switched g_m -C technique will be discussed. Moreover, we discuss how the frequency shifts are implemented using a switched g_m -C technique. Consequently, utilization of this idea into the subtraction circuit, will be discussed. In Section IV, signal splitting to supply the input voltage signal to the two shifted 4-path 2nd order BPFs and its effect on the resultant filter will be discussed. Section V and VI discuss the filter realization and measurements, respectively. In Section VII, conclusions will be drawn.

II. INCREASING BPF ORDER BY SUBTRACTION

In this work, we propose to use subtraction as a means to achieve a 4th order band-pass filter from the two 2nd order band-pass filters with slightly different center frequencies. The main idea is illustrated in Fig. 2. Intuitively, the relation between the phase of V_{out1} and V_{out2} (ϕ_1 and ϕ_2) is approximately $\phi_1 = -\phi_2$ in the pass-band of the resultant filter and therefore due to the subtraction, they will add up. However, for frequencies far out of the pass-band region of the resultant filter, the signals in the 2 paths are almost in-phase $\phi_1 = \phi_2$ and will cancel each other. Mathematically, the transfer function of each path in Fig. 2 is:

$$H_i(s) = \frac{V_{out,i}(s)}{V_{in}(s)} = \frac{R_p}{R_s + R_p} \times \frac{\omega_{3dB,i}s}{s^2 + \omega_{3dB,i}s + \omega_{ci}^2} \quad i = 1, 2 \quad (1)$$

where ω_{ci} and $\omega_{3dB,i}$ are center frequencies and bandwidths of the two paths. If the bandwidth of each path is the same ($\omega_{3dB,1} = \omega_{3dB,2} = \omega_{3dB}$) and assuming that $\omega_{c1} = \omega_c + 0.5\Delta\omega_c$ and $\omega_{c2} = \omega_c - 0.5\Delta\omega_c$, the total transfer function of the resultant filter will be:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{R_p}{R_s + R_p} \times \frac{2\omega_{3dB} \times \omega_c \times \Delta\omega_c \times s}{(s^2 + \omega_{3dB}s + \omega_{c1}^2)(s^2 + \omega_{3dB}s + \omega_{c2}^2)} \quad (2)$$

Now, we want to synthesize a 4th order BPF which has a bandwidth of BW(Hz) and is centered at ω_c . Let us assume that the desired LPF prototype is $k/(s^2 + as + b)$. For this purpose, the values needed for $\Delta\omega_c$ and ω_{3dB} are $2\pi BW \times \sqrt{4b - a^2}$ and $2\pi BW \times a$, respectively. For example, by subtracting the

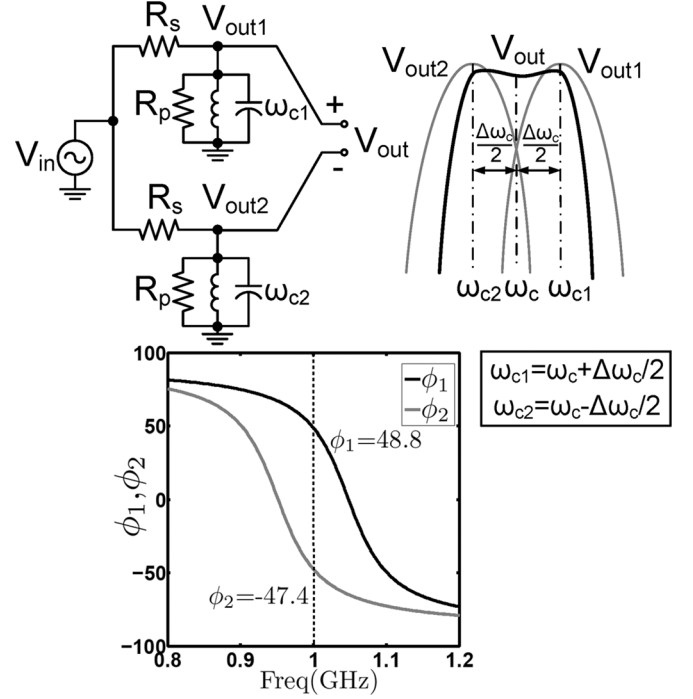


Fig. 2. Obtaining a 4th order BPF based on the subtraction of two 2nd order BPFs with slightly different center frequencies; The relation between the phase of each path (ϕ_1, ϕ_2): in the pass-band of the resultant filter is approximately $\phi_1 = -\phi_2$ and for frequencies far out of the pass-band region of the resultant filter, the signals in the 2 paths are almost in-phase ($\phi_1 = \phi_2$).

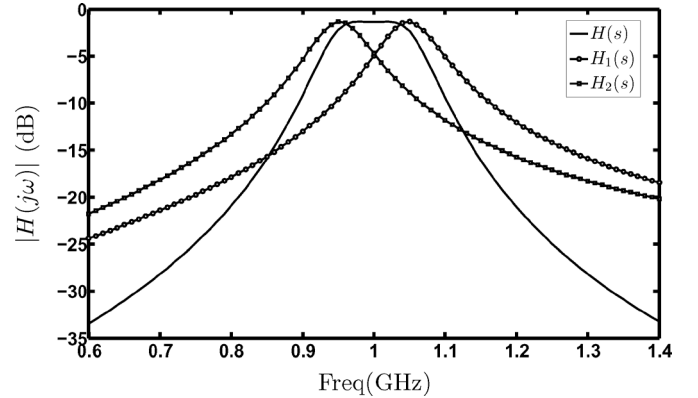


Fig. 3. A 4th order BPF centered at $f_c = 1$ GHz with BW = 124 MHz and 0.05 dB ripple ($a = 0.7, b = 0.27$) centered at 1 GHz as a result of the subtraction of two 2nd order BPFs with bandwidths of 87 MHz centered at $f_{c1} = 1.05$ GHz and $f_{c2} = 0.95$ GHz ($R_s = 50 \Omega$ and $R_p = 300 \Omega$).

outputs of two 2nd order BPFs with bandwidth of 87 MHz centered at $f_{c1} = 1.05$ GHz and $f_{c2} = 0.95$ GHz, a 4th order BPF centered at $f_c = 1$ GHz with 0.05 dB ripple and bandwidth of 124 MHz will result (Fig. 3).

Each RLC tank in Fig. 2 can be replaced by a 4-path passive mixer filter with different clock frequencies (f_{c1} and f_{c2} , one for each path). In this way, a tunable 4th order BPF can be made (Fig. 4(a)). Another property of this filter is that it can improve the limited ultimate rejection of conventional N-path filters. The filter shown in Fig. 4(a) will reduce to Fig. 4(b), for input frequencies far from the center frequency of the filter. In the case of no mismatch in the subtraction and the switch resistance values

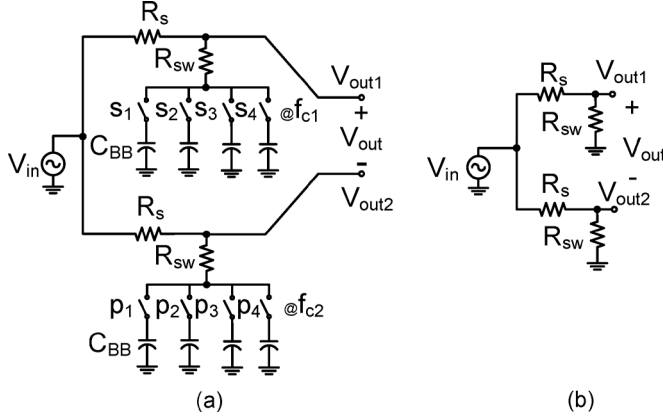


Fig. 4. (a) A 4th order tunable BPF using two different clock frequencies and (b) equivalent circuit to find the ultimate rejection.

of upper and lower paths, the ultimate rejection will be infinite ($R_{sw}/(R_{sw} + R_s) - R_{sw}/(R_{sw} + R_s) = 0$). In case of switch resistance mismatch ΔR_{sw} between upper and lower path, the ultimate rejection will be limited to $\Delta R_{sw}/(R_{sw} + R_s)$. Compared to the ultimate rejection of conventional N-path filters, a great improvement has been introduced. For example for a 1% mismatch between the switch resistance values of the upper and lower path and assuming $R_{sw} = 10 \Omega$ and $R_s = 50 \Omega$, the ultimate rejection will be 55 dB compared to 16 dB ultimate rejection of conventional N-path filters. A disadvantage of the filter shown in Fig. 4(a) is the need for a complicated clock circuitry. Instead, an alternative way is proposed to realize the filter with just one clock frequency which is discussed in Section III.

III. SHIFTING THE CENTER FREQUENCY OF A 4-PATH FILTER

The idea of shifting the center frequency of the 4-path filter with respect to the switching frequency f_{lo} using a g_m -C technique is illustrated in Fig. 5. The idea of shifting the center frequency of a 4-path filter has recently also been proposed independently in [18]. By exploiting the poly-phase signals in the baseband of a 4-path filter, its center frequency can be changed upward or downward with respect to the clock frequency. By doing a clockwise and counter clockwise feeding of the g_m cells to the baseband nodes ($V_{bi}, 1 \leq i \leq 4$) of a 4-path filter with capacitive baseband impedances, the center frequency of the filter is changed to $f_{lo} + g_m/(2\pi C_{BB})$ and $f_{lo} - g_m/(2\pi C_{BB})$, respectively. Consequently, the upper and lower path of the filter depicted in Fig. 4(a) can be substituted by the circuits shown in Fig. 5(a) and (b), respectively. In this way instead of two different clock frequencies, one clock frequency will suffice. This is a great advantage, because considering two slightly different clock frequencies on an IC will cause serious interference problems.

When f_{in} is around $k f_{lo}$, the phase relation between the voltages of baseband nodes $V_{bi} (1 \leq i \leq 4)$ of a 4-path filter can be described by $V_{bm} = V_{bn} e^{+jk\pi/2 \times (m-n)}$, ($1 \leq (m, n) \leq 4$). By exploiting that, the interactions between the baseband nodes due to the g_m cells in filters shown in Fig. 5 can be lumped to an effective baseband admittance $Y_{BB}(s, k)$ when the input frequency is around $k f_{lo}$.

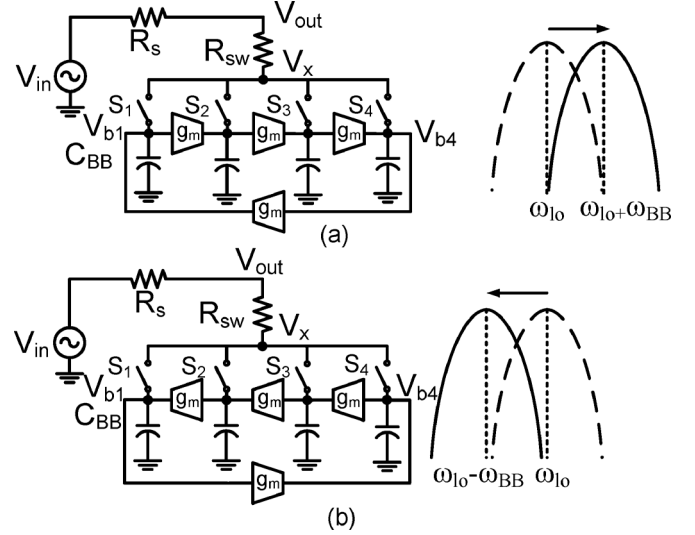


Fig. 5. Clockwise and counter clockwise feeding of the g_m cells in baseband nodes to shift the center frequency of a 4-path filter a) upward and b) downward compared to ω_{lo} by $\omega_{BB} = g_m/C_{BB}$.

$Y_{BB}(s, k)$ for f_{in} around $k f_{lo}$ ($1 \leq k \leq 3$) for filter shown in Fig. 5(a) is illustrated in Fig. 6(a). From Fig. 6(a), $Y_{BB}(s, 1) = C_{BB}(s - j\omega_{BB})$, $Y_{BB}(s, 2) = sC_{BB} - g_m$ and $Y_{BB}(s, 3) = C_{BB}(s + j\omega_{BB})$, where ω_{BB} is g_m/C_{BB} (In the same way the filter shown in Fig. 5(b) can be analyzed). Therefore the center frequency of the baseband admittance is modified from zero to ω_{BB} for $Y_{BB}(s, 1)$ and $-\omega_{BB}$ for $Y_{BB}(s, 3)$, however for $Y_{BB}(s, 2)$, the center frequency of the baseband admittance does not change. In N-path filters, the baseband admittance characteristics will be translated to $k f_{lo}$ $k \in \mathbb{Z}$ [8], [9], [19]. This means that the center frequency of the filter shifts upward around f_{lo} and downward around $3f_{lo}$ by $g_m/(2\pi C_{BB})$. The situation is different around $2f_{lo}$ in which the center frequency does not change. Instead the g_m s create a negative resistance, $-1/g_m$, in parallel with each baseband capacitor which leads to an increase in the pass-band gain and reduction of bandwidth at $2f_{lo}$. This behavior is shown in Fig. 6(b).

It is found that exploiting the differential G_m s ($G_m = 0.5g_m$) with good common-mode rejection can prevent the creation of this negative resistance¹ at $2f_{lo}$. Exploiting the differential G_m s is illustrated in Fig. 7. The filter with the differential G_m s acts the same as the one with the single-ended g_m s for input frequencies around f_{lo} and $3f_{lo}$, however for input frequencies around $2f_{lo}$ because of the fact that $V_{b1} = V_{b3}$ and $V_{b2} = V_{b4}$, the output current of both differential G_m s will be diminished to zero ($G_m(V_{b1} - V_{b3}) = G_m(V_{b2} - V_{b4}) = 0$). As a result, there will be no effect from the differential G_m s and the filter operates similar to a conventional 4-path filter for input frequencies around $2f_{lo}$. The frequency shifting with single-ended and differential transconductances has been compared in Fig. 8 (see Section V). As can be seen, exploiting the differential G_m s suppresses the positive feedback at even harmonics of f_{lo} . Fig. 9 shows a tunable 4th order BPF based on the subtraction of two 2nd order BPFs whose center frequencies are shifted upward and downward relative to f_{lo} using the differential G_m cells.

¹The condition for the stability is $g_m < 1/(4(R_s + R_{sw}))$.

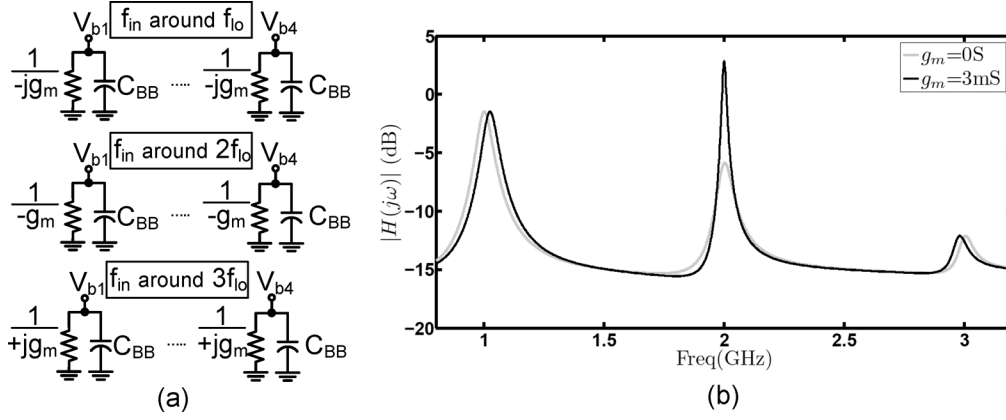


Fig. 6. (a) Effective baseband admittance $Y_{BB}(s, k)$ ($1 \leq k \leq 3$) for filter shown in Fig. 5(a), V_{bi} s ($1 \leq i \leq 4$) are the baseband nodes of the filter; and (b) SpectreRF simulation of Fig. 5(a) with $g_m = 0$ mS and 3 mS ($R_s = 50 \Omega$, $R_{sw} = 10 \Omega$, $C_{BB} = 20$ pF and $\omega_{lo} = 1$ GHz).

Additionally, a second set of switches has been added to each path to increase the ultimate rejection of each path. In this way, node V_x instead of node V_{out} in Fig. 5(a) and (b) is exploited. Therefore the ultimate rejection of the filter will be much less prone to the mismatch in the subtraction circuitry and switches. As mentioned before, there is no contribution from the differential G_m s at $2f_{lo}$ in both paths. As a result, both paths operate similar to each other and accordingly the band-pass filter shape at $2f_{lo}$ will be suppressed due to the subtraction (Fig. 10). Using (15), we can calculate the transfer function of the filter around f_{lo} (3). $G(s, k)$ is a LPF due to the combination of the baseband and source admittances which due to the transparency of the switches is translated to a BPF around kf_{lo} . The transfer function of the filter around f_{lo} can be found by using two terms ($k = -1, 1$) of (15).

$$\begin{aligned} T_1(s) &= \frac{V_{out1}(s)}{V_{in}(s)} \\ &= \frac{8}{\pi^2} \times (G(s - j\omega_{lo}, 1) + G(s + j\omega_{lo}, -1)) \end{aligned} \quad (3)$$

where $G(s, \pm 1)$ is:

$$\begin{aligned} G(s, \pm 1) &= \frac{1}{1 + 4R_x Y_{BB}(s, \pm 1)} \\ &= \frac{1}{1 + 4R_x (sC_{BB} \pm jg_m)} \end{aligned} \quad (4)$$

and R_x is $R_s + R_{sw}$. Subsequently, $T_1(s)$ will be:

$$\begin{aligned} T_1(s) &= \frac{8}{\pi^2} \times \left(\frac{1}{1 - j4g_m R_x + 4R_x C_{BB}(s - j\omega_{lo})} \right) \\ &+ \frac{8}{\pi^2} \times \left(\frac{1}{1 + j4g_m R_x + 4R_x C_{BB}(s + j\omega_{lo})} \right) \\ &= \frac{8}{\pi^2} \times \frac{s/(2R_x C_{BB})}{s^2 + s/(2R_x C_{BB}) + \left(\frac{g_m}{C_{BB}} + \omega_{lo} \right)^2} \end{aligned} \quad (5)$$

$T_2(s)$ can be easily found by changing g_m to $-g_m$ in (5). Then, the total transfer function of the filter ($T(s) = T_1(s) - T_2(s)$) is described by (6) where $\omega_{c1} = \omega_{lo} + g_m/C_{BB}$ and $\omega_{c2} = \omega_{lo} - g_m/C_{BB}$. To synthesize a 4th order BPF with bandwidth of BW(Hz) which is centered at ω_{lo} and assuming that the desired LPF prototype is $k/(s^2 + as + b)$, the values needed for C_{BB} and g_m are $1/(4\pi a R_x \times BW)$ and $1/(4R_x) \times$

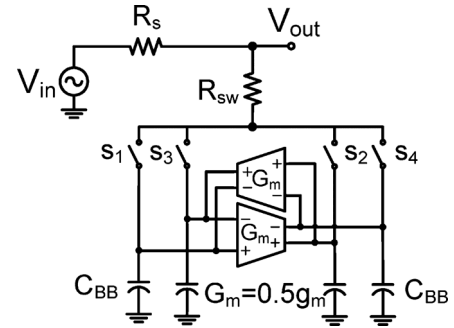


Fig. 7. Using the differential G_m s with good common-mode rejection instead of the single-ended ones to shift the center frequency of 4-path filter upward.

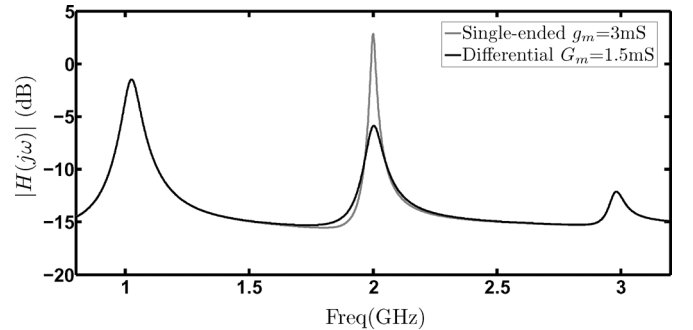


Fig. 8. SpectreRF simulation of Fig. 5(a) with $g_m = 3$ mS and Fig. 7 with $G_m = 1.5$ mS ($R_s = 50 \Omega$, $R_{sw} = 10 \Omega$, $C_{BB} = 20$ pF and $\omega_{lo} = 1$ GHz).

$\sqrt{4b/a^2 - 1}$, respectively. The bandwidth of the filter can be tuned by changing the value of C_{BB} while the value of G_m is constant. In fact, the G_m value determines the pass-band shape of the filter while the value of baseband capacitor C_{BB} determines the bandwidth of the filter. This feature can be used to accommodate multiple standards. For example for $R_s = 50 \Omega$ and $R_{sw} = 10 \Omega$, a tunable 4th order BPF with bandwidth of 20 MHz will result for $C_{BB} = 95$ pF and $G_m = 2.3$ mS (Fig. 10). Moreover, Fig. 10 shows the suppression of BPFs at even harmonics of f_{lo} .

$$\begin{aligned} T(s) &= \frac{V_{out}(s)}{V_{in}(s)} = T_1(s) - T_2(s) = \frac{16}{\pi^2} \times \frac{g_m \omega_{lo}}{R_x C_{BB}^2} \\ &\times \frac{s}{\left(s^2 + \frac{s}{2R_x C_{BB}} + \omega_{c1}^2 \right) \left(s^2 + \frac{s}{2R_x C_{BB}} + \omega_{c2}^2 \right)} \end{aligned} \quad (6)$$

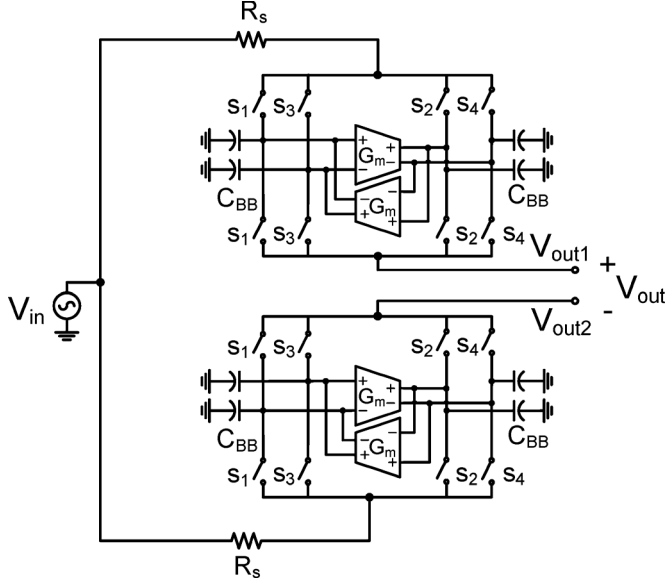


Fig. 9. A 4th order tunable BPF by the subtraction of two 2nd order BPFs which their center frequencies have been shifted upward and downward relative to f_{lo} ($G_m = 0.5g_m$) using switched g_m -C technique; A second set of switches has been added to each path to increase the ultimate rejection of each path.

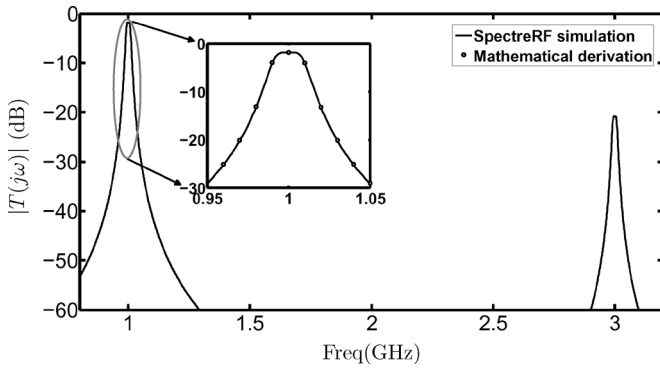


Fig. 10. Comparing SpectreRF simulation of the filter shown in Fig. 9 with mathematical derivation (6) for a 4th order BPF with bandwidth of 20 MHz ($a = 0.7$, $b = 0.27$) centered at 1 GHz ($R_s = 50 \Omega$, $R_{sw} = 10 \Omega$, $G_m = 2.3$ mS and $C_{BB} = 95$ pF) and demonstration of the suppression of band-pass filtering at even harmonics of f_{lo} .

IV. SPLITTING THE INPUT SIGNAL

In practice, the output resistance of V_{in} is not zero and this leads to an interaction between the two paths which is undesirable and will impact the transfer function of the filter. Therefore, it is needed to split the input voltage to each path while having as little interaction as possible between the two paths. There are several options to do this. For example, two amplifiers can be exploited for this purpose but this limits the linearity of the filter. The next possibility is using the time domain signal splitting by series switches with each path which are clocked by two anti-phase clock signals at $4f_{lo}$. For the proper operation of the filter in the time domain signal splitting, the clock signals of one path need to be shifted by $T_{lo}/8$ compared to the clock signals of the other path which complicates the clock circuitry. Another option is to use relatively high capacitive impedances compared to the source resistance (Fig. 11). Although it leads

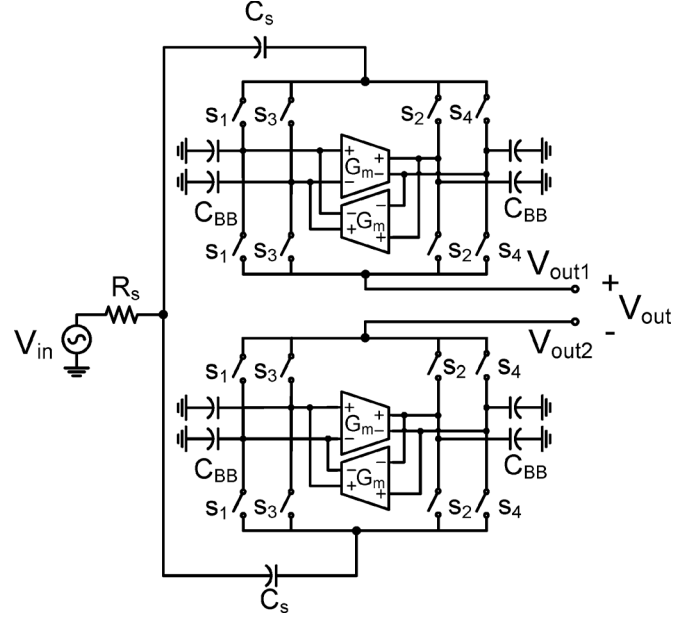


Fig. 11. Splitting the input signal and providing isolation between the paths by using relatively (compared to R_s) high series capacitive impedances C_s in each path.

to an increase in the NF of the filter, exploitation of the series capacitors is chosen due to its simplicity and considerable increase in the quality factor of the filter compared to the other approaches. Therefore the filter shown in Fig. 11 will be the implemented filter.

A. The Effect of Series Capacitor on a Conventional 4-Path Filter

First, the effects of addition of a series capacitor to each path in Fig. 11 individually while assuming $G_m = 0$ will be investigated. Intuitively, due to the fact that the input impedance of a 4-path filter imitates a parallel RLC tank, the addition of a series capacitor acts as an L-match [23] section and effectively increases the quality factor and the voltage gain of the filter. Moreover from Appendix, $V_{out1,2}/V_{in}$ in Fig. 11 by assuming that $\tau_s \omega_{lo} < 0.5$ ($\tau_s = R_x C_s$) and neglecting the mutual loading effect of each path on the other one,² will be:

$$T(s) = \frac{V_{out1,2}}{V_{in}} \cong \frac{8}{\pi^2} \times \frac{\tau_s s}{1 + \tau_s s} \times \frac{s/(2R_x C_{BB})}{s^2 + (C_s \omega_{lo}/(\pi C_{BB}))s + \omega_{lo}^2 \times (1 - C_s/(\pi C_{BB}))}. \quad (7)$$

The $|T|_{max} \cong 4/(\pi \sqrt{1 + \tau_s^2 \omega_{lo}^2})$ occurs at $f_c \cong f_{lo} \times (1 - 0.5C_s/(\pi C_{BB}))$. As an example, for $R_s = 50 \Omega$, $R_{sw} = 10 \Omega$, $C_{BB} = 20$ pF, $C_s = 1$ pF and $f_{lo} = 1$ GHz, the center frequency of the filter will be $f_c = 992$ MHz and the maximum gain will be $A_{v,max} = 1.5$ dB (Fig. 12). As can be seen, the gain has been increased by approximately 3.3 dB compared to a conventional 4-path filter. The quality factor of the filter can be approximated by $Q \cong \pi C_{BB}/C_s - 2$. The improvement in Q can be significant, e.g., from 15 to 60 for the case given in

²Removing the other path;

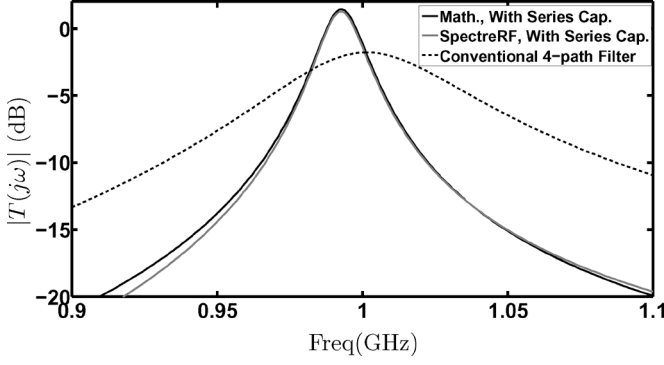


Fig. 12. SpectreRF simulation of one path in Fig. 11 with and without a series cap, $C_s = 1$ pF, while $G_m = 0$ and the other path is removed compared with mathematical derivation(7); $R_s = 50 \Omega$, $R_{sw} = 10 \Omega$, $C_{BB} = 20$ pF and $f_{lo} = 1$ GHz.

Fig. 12. Also shown in Fig. 12 is a comparison between the calculated filter shape (7) and the simulation.

The NF at node $V_{out1,2}$ for frequencies around f_{lo} by assuming that $\tau_s \omega_{lo} < 0.5$, $G_m = 0$ and neglecting the noise contribution of the second set of switches and loading effect of each path on the other one, is described in (8) (see (23)):

$$F(\omega) \cong \frac{\pi}{4} \times \left(1 + \frac{R_{sw}}{R_s}\right) \times \left(\omega_{lo} \tau_s + \frac{1}{\omega_{lo} \tau_s} \times \left(\frac{\omega_{lo}}{\omega}\right)^2\right). \quad (8)$$

For $R_s = 50 \Omega$, $R_{sw} = 10 \Omega$, $C_{BB} = 20$ pF, $C_s = 1$ pF and $f_{lo} = 1$ GHz, the NF of the filter is approximately 4.5 dB. Despite the increase in voltage gain due to the usage of a series capacitor, the NF of the filter increases compared to a conventional 4-path filter. Simulations correspond to calculations within 0.2 dB.

B. Transfer Function of the Implemented Filter

In the presence of a frequency shift due to the G_m cells, the transfer function shown in (7) needs to be modified. It is just needed to change ω_{lo} to $\omega_{lo} + g_m/C_{BB}$ and $\omega_{lo} - g_m/C_{BB}$ in (7) to find $T_1(s) = V_{out1}/V_{in}$ and $T_2(s) = V_{out2}/V_{in}$ in Fig. 11, respectively. By doing so, the total transfer function ($T = T_1 - T_2$) of the filter illustrated in Fig. 11 while neglecting the mutual loading effect of each path on the other one is described in:

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} \cong \frac{16g_m\omega_{lo}(1 - C_s/(\pi C_{BB}))}{\pi^2 C_{BB}^2 R_x} \times \frac{\tau_s s}{1 + \tau_s s} \times \frac{s}{(s^2 + \alpha s + \omega_{x1}^2) \times (s^2 + \alpha s + \omega_{x2}^2)} \quad (9)$$

where $\omega_{x1} = (\omega_{lo} + g_m/C_{BB}) \times \sqrt{1 - C_s/(\pi C_{BB})}$, $\omega_{x2} = (\omega_{lo} - g_m/C_{BB}) \times \sqrt{1 - C_s/(\pi C_{BB})}$ and $\alpha = C_s \omega_{lo}/(\pi C_{BB})$. To synthesize a 4th order BPF with bandwidth of BW(Hz) which is centered at ω_c and assuming that the desired prototype LPF is $k/(s^2 + as + b)$, the values needed for C_{BB} and g_m are $C_s \omega_{lo}/(2a\pi^2 \times BW)$ and $C_s \omega_{lo}/(2\pi) \times \sqrt{4b/a^2 - 1}$, respectively.

Interestingly, reducing the series capacitance C_s lowers the required values for C_{BB} and G_m for a certain bandwidth. To

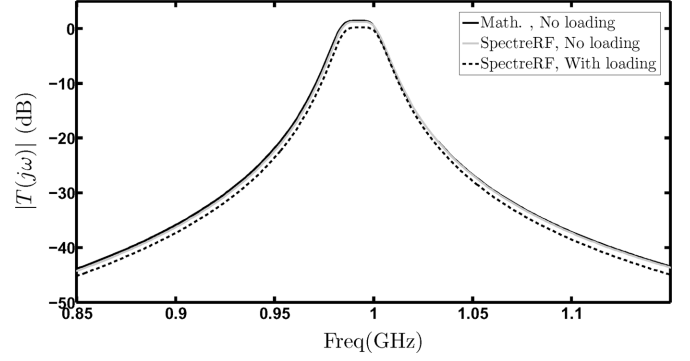


Fig. 13. Comparing SpectreRF simulation of the filter shape with and without considering the mutual loading effect of each path on the other one with the derived (9) where the mutual loading effect is not taken into account; $R_s = 50 \Omega$, $R_{sw} = 10 \Omega$, $C_{BB} = 20$ pF, $G_m = 0.5$ mS and $C_s = 1$ pF.

achieve a bandwidth of 20 MHz at 1 GHz while C_s is 1 pF, the values of C_{BB} and G_m will be 20 pF and 0.5 mS, respectively. However without using C_s , the required values are 95 pF and 2.3 mS (Fig. 10). This means that the total value of the baseband capacitances reduces from 380 pF to 80 pF in each path. Nevertheless, there is a tradeoff between the reduction in the value of series capacitor C_s and the NF of the filter (see Subsection C). In Fig. 13 the simulated filter shape is compared with derived (9). As can be seen, the mutual loading effect³ of each path on the other one leads to 1 dB degradation in voltage gain in the pass-band of the filter. Because of the frequency dependency of the impedance of the series capacitors, two values of 1.7 pF and 1 pF are used for C_s for $f_c = 0.4$ GHz – 0.7 GHz and $f_c = 0.7$ GHz – 1.2 GHz, respectively. The simulated transfer function of the proposed filter for center frequencies from 0.4 GHz to 1.2 GHz is illustrated in Fig. 14. The maximum pass-band ripple is 0.6 dB.

It is interesting to mention that the same reduction in the baseband capacitance values can be achieved, if the series capacitors are substituted by series resistors. In this case, the required series resistance value in each path is around 200 Ω which leads to the noise figure of 9.3 dB while by utilizing the series capacitors, the noise figure of the filter will be 5.6 dB (see subsection C), respectively.⁴

Finally, it should be mentioned that the N-path filters much like any hard switching mixers [24] suffer from folding-back from harmonics of f_{lo} to the pass-band of the filter at f_{lo} [14]. Increasing the number of phases relaxes this issue (folding back begins from $(N - 1) f_{lo}$ where N is the number of phases [18]). Moreover, folding back from harmonics of the f_{lo} , can be eliminated by a time-invariant wideband and fixed low-pass pre-filter. The down-conversion of up-converted baseband noise to harmonics of f_{lo} in the receiver can be eliminated by using a harmonic rejection mixer [24] or a time-invariant wideband low-pass post-filtering. The phase noise of the clock signals can increase the NF of the filter because of the reciprocal mixing of out-of-band interferers to the pass-band of the filter [19].

³The mutual loading effect of each path on the other one can be distinguished in the simulation by driving each path with a separate input voltage source.

⁴The noise contribution of the G_m cells is not taken into account.

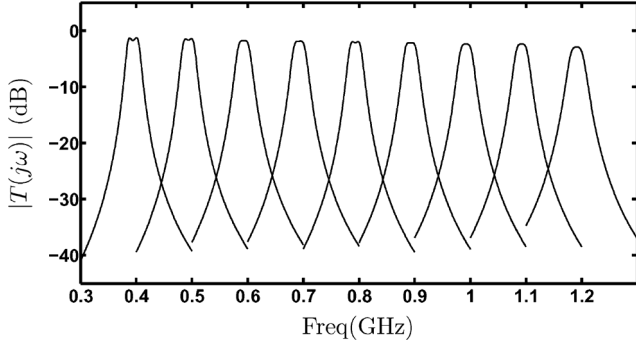


Fig. 14. SpectreRF simulation of 4th order switched G_m -C BPF with bandwidth of 20 MHz and ripple < 0.6 dB ($a = 0.76$, $b = 0.26$) from 0.4 GHz to 1.2 GHz; $R_s = 50 \Omega$, $R_{sw} = 10 \Omega$, $C_{BB} = 20$ pF, $G_m = 0.5$ mS and $C_s = 1$ pF and 1.7 pF.

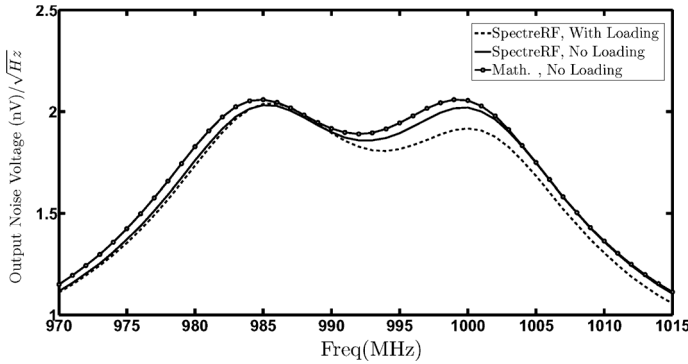


Fig. 15. Comparing SpectreRF simulation of the output noise voltage of the filter shown in Fig. 11 with and without taking into account the mutual loading effect of each path on the other one with its mathematical derivation excluding the noise contribution of the G_m cells (24).

C. NF of the Implemented Filter

The output voltage noise of the filter illustrated in Fig. 11 excluding the noise contribution of the G_m cells is found in (24). In Fig. 15, A comparison between the SpectreRF simulation and the mathematically derived equation has been made. As can be seen, the SpectreRF simulation and the derived equation closely match and not taking into account the mutual loading effect of each path on the other path introduces less than 5% error. The NF of the filter, not taking into account the noise contribution of the G_m cells, is 5.6 dB.

To take into account the noise contribution of the differential G_m cells, first the transfer function of the equivalent baseband current noises in each path (I_{n1} , I_{n2}) to the output of each path should be found (using the circuit shown in Fig. 16). Because of the limited bandwidth of the baseband nodes, only the low frequency contents of the baseband current noises are taken into account. A comparison between SpectreRF simulation and the derived equations (see (27) and (28)) for $V_{out1,2}(s + j\omega_{lo})/I_{n1,2}(s)$ of the filter has been made in Fig. 16(c).

Consequently, the total NF of the filter will be (10) where F_1 (see (29)) is the noise figure of the filter without considering the noise contribution of the G_m cells and NEF_2 (see (30)) is the noise excess factor due to the differential G_m cells in both paths.

$$F = F_1 + NEF_2 \quad (10)$$

The equivalent output current noise of the differential G_m cells (Fig. 18(a)) can be estimated by $I_{nb}^2 \cong g_m^2/4 \times (8kT/g_m + 8kT/(R_p g_m^2))$ where R_p is the degeneration resistance of the PMOS transistor in Fig. 18(a). The $1/f$ noise contribution of the G_m cells is heavily reduced by exploiting large transistors being heavily degenerated, which is possible thanks to using a high supply voltage for the baseband circuit since speed is not an issue here. A comparison between SpectreRF simulation of the total NF of the filter and its mathematical derivation (10) is illustrated in Fig. 17. The calculated and simulated NF of the implemented filter are 9.6 dB and 9.8 dB, respectively.

Most of the noise comes from the G_m cells and the source impedance transformation due to C_s . Increasing the value of C_s lowers the impedance transformation ratio but on the other hand it increases the loading effect of each path on the other one which leads to increase in the loss of the filter. Moreover, it leads to more area consumption (due to the baseband capacitors) and bigger G_m values which indeed increases the noise contribution of the G_m cells. Simulation shows the optimum range for the series capacitor is $1 \text{ pF} \leq C_s \leq 2 \text{ pF}$. Further increase in C_s leads to excessive loss due to more interaction between the two paths and in contrast reducing the series capacitor increases the NF of the filter considerably. Exploiting $C_s = 2$ pF leads to NF of 8.6 dB and -3.8 dB voltage gain while using $C_s = 1$ pF (our case), leads to NF of 9.8 dB and voltage gain of -2.2 dB. C_s of 1 pF is chosen over 2 pF because of less reduction in the voltage gain of the filter and 50% reduction in the area of the baseband capacitors.

V. REALIZATION

The filter was realized in 65 nm CMOS LP technology. The schematic of the proposed filter is illustrated in Fig. 18(b). A modulo-4 ring counter has been used to obtain 4 non-overlapping clock signals with 25% duty cycle. The simplified block diagram of the quadrature clock generator with low phase error [24] is shown in Fig. 19. A master clock (CLK) at 4 times the switching frequency is applied externally. A D flip-flop based divider divides the input clock by four and produces 4 clock signals with 25% duty cycle. Due to its lower power consumption and higher speed, D flip-flops based on transmission gates have been exploited [24].

Every switch in the filter, which is realized by NMOS transistor, has been sized ($W/L = 50 \mu\text{m}/60 \text{ nm}$) to obtain an on resistance of 10Ω . Although the ultimate rejection of the filter is relatively independent from the choice of switch resistances, low switch resistances are chosen to reduce their noise and nonlinearity contributions and the mismatch between them. Nevertheless, increasing the size of switches will introduce more parasitic capacitance to the input and output port of the filter which reduces the voltage gain of the filter. In our case, parasitic capacitances introduced 2 dB reduction in the voltage gain of the filter. Moreover, utilization of larger switch transistors increases the dynamic power consumption and the LO leakage to the input port of the filter. Because the drain and source of each switch have a DC bias of 0.8 V, for proper operation (high linearity and low on resistance) of the switches, the low and high levels of the clock signals should be raised by

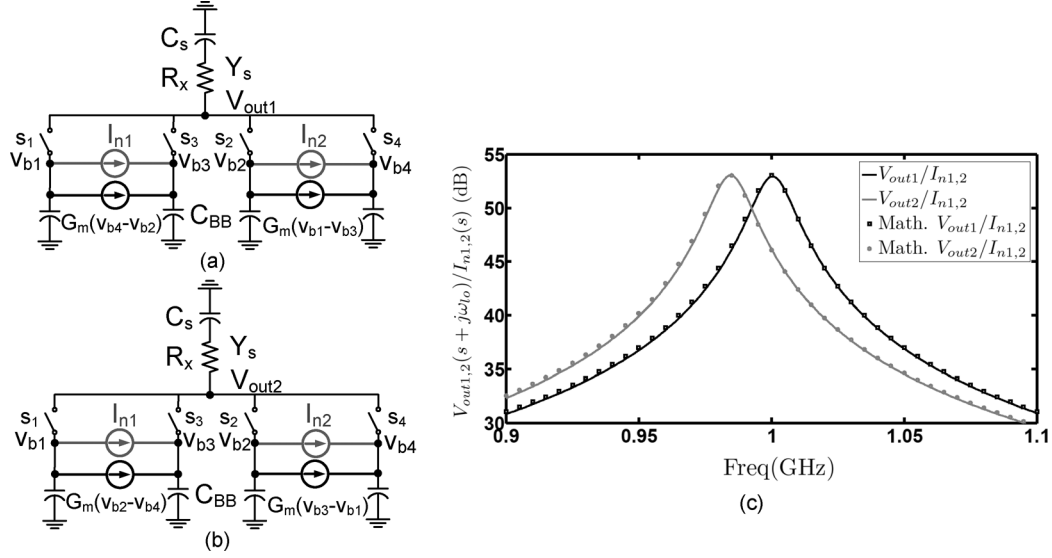


Fig. 16. Circuits used to derive the transimpedance gain from $I_{n1,2}(s)$ to $V_{out1,2}(s + j\omega_{lo})$ for each path of the filter shown in Fig. 11 and (c) Comparing the SpectreRF simulation of the transimpedance gain of $V_{out1}/I_{n1,2}$ and $V_{out2}/I_{n1,2}$ with their mathematical derivations (see (27) and (28)), $R_s = 50 \Omega$, $R_{sw} = 10 \Omega$, $C_{BB} = 20$ pF, $C_s = 1$ pF, $G_m = 0.5$ mS and $f_{lo} = 1$ GHz.

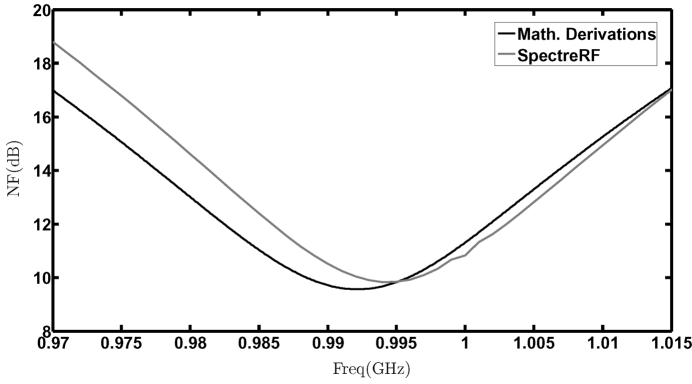


Fig. 17. Comparing the SpectreRF simulation of the NF of the filter and its mathematical derivation (10) assuming a 1 dB voltage loss due to the mutual loading effect of each path one the other one.

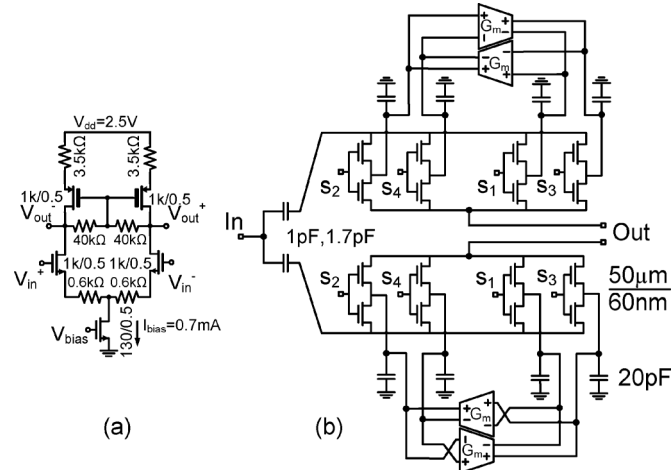


Fig. 18. (a) Implementation of the differential G_m cells and (b) Schematic of the proposed filter.

0.8 V. Simply, the clock signals are ac coupled to the gate of each switch which has a high ohmic resistor to a bias voltage of 1.1 V. The ac-coupling capacitors (MIM capacitors with

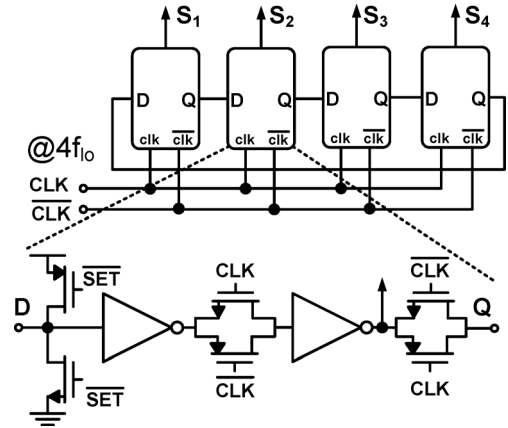


Fig. 19. A 4-phase non-overlapping clock generator with low phase mismatch (one D flip-flop shown in transistor level).

$C = 2$ pF) have been sized big enough to minimize the voltage loss due to the capacitive division between the ac-coupling capacitor and gate capacitance of the switches. The overlap between the adjacent clock signals reduces the voltage gain, quality factor and deteriorates the linearity of the filter. The PMOS transistors of inverters in Fig. 19 have been weakened compared to NMOS transistors to produce non-overlapping clocks (the crossing point of adjacent clocks has been lowered from $V_{DD}/2$ to lower than the threshold voltage of switching transistors.). The transfer function of the filter for adjacent clocks having cross-points of $V_{DD}/2$ and cross-points lower than $V_{th,n}$ are compared in Fig. 21. As can be seen, the overlap between the adjacent clocks introduces about 1 dB reduction in the pass-band gain of the filter. Moreover, overlapping between the adjacent clock signals increases the noise figure by 0.6 dB.

The buffers that drive the switches have been sized to achieve rise and fall time of less than 30 ps. The implementation of the differential G_m cells is depicted in Fig. 18(a) which draws 0.7 mA from 2.5 V. Due to the parasitic capacitance of the switches at input RF node which effectively increases the

series capacitance, the value of the G_m changed from 0.5 mS to 0.7 mS (G_m cells are slightly tunable). The length of each transistor is chosen to be $0.5 \mu\text{m}$ to reduce the $1/f$ noise contribution and increase the output impedance. Resistive degeneration has been used to linearize the G_m and lower the $1/f$ noise contribution further. The bias voltage of the input and output of the differential G_m are equal and chosen to be 0.8 V. To obtain a bandwidth of 20 MHz, the baseband capacitors C_{BB} are 20 pF and made from accumulation-mode N-type MOS capacitors which are the densest on-chip capacitors. When they are biased ($V_{GS} > 0$), they are reasonably linear [25]. In our case, each baseband capacitor is biased at 0.8 V. In presence of mismatch among the baseband capacitors and G_m cells of the BPF, any RF input at $f_{lo} + f_m$ can be folded on top of the desired channel as a component at $f_{lo} - f_m$ [26]. The folding is proportional to $(\Delta G_m) / (G_m \sqrt{1 + (\omega_m / \omega_{BB})^2}) + (\Delta C_{BB}) / (C_{BB} \sqrt{1 + (\omega_{BB} / \omega_m)^2})$. The large area of C_{BB} and G_m cells greatly reduces the mismatch between them. Therefore the phase mismatch between the clocks is the dominant factor in reducing the image rejection [21]. Monte-Carlo Simulations show that the folding is < -52 dB for $f_{lo} = 1$ GHz and $f_m = 2$ MHz. Each series capacitor which has two modes is made of two parallel MIM capacitors of 1 pF and 0.7 pF. The selection of the series capacitor value is in this way: for $f_{in} = 0.7$ –1.2 GHz, C_s is 1 pF and for $f_{in} = 0.4$ –0.7 GHz C_s is 1 pF + 0.7 pF = 1.7 pF. The measurement interface has been illustrated in Fig. 20. For NF, filter shape and out-of-band linearity measurements, two buffer stages have been added after the filter (port I). Moreover, to measure the in-band IIP₃ of the filter while not being affected by the non-linearities in the buffers, a simple resistive divider has been used (port II). An ac-coupled differential amplifier is used to perform the subtraction and two push-pull stages are exploited for matching purposes. In the differential amplifier, the gates of the PMOS transistors are connected via a resistor R_{b2} to ground to increase the voltage headroom of the input transistors. In this way, the DC bias of the output voltage of the differential amplifier will be $(1 + R_{b1} / (2R_{b2})) \times (V_{DD} - V_{SGP})$. To maintain the bandwidth and filter shape of the filter over process corners, the value of G_m and C_{BB} should be programmable. Because the center frequency of the filter is set by an external clock frequency, the center frequency of the filter does not change. This is in contrast to g_m -C filters [7] where a separate PLL is needed to correct the center frequency of the filter over process corners.

VI. MEASUREMENTS

The chip micrograph of the proposed filter is illustrated in Fig. 22. The chip has been fabricated in CMOS LP 65 nm technology and the active area of the filter is 0.127 mm^2 . The chip is mounted in a QFN24 package and tested on a printed circuit board. The measured transfer function of the filter is compared with the SpectreRF simulation of the proposed filter and a conventional 4-path filter in Fig. 23 (with the same baseband capacitor $C_{BB} = 20$ pF). As can be seen, the ultimate rejection and order of filter have been improved compared to conventional 4-path filters [20]. The tunability of the filter from 0.4 GHz to 1.2 GHz has been measured and illustrated in Fig. 24.

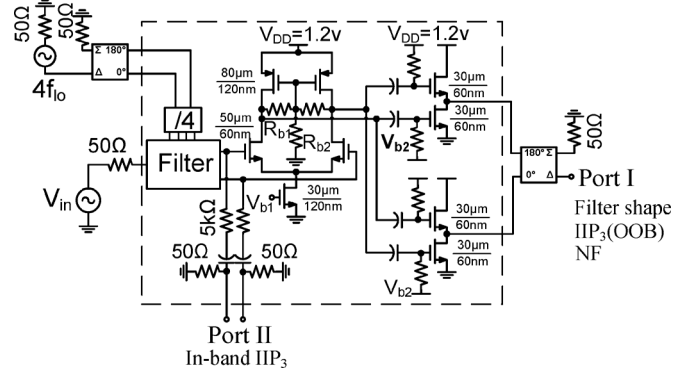


Fig. 20. Measurement interface.

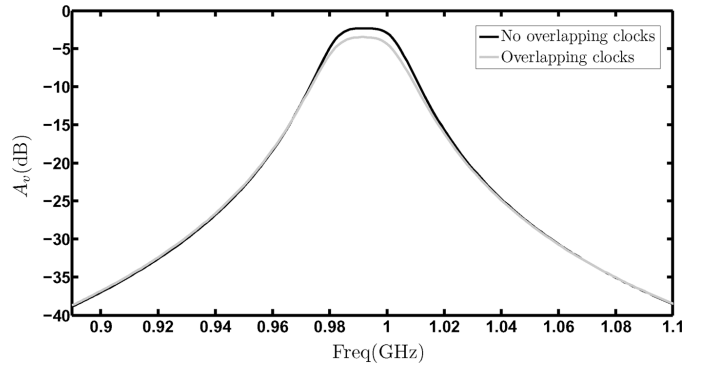


Fig. 21. The SpectreRF simulation of the transfer function of the filter with and without reducing the cross-points of the adjacent clocks from $V_{DD}/2$ to lower than $V_{th,n}$.

The measured results are in agreement with the simulation results shown in Fig. 14 within 0.3 dB. The maximum pass-band ripple is around 0.4 dB. Although the BPFs at second harmonics of f_{lo} have been suppressed due to subtraction, the BPFs at odd harmonics of the f_{lo} still exist. The voltage gain of the filter at $k f_{lo}$ ($k = 3, 5, \dots$) is $1/k^2$ times lower than the voltage gain of the filter at f_{lo} . As can be seen in Fig. 23, there is almost 20 dB gain difference between the gain of filter at f_{lo} and $3f_{lo}$. If more filtering is needed, an LTI low-pass filter or harmonic rejection mixer [24] can be utilized. A closer view of the filter shape measurements is illustrated in Fig. 25. Because of the constant bandwidth nature of the N-path filters, the quality factor of the filter reduces as the center frequency of the filter reduces. In our case, the quality factor Q changes from 60 for $f_c = 1.2$ GHz to 20 for $f_c = 0.4$ GHz. In N-path filters, there is a direct trade-off between area (which is consumed by baseband capacitors) and quality factor. Furthermore, the quality factor can be enhanced by increasing the source resistance. The transfer function of 10 samples has been measured to demonstrate the consistency of the filter against mismatch. These measurements are shown in Fig. 26. As can be seen, the filter shape is quite robust to the mismatch. The ultimate rejection of the filter is approximately 58 dB which is probably limited by the direct coupling between the input and output bond wires. The measured in-band IIP₃ of the filter is +9 dBm which has been measured at port II in Fig. 20 while the simulated in-band IIP₃ is +11 dBm. It is found in simulation that reducing the overlap between the adjacent clock signals (Lowering the cross-point of adjacent clocks to lower than the threshold voltage of switching transistors), increases the IIP₃.

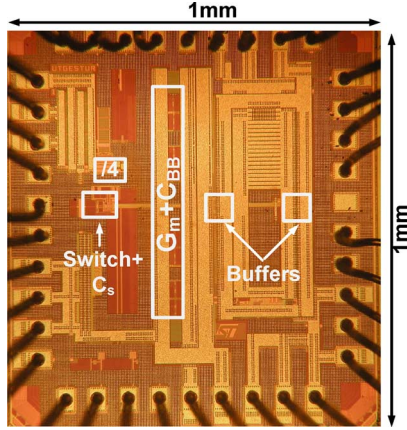


Fig. 22. 65 nm CMOS chip micrograph indicating functional blocks.

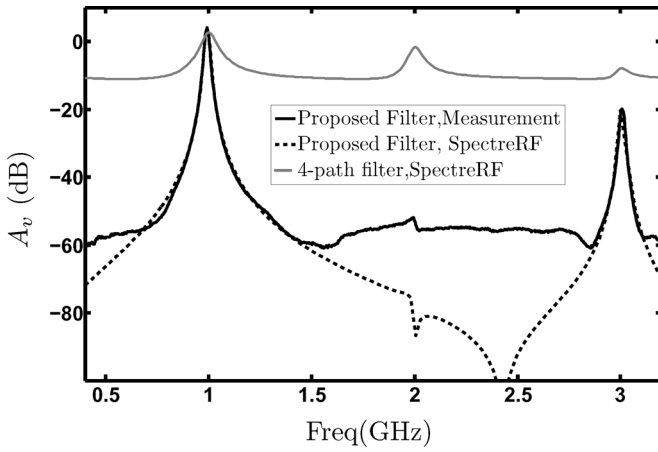


Fig. 23. Comparing the measured filter shape at 1 GHz with the SpectreRF simulation of the proposed filter and conventional 4-path filter (The gain of the buffers is estimated from the SpectreRF simulation and has been de-embedded from the measurement.).

of the filter by 1.8 dBm. Because of the high linearity of the switches and baseband capacitors, the linearity of the filter is mainly limited to G_m cells. The measured out-of-band IIP₃ for an offset frequency of $\Delta f = +50$ MHz is +29 dBm which was measured at port I in Fig. 20. Due to the large amount of filtering before the buffers, the nonlinearity of the buffers is not important in the measurement of out-of-band IIP₃. Another measurement has been performed to check the persistency of the filter shape and its ultimate rejection when a large out-of-band interferer exists very near to the pass-band of the filter. The measured transfer function of the filter with and without a +2 dBm continuous wave blocker which is located at +50 MHz and +30 MHz offset from the center frequency of the filter has been measured and compared in Fig. 27 and as can be seen, the filter is quite robust to the large out-of-band interferers. A +2 dBm blocker located at +30 MHz offset from the center frequency of the filter reduces the pass-band gain by 1.5 dB (At port II in Fig. 20).

The LO leakage power to the input port of the filter is < -60 dBm which is mainly caused by the capacitive mismatch in the switches. The measured NF of the filter is 10 dB (The noise of buffers is calculated from simulation and de-embedded from the measurement.) which is in agreement with the theory and simulation (Fig. 17). Most of the noise comes from G_m

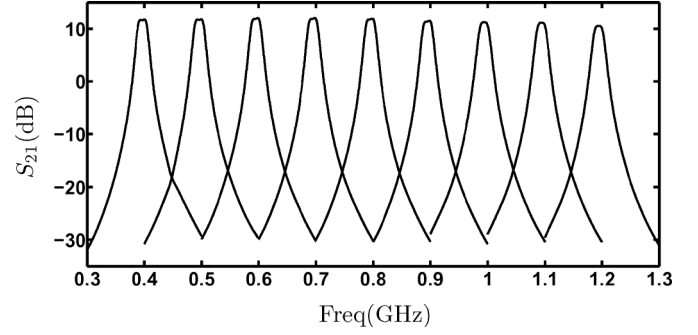


Fig. 24. Measured transfer function of the filter from 0.4 GHz to 1.2 GHz.

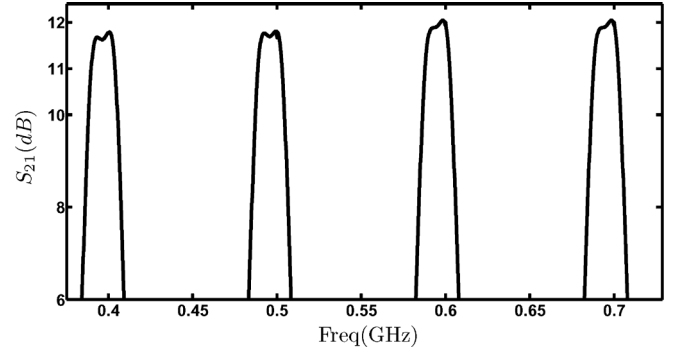


Fig. 25. Measured pass-band shape of the filter.

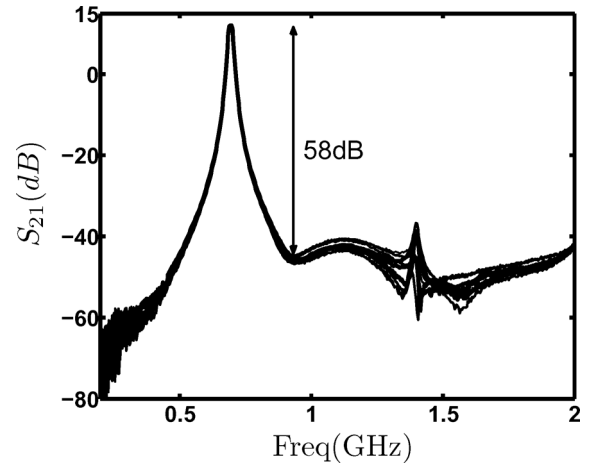


Fig. 26. Measurements of transfer function of 10 samples to demonstrate the consistency of the filter against mismatch.

TABLE I
COMPARISON BETWEEN MEASUREMENT AND SIMULATION RESULTS

	Meas.	Sim.
BW(MHz)	21	21
Ult. Rej. (dB)	>55	>70
IIP ₃ (in-band)(dBm)	>+9	>+10.6
IIP ₃ (OOB)(dBm)	+29	+32
NF(dB)	9.7-10.5	9.6-10.3
Max. Ripple(dB)	<0.4	<0.6
Voltage gain(dB)	-2,-3.2	-1.7,-2.7

cells and the impedance transformation of the source resistance due to the series capacitors C_s . A comparison between simulation and measurement has been done in Table I. Furthermore,

TABLE II
COMPARISON TABLE

	Mirzae JSSC'11[13]	Andrews JSSC'10[14]	Ghaffari RFIC'10[20]	Thai JSSC'10[15]	Soorapanth JSSC'02[3]	Razafimandimby ESSCIRC'06[2]	Oualkadi RFIC'07[17]	This work
Type	Receiver	Receiver	Filter	Filter	Filter	Filter	Filter	Filter
Technology ^a	65nm	65nm	65nm	65nm	250nm	SiGe: BiCMOS250nm +piezoelectric	350nm	65nm
Center Frequency(GHz)	2.14	0.05-2.4	0.1-1	0.08	2.14	2.14	0.24-0.53	0.4-1.2
Order of filter	6	2	2	4	6	4	2	4
BW(MHz)	4	20	35	10	60	60	2-5	21
Ultimate Rejection (dB)	48 ^d	13 ^h	16 ^c	32	?	28	24	55
IIP ₃ (in-band)(dBm)	-8.5	-67	+19	-2	-4.9	+35	<-40	+9
IIP ₃ (out-of-band)(dBm)	-6.3 ^k	+25	?	?	?	?	?	+29 ⁱ
NF(dB)	5.3 ^e	5.5	5.5	21.5	19	9 ^f	9	10 ^a
Active Area(mm ²)	0.76	2.5	0.07	0.25	3.51	6.65	1.93	0.127
Max. Ripple(dB)	N.A	N.A	N.A	0.1	0.7	1.5	N.A	0.4
Power Consumption(mW)	34.2	60	18	13.2	17.5	7	63	21.4 ^b

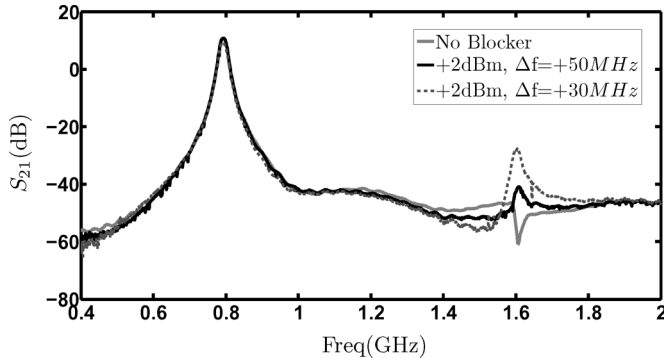
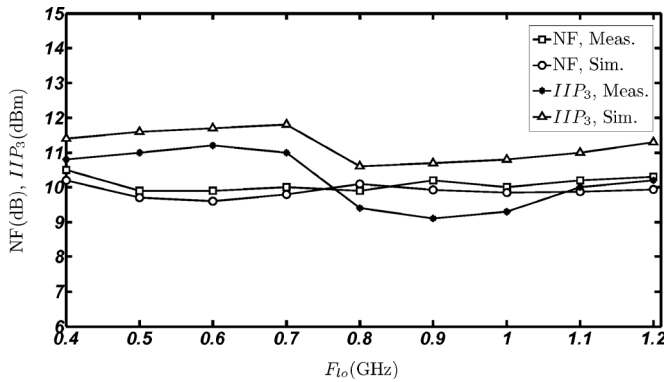
^a Buffers noise contribution is de-embedded($V_{in,n,rms}=2.66nV/\sqrt{Hz}$).^b 2.8 mA static and 12 mA dynamic current consumption @ 1GHz ^c $R_{sw}=5\Omega$ ^d It is achieved by cascading 3 BPF, of which most filtering is done in IF.^e 10dB on-chip passive gain in Front^f Estimated from the loss of filter

Fig. 27. The measured transfer function of the filter with and without +2 dBm continuous wave blocker which is located +50 MHz and +30 MHz offset far from the center frequency of the filter.

Fig. 28. The measured and simulated IIP₃ and NF of the proposed filter over the whole band.

a comparison between measurements and simulation results of NF and IIP₃ over the whole band has been done in Fig. 28.

N-path filters for good linearity and low noise figure need clock signals with low rise and fall time to drive large switches which indeed raises the dynamic power consumption of the filter. The static power consumption is 7 mW over the tuning band and the dynamic power consumption varies from 5.8 mW to 14.4 mW. The filter is compared with [2], [3], [13]–[15], [17], [20] in Table II. We even added filtering-receivers [13], [14]

in the comparison table. Our filter outperforms Q-enhancement [3] and g_m -C [15] filters from a linearity, noise and tunability point of view. According to [5], the DR of g_m -C filters depends on $1/Q^2$ while the dynamic range of Q-enhancement filters depends on Q_0^2/Q^2 where Q_0 is the quality factor of on-chip inductors. g_m -C filters need extra circuitry (gyrators) to synthesize inductors and Q-enhancement filters require extra circuitry (a negative impedance) to enhance the Q of on-chip inductors and these extra circuitries lead to a lower DR. However in the N-path technique, the required Q of the filter can be obtained by increasing C_{BB} ($Q \propto C_{BB}R_x$) and no extra active devices is needed. Therefore the Q of the N-path filter is decoupled from its DR. The DR [5] of the proposed filter is 95 dB in 1 MHz bandwidth. According to the FOM defined in [5], the FOM of our filter is 146.4 dB-Hz/mW at $f_c = 1$ GHz and 148.5 dB-Hz/mW at $f_c = 0.4$ GHz which is higher than the FOM of the Q-enhancement filters [3] (129.2 dB-Hz/mW) and [4] (125.6 dB-Hz/mW). Compared to [14], [20], it has better pass-band shape and much higher rejection at RF frequencies. Moreover, this work has comparable out-of-band rejection and better pass band shape compared to [13]. The proposed filter is a good candidate for substituting the SAW filters used in IF section of a Super-Heterodyne receiver where the IF frequency can be adapted to actual interference conditions.

VII. CONCLUSION

A 4th order switched g_m -C BPF technique is proposed to improve the filter shape and ultimate rejection of 4-path passive mixer filters. The technique exploits subtraction of output voltages of the two 2nd order 4-path band-pass filters with shifted center frequency. The frequency shift of the 4-path BPF is realized by coupling the baseband capacitor voltages via two differential transconductors, in either a clockwise or counter clockwise fashion. Capacitive splitting of the input signal is used to reduce mutual loading of the two 4-path BPFs and increase their quality factors. The center frequency of the filter is tunable from 0.4 GHz to 1.2 GHz with a bandwidth of around 21 MHz. The ultimate rejection of the filter is >55 dB and the in-band and

out-of-band ($\Delta f = +50$ MHz) IIP₃ of the filter are +9 dBm and +29 dBm, respectively. The NF of the filter is 10 dB. The filter NF is similar to a typical mixer NF and therefore it is not suitable for antenna filter applications. Typically in fully integrated receivers, filtering is needed at different places along the receiver chain where our proposed filter can perform some of the required filtering, especially where tunability and integration are important. This filter is a good candidate for substituting the SAW filters used in IF section of a Super-Heterodyne receiver where the IF frequency can be adapted to actual interference conditions. Moreover, because the impedance level of an IF section is typically much higher than 50 Ω , the quality factor of the filter can be increased considerably compared to the case where R_s is 50 Ω . The power consumption of the filter varies from 12.8 mW to 21.4 mW over the tuning frequency range. The filter has been fabricated in CMOS LP 65 nm technology and the active area is 0.127 mm².

APPENDIX

Firstly, the transfer function of an N-path filter with a generic source admittance and a generic but with limited bandwidth baseband admittance will be calculated. This formulas are used in the body of the paper to analyze the effect of the added g_m cells on a conventional 4-path filter. Moreover based on these calculations, the effects of the addition of a series capacitor to the source resistance of a conventional 4-path filter on its transfer function and NF will be analyzed. Finally, the NF of the final filter shown in Fig. 11 will be calculated.

AN N-PATH FILTER WITH GENERIC SOURCE AND BASEBAND IMPEDANCES

With a derivation analogous to [8], [18] and by assuming that: 1) N is the number of phases and the duty cycle of the clock signals $s_i(t)$ ($i = 1 - N$) is $1/N$, 2) ω_{lo} is the switching frequency, 3) $Y_s = Y'_s/(R_{sw}Y'_s + 1)$, 4) if there is an interaction between the baseband nodes (like the g_m s in our case), the effective baseband admittance $Y_{BB}(s, k)$ will be different for f_{in} around $k f_{lo}$ $k \in Z$, 5) to take into account the effect of the harmonics of f_{lo} , we define an effective source admittance⁵ $Y_{s,eff,k}(s)$ for f_{in} around $k f_{lo}$, $k \in Z$, 6) $a_m = e^{-j\pi m/N}/N \times \text{sinc}(\pi m/N)$ is the Fourier coefficient of $s_1(t)$, and 7) each switch is modeled with an ideal switch in series with switch resistance R_{sw} and parasitic capacitance of the switches is not taken into account, the total transfer function of an N-path filter with a generic source admittance and a generic but with limited bandwidth baseband admittance (Fig. 29) can be written in the form of:

$$\begin{aligned} V_x(s) &= \sum_{l=-\infty}^{+\infty} H_l(s) \times V_{in}(s - j l N \omega_{lo}) \\ H_l(s) &= \sum_{m=-\infty}^{+\infty} N^2 a_m a_{lN-m} Z_x(s - j m \omega_{lo}, k) \\ &\quad \times Y_s(s - j l N \omega_{lo}) \end{aligned} \quad (11)$$

⁵In the case of $Y'_s = 1/R_s$, the effective source admittance will be $1/(R_s + R_{sw})$.

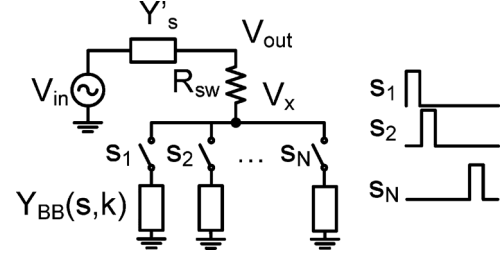


Fig. 29. N-path Filter with generic source admittance and generic but limited bandwidth baseband admittance exploiting non-overlapping clock signals.

where l is a folding back index term and $Z_x(s, k)$ is described by:

$$\begin{aligned} Z_x(s, k) &= \frac{1}{N Y_{BB}(s, k) + Y_{s,eff,k}(s)} \\ Y_{s,eff,k}(s) &= \sum_{m=-\infty}^{+\infty} N^2 |a_{Nm-k}|^2 Y_s(s - j \omega_{lo}(Nm - k)) \end{aligned} \quad (12)$$

To find the transfer function of the filter with no net frequency translation, the l in (11) should be zero. Consequently, $V_x(s)/V_{in}(s)$ will be:

$$\begin{aligned} T(s) &= \frac{V_x(s)}{V_{in}(s)} = Y_s(s) \\ &\quad \times \sum_{m=-\infty}^{+\infty} \text{sinc}^2(\pi m/N) Z_x(s - j m \omega_{lo}, m) \end{aligned} \quad (13)$$

$V_{out}(s)/V_{in}(s)$ can be found using superposition and substitution theorems and it will be $V_{out}(s)/V_{in}(s) = (T(s) + R_{sw}Y'_s(s))/(R_{sw}Y'_s(s) + 1)$. Furthermore, (11) can be exploited to find the folding back components from $\omega_{in} = (1 - mN)\omega_{lo} + \Delta\omega$ to $\omega_{out} = \omega_{lo} + \Delta\omega$, $m \in Z$ (14).

$$\begin{aligned} A_{fold}|_{\omega_{lo} + \Delta\omega} &= \text{sinc}^2(\pi/N) \times \frac{1}{mN - 1} \times Z_x(\Delta\omega, 1 - mN) \\ &\quad \times Y_s((1 - mN)\omega_{lo} + \Delta\omega) \end{aligned} \quad (14)$$

In the case of a resistive source admittance $Y'_s = 1/R_s$, the effective admittance of $Y_{s,eff,k}$ is simplified to $1/(R_s + R_{sw})$. Therefore, (13) will be simplified to (15).

$$T(s) = \frac{V_x(s)}{V_{in}(s)} = \sum_{k=-\infty}^{+\infty} \text{sinc}^2\left(\frac{k\pi}{N}\right) \times G(s - j k \omega_{lo}, k) \quad (15)$$

where $G(s, k)$ is a LPF due to the combination of a baseband admittance $Y_{BB}(s, k)$ and a source resistance and described in (16).⁶

$$G(s, k) = \frac{1}{(R_s + R_{sw})N Y_{BB}(s, k) + 1}, \quad f_{in} \text{ around } k f_{lo}, k \in Z \quad (16)$$

⁶Because each baseband admittance sees $R_s + R_{sw}$ for $1/N$ th of the clock period, the effective resistance that each baseband admittance sees is $N(R_s + R_{sw})$.

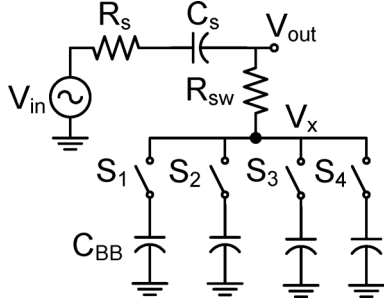


Fig. 30. Addition of a series capacitor C_s to the source resistance R_s of a conventional 4-path filter.

ADDITION OF A SERIES CAPACITOR TO THE SOURCE IMPEDANCE OF A CONVENTIONAL 4-PATH FILTER

Now based on (12)–(14), the effects of a series capacitor with the source resistance (Fig. 30) on the transfer function of a 4-path filter can be investigated. In our case, $N = 4$ and $Y_s(s) = 1/R_x \times \tau_s s / (1 + \tau_s s)$ where $\tau_s = R_x \times C_s$ and $R_x = R_s + R_{sw}$. By using (13), the transfer function of the filter around f_{lo} can be found. Due to the limited bandwidth of the baseband admittances, only the two terms ($m = 1, -1$) of (13) are of interest.

$$T(s) = \frac{V_x}{V_{in}} = \frac{8}{\pi^2 R_x} \times \frac{\tau_s s}{1 + \tau_s s} \times (Z_x(s - j\omega_{lo}, 1) + Z_x(s + j\omega_{lo}, -1)) \quad (17)$$

$Z_x(s, \pm 1)$ is found using (12).

$$Z_x(s, \pm 1) = \frac{1}{4C_{BB}s + j\text{Imag}(Y_{s,\text{eff},\pm 1}) + \text{Real}(Y_{s,\text{eff},\pm 1})} \quad (18)$$

From (12), the effective source admittance $Y_{s,\text{eff},1}$ for input frequencies around f_{lo} by assuming that $|\omega| \ll |(4m - 1)\omega_{lo}|$ ($m \in Z$) can be found.

$$\begin{aligned} Y_{s,\text{eff},1} &\cong \sum_{m=-\infty}^{+\infty} 16|a_{4m-1}|^2 Y_s(-j\omega_{lo}(4m - 1)) \\ &\cong \frac{8}{\pi^2 R_x} \times \sum_{m=-\infty}^{+\infty} \frac{1}{(4m - 1)^2} \times \frac{-j\tau_s \omega_{lo}(4m - 1)}{1 - j\tau_s \omega_{lo}(4m - 1)} \end{aligned} \quad (19)$$

It can be proven that $\text{Imag}(Y_{s,\text{eff},-1}) = -\text{Imag}(Y_{s,\text{eff},1})$ and $\text{Real}(Y_{s,\text{eff},-1}) = \text{Real}(Y_{s,\text{eff},1})$. The real and imaginary parts of $Y_{s,\text{eff},1}$ in terms of R_x and $\tau_s \omega_{lo}$ have been illustrated in Fig. 31. Interestingly as can be seen from Fig. 31, for $\tau_s \omega_{lo} < 0.5$, both real and imaginary parts of the $Y_{s,\text{eff},1}$ can be well estimated by $2\tau_s \omega_{lo} / (\pi R_x)$. Therefore by utilizing the mentioned approximation, (17) can be changed to:

$$\begin{aligned} T(s) &\cong \frac{V_x}{V_{in}} = \frac{8}{\pi^2} \times \frac{\tau_s s}{1 + \tau_s s} \\ &\times \frac{s / (2R_x C_{BB})}{s^2 + (C_s \omega_{lo} / (\pi C_{BB}))s + \omega_{lo}^2 \times (1 - C_s / (\pi C_{BB}))} \end{aligned} \quad (20)$$

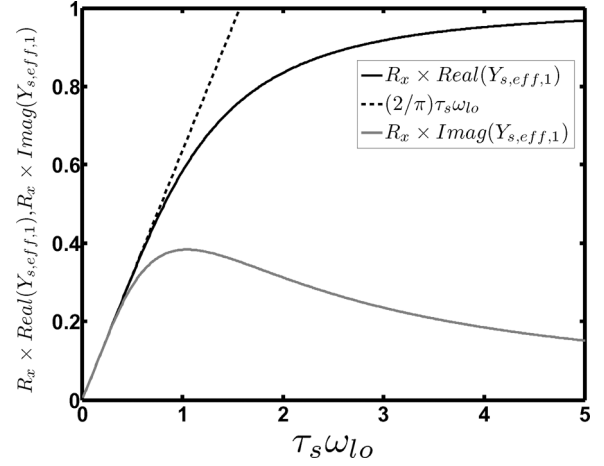


Fig. 31. $R_x \times \text{Imag}(Y_{s,\text{eff},1})$, $R_x \times \text{Real}(Y_{s,\text{eff},1})$ and their approximation as a function of $\tau_s \omega_{lo}$.

Now, the effect of a series capacitor with source resistance on the noise figure of a conventional 4-path filter will be investigated. By using (14), the output noise voltage at node V_x can be found.

$$\begin{aligned} |V_{x,n}|_{\omega_{lo} + \Delta\omega}^2 &= 4kTR_x \sum_{m=-\infty}^{+\infty} A_{\text{fold}}^2 = 4kTR_x \times \frac{64(\tau_s \omega_{lo})^2}{R_x^2 \pi^4} \\ &\times \sum_{m=-\infty}^{+\infty} \frac{|Z_x(\Delta\omega, 1 - 4m)|^2}{1 + \tau_s^2 \omega_{lo}^2 (1 - 4m)^2} \end{aligned} \quad (21)$$

It can be proven that $Z_x(s, 1 - 4m) = Z_x(s, 1)$. (21) can be simplified for $\tau_s \omega_{lo} < 0.5$ using Fig. 31.

$$|V_{x,n}|_{\omega_{lo} + \Delta\omega}^2 \cong 4kT \times \frac{16\tau_s \omega_{lo}}{R_x \pi^3} \times |Z_x(\Delta\omega, 1)|^2 \quad (22)$$

By exploiting (17), the gain of the 4-path filter with a series capacitor around f_{lo} is $8/(\pi^2 R_x) \times j\tau_s \omega / (1 + j\tau_s \omega) \times Z_x(\Delta\omega, 1)$. Consequently, the NF at node V_x is described in (23).

$$\begin{aligned} F|_{\omega=\omega_{lo}+\Delta\omega} &\cong \left(1 + \frac{R_{sw}}{R_s}\right) \times \frac{\pi}{4} \\ &\times \left(\omega_{lo} \tau_s + \frac{1}{\tau_s \omega_{lo}} \times \left(\frac{\omega_{lo}}{\omega}\right)^2\right). \end{aligned} \quad (23)$$

NF CALCULATION OF THE IMPLEMENTED FILTER

In this section we develop the material needed to derive the NF of the resultant filter shown in Fig. 11. The total output noise voltage of the filter shown in Fig. 11 for $\omega_{lo} \tau_s < 0.5$ (excluding the noise contribution of the differential G_m cells and neglecting the mutual loading effect of each path on the other one) is found in a similar way as (21).

$$\begin{aligned} |V_{\text{out},n}|^2 &\cong 8kTR_{sw} + 4kT \times \frac{16C_s \omega_{lo}}{\pi^3} \\ &\times (|Z_{x,\text{path}1}(s, 1)|^2 + |Z_{x,\text{path}2}(s, 1)|^2) \end{aligned} \quad (24)$$

Where $Z_{x,path1}(s, 1)$ and $Z_{x,path2}(s, 1)$ are:

$$\begin{aligned} Z_{x,path1}(s, 1) &= \frac{1}{4C_{BB}(s - j\omega_{BB}) + \frac{2}{\pi}C_s\omega_{lo}(1 + j)} \\ Z_{x,path2}(s, 1) &= \frac{1}{4C_{BB}(s + j\omega_{BB}) + \frac{2}{\pi}C_s\omega_{lo}(1 + j)} \end{aligned} \quad (25)$$

and ω_{BB} is g_m/C_{BB} . Note that the first term in (24) is due to the noise contribution of the switch resistances of the second set of switches. In fact, the noise of the switch resistances of the second set of switches is not subject to folding back issues and only the noise contents around f_{lo} will deteriorate the NF. Now, we will investigate the noise contribution of the differential G_m cells. At first, the transimpedance of $V_{out1}(\omega_{lo} + \Delta\omega)/I_{n1,2}(\Delta\omega)$ shown in Fig. 16(a) will be found. Due to the differential G_m cells and the differential stimulation of the circuit (I_{n1} or I_{n2}), $V_{b1} = -V_{b3}$ and $V_{b2} = -V_{b4}$. By assuming that $I_{n2} = 0$ and writing the KCL at nodes V_{b1} and V_{b2} , V_{bi}/I_{ni} $i = 1, 2$ can be found by assuming that $\tau_s\omega_{lo} < 0.5$:

$$\begin{aligned} \frac{V_{b1}(s)}{I_{n1}(s)} &= \frac{C_{BB}s + \frac{1}{2\pi}C_s\omega_{lo}}{(C_{BB}s + \frac{1}{2\pi}C_s\omega_{lo})^2 + 4(G_m - \frac{1}{4\pi}C_s\omega_{lo})^2} \\ \frac{V_{b2}(s)}{V_{b1}(s)} &= \frac{-2(G_m - \frac{1}{4\pi}C_s\omega_{lo})}{C_{BB}s + \frac{1}{2\pi}C_s\omega_{lo}}. \end{aligned} \quad (26)$$

By exploiting $v_{out1} = v_{b1} \times (s_1(t) - s_3(t)) + v_{b2} \times (s_2(t) - s_4(t))$ and the fact that we are just interested in $V_{out1}(\omega_{lo} + \Delta\omega)$, $V_{out1}(\omega_{lo} + \Delta\omega)/I_{n1}(\Delta\omega)$ will be calculated.

$$\begin{aligned} \frac{V_{out1}(s + j\omega_{lo})}{I_{n1}(s)} &= 2a_1 \\ &\times \frac{C_{BB}s + 2jG_m + \frac{1}{2\pi}C_s\omega_{lo} \times (1 - j)}{(C_{BB}s + \frac{1}{2\pi}C_s\omega_{lo})^2 + 4(G_m - \frac{1}{4\pi}C_s\omega_{lo})^2} \end{aligned} \quad (27)$$

Interestingly, $V_{out1}(s + j\omega_{lo})/I_{n2}(s)$ will be

$$\frac{V_{out1}(s + j\omega_{lo})}{I_{n2}(s)} = -j \times \frac{V_{out1}(s + j\omega_{lo})}{I_{n1}(s)}. \quad (28)$$

To find the same transfer function for the filter shown in Fig. 16(b), it is just needed to change G_m to $-G_m$ in (27) and (28). Consequently, the total NF of the filter will be $F = F_1 + NEF_2$ where F_1 (29) is the noise figure of the filter without considering the noise contribution of the G_m cells and NEF_2 (30) is the noise excess factor due to the differential G_m cells in both paths.

$$\begin{aligned} F_1|_{\omega=\omega_{lo}+\Delta\omega} &= \frac{2R_{sw}}{R_s|T(j\omega)|^2} + \frac{16C_s\omega_{lo}}{R_s\pi^3|T(j\omega)|^2} \\ &\times (|Z_{x,path1}(\Delta\omega, 1)|^2 + |Z_{x,path2}(\Delta\omega, 1)|^2) \end{aligned} \quad (29)$$

$$\begin{aligned} NEF_2|_{\omega=\omega_{lo}+\Delta\omega} &= \frac{|I_{nb}|^2}{2kTR_s|T(j\omega)|^2} \\ &\times \left(\left| \frac{V_{out1}}{I_{nb}} \right|^2 + \left| \frac{V_{out2}}{I_{nb}} \right|^2 \right). \end{aligned} \quad (30)$$

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REFERENCES

- [1] D. Ruffieux, J. Chabloz, M. Contaldo, C. Muller, F. Pengg, P. Tortori, A. Vouilloz, P. Volet, and C. Enz, "A narrowband multi-channel 2.4 GHz MEMS-based transceiver," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 228–239, Jan. 2009.
- [2] S. Razafimandimby, C. Tilhac, A. Cathelin, A. Kaiser, and D. Belot, "An electronically tunable bandpass BAW-filter for a zero-IF WCDMA receiver," in *Proc. Eur. Solid-State Circuits Conf. (ESS-CIRC)*, Sep. 2006, pp. 142–145.
- [3] T. Soorapanth and S. Wong, "A 0-dB IL 2140±30 MHz bandpass filter utilizing Q-enhanced spiral inductors in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 579–586, May 2002.
- [4] J. Kulyk and J. Haslett, "A monolithic CMOS 2368±30 MHz transformer based Q-enhanced series-C coupled resonator bandpass filter," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 362–374, Feb. 2006.
- [5] W. Kuhn, D. Nobbe, D. Kelly, and A. Orsborn, "Dynamic range performance of on-chip RF bandpass filters," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 50, no. 10, pp. 685–694, Oct. 2003.
- [6] Y. Tividis, "Integrated continuous-time filter design—An overview," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 166–176, Mar. 1994.
- [7] H. Khorramabadi and P. Gray, "High-frequency CMOS continuous-time filters," *IEEE J. Solid-State Circuits*, vol. 19, no. 6, pp. 939–948, Dec. 1984.
- [8] L. Franks and I. Sandberg, "An alternative approach to the realizations of network functions: The N-path filters," *Bell Syst. Tech. J.*, pp. 1321–1350, Sep. 1960.
- [9] G. Temes and S. K. Mitra, *Modern Filter Theory and Design*. New York: Wiley, Nov. 1973.
- [10] D. von Grunigen, R. Sigg, J. Schmid, G. Moschytz, and H. Melchior, "An integrated CMOS switched-capacitor bandpass filter based on N-path and frequency-sampling principles," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 753–761, Dec. 1983.
- [11] J. Pandel, D. Bruckmann, A. Fettweis, B. Hosticka, U. Kleine, R. Schweer, and G. Zimmer, "Integrated 18th-order pseudo-N-path filter in VIS-SC technique," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 1, pp. 48–56, Feb. 1986.
- [12] P. V. A. Mohan and B. Ramachandran, *Switched Capacitor Filters: Theory, Analysis and Design*. New York: Prentice-Hall PTR, 1995.
- [13] A. Mirzaei, H. Darabi, and D. Murphy, "A low-power process-scalable super-heterodyne receiver with integrated high-Q filters," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2920–2932, Dec. 2011.
- [14] C. Andrews and A. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.
- [15] H. Le-Thai, H. H. Nguyen, H. N. Nguyen, H. S. Cho, J. S. Lee, and S. G. Lee, "An IF bandpass filter based on a low distortion transconductor," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2250–2261, Nov. 2010.
- [16] B. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.
- [17] A. El Oualkadi, M. El Kaamouchi, J. Paillot, D. Vanhoenacker-Janvier, and D. Flandre, "Fully integrated high-Q switched capacitor bandpass filter with center frequency and bandwidth tuning," in *IEEE RFIC Symp. Dig.*, 2007, pp. 681–684.
- [18] A. Mirzaei, H. Darabi, and D. Murphy, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 59, no. 1, pp. 52–65, Jan. 2012.
- [19] A. Mirzaei and H. Darabi, "Analysis of imperfections on performance of 4-phase passive-mixer-based high-Q bandpass filters in SAW-less receivers," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 58, no. 5, pp. 879–892, May 2011.
- [20] A. Ghaffari, E. Klumperink, and B. Nauta, "A differential 4-path highly linear widely tunable on-chip band-pass filter," in *IEEE RFIC Symp. Dig.*, May 2010, pp. 299–302.
- [21] A. Ghaffari, E. Klumperink, M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.

- [22] M. Darvishi, R. Van der Zee, E. Klumperink, and B. Nauta, "A 0.3-to-1.2 GHz tunable 4th-order switched g_m -C bandpass filter with >55 dB ultimate rejection and out-of-band IIP3 of 29 dBm," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2012, pp. 358–360.
- [23] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 2003.
- [24] Z. Ru, N. Moseley, E. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec. 2009.
- [25] C. Hung, Y. Ho, I. Wu, and K. O, "High-Q capacitors implemented in a CMOS process for low-power wireless applications," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 5, pp. 505–511, May 1998.
- [26] A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri, "A 65 nm CMOS Q-Band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, Apr. 2011.



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