A 0.13 μm 8 Mb Logic-Based Cu_XSi_YO ReRAM With Self-Adaptive Operation for Yield Enhancement and Power Reduction

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***Abstract*—A 0.13 μm 8 Mb Cu_xSi_yO resistive random access memory (ReRAM) test macro with $20F^2$ cell size is developed based on logic process for embedded applications. Smart and adaptive write and read assist circuits are proposed to fix yield and power consumption issues arising from large variations in set/reset time and high-temperature cell resistance. Self-adaptive write mode (SAWM) helps increase the R_{off}/R_{on} window from 8X to 24X at room temperature. The reset bit yield is improved from 61.5% to 100% and the high power consumption is eliminated after the cell switches to R_{on} during set. Self-adaptive read mode (SARM) increases read bit yield from 98% to 100% at 125°C. The typical access time of the on-pitch voltage sense amplifier (SA) is 21 ns. High bandwidth throughput is supported.**

***Index Terms*—On-pitch sense amplifier, ReRAM, self-adaptive read mode (SARM), self-adaptive write mode (SAWM).**

I. Introduction

RESISTIVE random access memory (ReRAM) is very attractive for dense storage in embedded applications because of its good scalability and complementary metal-oxide-semiconductor (CMOS) compatibility. There have been many published ReRAM materials and devices [1]–[5]. However, their performance was mainly based on a single cell or a small quantity of cells instead of large arrays.

Since 2004, several ReRAM test chips have come up gradually. Read and write circuits for cross-point array were proposed for high density application in [6]. A new bidirectional diode was implemented as the memory cell select element to suppress the leakage current in the multi-layered cross-point array for high density, with a number of circuit techniques to provide high write throughput [7]. Read and write circuits were addressed for high speed or high bandwidth in [8], [9]. A read reference produced by dummy array was employed to exclude the negative effect of tail bits in read yield [10]. A body-drain-driven current-mode sense amplifier was proposed to maintain adequate sense margins at low VDD such as 0.5 V [11]. Among the published literature, however, yield and power consumption issues resulting from large variations in set/reset time and high-temperature cell resistance have not been addressed yet.

The set power consumption and reset yield issues are described in Fig. 1. The previous set and reset algorithms are SVP (single voltage pulse) and RPS (ramped-pulse series, write-verify-write) respectively, which are the same with our previous work [12]. The measurement results show large set/reset time variations. To meet the set yield requirement and decrease the number of reset ramped pulses, the durations of set and reset pulses are usually longer than that required by the fast cells. Hence, high power consumption is generated because of high current flowing through the fast cells, which transition quickly to R_{on} during set. Moreover, the write disturbance can lead to reset failure because the fast cells may be set back to R_{on} again after the cell switches to R_{off} during reset. This can also result in wide R_{off} distribution and decrease the R_{off}/R_{on} window.

The ReRAM cell resistances have large variations at high temperature, particularly for R_{off} distribution, which extends to low resistance direction more critically than R_{on} does [5]. Degradation of the R_{off}/R_{on} window may lead to read failure at high temperature.

This paper introduces smart and adaptive write and read assist circuits to address the above-mentioned issues. Self-adaptive write mode (SAWM) can detect whether the cell resistance switches during set/reset and turn off the write stimulus instantly. Therefore, the duration of the large current after the fast cell switches to R_{on} during set is shortened and the power for set is saved. Additionally, the reset failure due to the write disturbance can also be avoided. Self-adaptive read mode (SARM) can generate a dynamic reference based on a dummy row of ReRAM cells to track the cell resistance variation under different process and temperature conditions. This can ensure the sense margin to be kept adequate even at high temperature, for example 125°C. On-pitch voltage sense amplifier (SA) with high area efficiency is employed to support SARM and high bandwidth throughput.

The rest of the paper is organized as follows: Section II discusses the write algorithm and the circuit implementation of SAWM. Section III describes SARM including dynamic reference generation and on-pitch voltage SA. Section IV presents silicon measurement results of the 8 Mb test chip. The final section concludes the paper.

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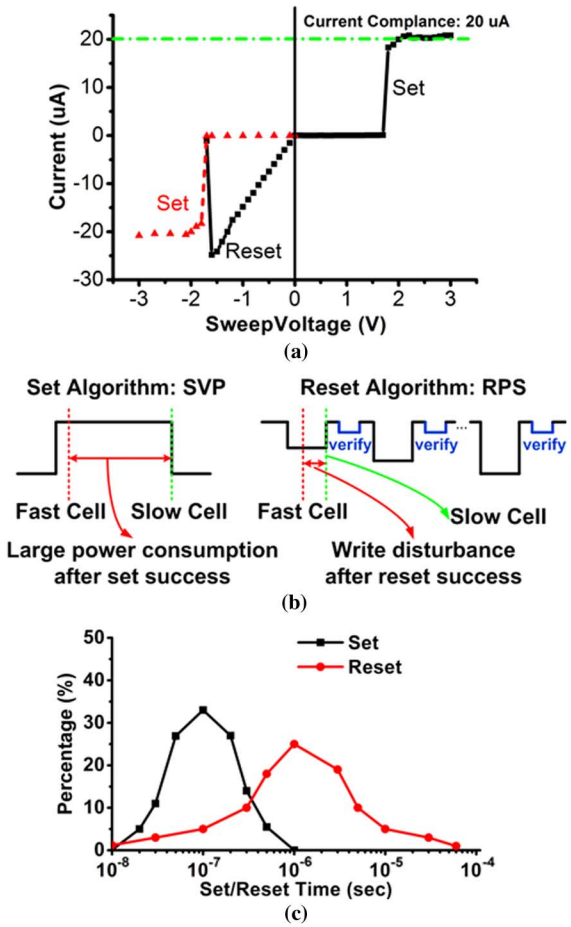


Fig. 1. (a) Cu_xSi_yO ReRAM I-V curve. Positive voltage can realize set, however, negative voltage can realize both set and reset. (b) SVP and RPS algorithms for set and reset respectively. (c) Set time based on SVP distributes from 10 to 100 ns. Reset time based on RPS distributes from 10 ns to 60 μs. Fixed set and reset pulse at slowest case will lead to large set power and reset failure.

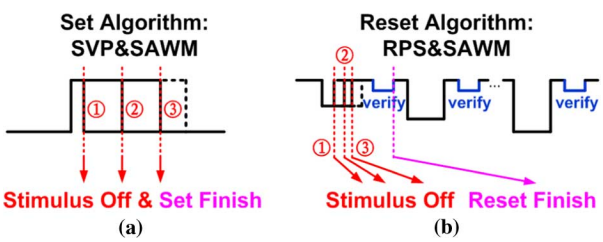


Fig. 2. Set and reset algorithms with SAWM: (a) SVP&SAWM for set and (b) RPS&SAWM for reset. Three cells with different set and reset times are given respectively.

II. Self-Adaptive Write Mode

A. Write Algorithm With Self-Adaptive Write Mode

Fig. 2 shows the set and reset algorithms with the proposed SAWM. During set/reset, the cell resistance is monitored and the enforced stimulus will be turned off once a resistance switch is detected. Power consumption and the write disturbance issues can be effectively resolved by means of SAWM. In our work, the response time from the resistance switch to the turn-off of write stimulus is key for power consumption saving and write disturbance elimination.

B. Circuit Implementation

Fig. 3 shows the write path with SAWM. Along the write path, there are a verdict module, a write bias module, a SAWM module, a polarity selector, a column selector and an array of ReRAM cells. The SAWM algorithm is implemented by the SAWM module with the verdict module. The SAWM module monitors the cell resistance in real time during set/reset and provides the verdict module with a feedback signal, FB, which indicates the cell resistance switch. Because the write voltage Vwrite is made relatively constant by the regulator, the change of the current through the write path Iwrite will reflect the cell resistance switch. To achieve a short settle time of Iwrite after the switch of cell resistance during set/reset, the single-stage operational transconductance amplifier (OTA) is chosen to implement the amplifier in the regulator because it has larger bandwidth compared with other sophisticated structures. Moreover, the gain of the amplifier can be exchanged for higher bandwidth to improve its performance. Although the tracking error of the regulator may increase due to less gain, this doesn't affect the write operation since Vwrite is not a fixed value for set/reset. Iwrite is then duplicated by the current mirror to obtain the current Im, which is imposed over a sample resistor Rs to acquire a sample voltage Vs. FB is acquired by comparing Vs with the reference voltage Vref.

The verdict module determines whether the write process is finished by assigning the enable signal COMP "1" standing for "not finished" or "0" standing for "finished" according to the write enable signal WEN, the written value DATA, and FB from the SAWM module. The verdict module is consisted of a number of logic gates and two pull-down transistors. Fig. 4 shows the timing waveforms of the verdict module during reset and set. At the beginning of both reset and set, WEN becomes "1" first, and then the signal PU which lags several nanoseconds behind WEN, pulls up the signal Flag to "1" through M1. Thus, COMP is evaluated to be "1" to ensure that the write bias and SAWM modules to begin to generate an appropriate writing voltage. After PU becomes "1", the state of Flag will depend on the XNOR result of DATA and FB_B, which is the inversion of FB. During set, FB first rises from "0" to "1" after the cell resistance switches to R_{on}, and then returns to "0" after the write stimulus is off. In order to turn off the write stimulus after FB first switches from "0" to "1", COMP should be kept as "0" by locking Flag as "0", which is realized by pulling FB_B down to "0" through transistors PD1 and PD2. Otherwise, oscillation may take place around the feedback loop during set.

The amplitude of Vwrite can be adjusted by setting Bias[M:1] and the polarity of Vwrite can be determined using a polarity selector. The write bias module, as shown in Fig. 5, is formed by a resistive voltage divider and a multiplexer. The resistive voltage divider divides the voltage drop from power to ground into 32 levels and the multiplexer selects the required level as the bias voltage, which is then fed into the voltage buffer. The polarity selector is composed of a pull-down transistor and four transfer gates and determines whether the write stimulus is applied on BL or SL according to DATA. The pull-down transistor PD3 will pull Vwrite to ground when COMP is "0". Even if PD3 is omitted, the write bias module can independently turn off the

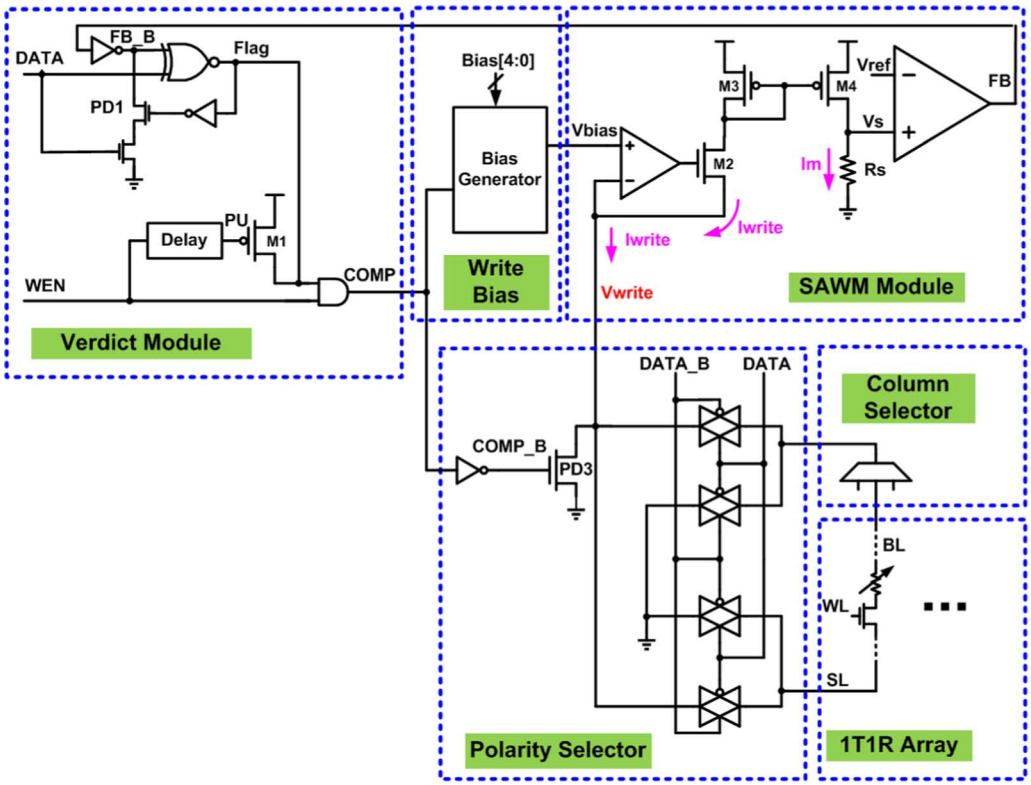


Fig. 3. The write path with SAWM consists of verdict module, write bias module, SAWM module, polarity selector, column selector and array.

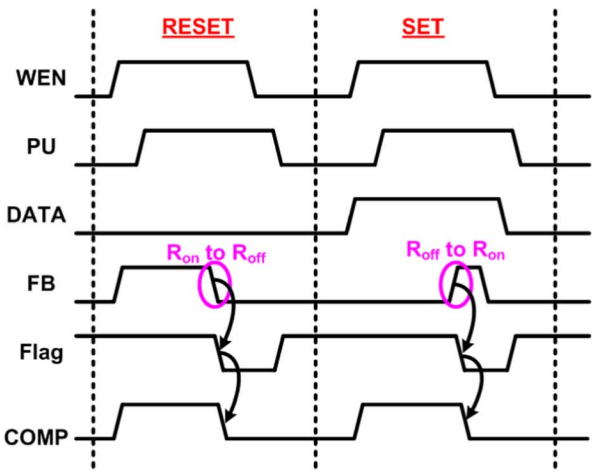


Fig. 4. Timing waveforms of verdict module during reset and set.

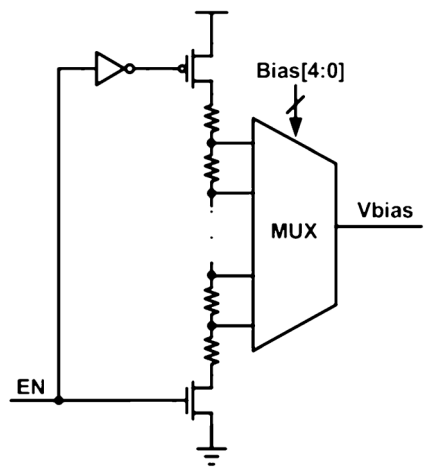


Fig. 5. Bias generator composing a resistive voltage divider and a multiplexer.

write stimulus, the function of PD3 is to provide a faster response to the COMP signal path by having one inverter delay to the gate of PD3 which quickly disables the write stimulus Vwrite. This process offers the advantages of further saving the set power and reducing the write disturbance during reset.

Fig. 6 shows the simulation result of the write critical path employing the proposed SAWM. The reset and set operations are executed in succession assuming that the required set and reset times are both 20 ns. At the beginning of set/reset, PU lags behind WEN by about 4 ns to forcibly pull up Flag high and thus COMP becomes effective to start write operation. When the cell resistance switches from $R_{on}(R_{off})$ to $R_{off}(R_{on})$ during reset (set), Iwrite will decrease (increase), so will Iw and Vs. Then, FB will switch from "1" ("0") to "0" ("1"). After that, COMP will become ineffective to turn off Vwrite. Moreover, the total delay from the cell resistance switch to the turn-off of Vwrite consists of three parts, such as the propagation delay of the SAWM module (Delay0), the propagation delay of the verdict module (Delay1), and the propagation delay arising from the polarity selector, the column selector, and the bitline or source line in all (Delay2). From Fig. 6, the total delay from the cell resistance switch to the turn-off of Vwrite can be as fast as 1.9 ns and 1.8 ns for reset and set, respectively. Delay0 to Delay2 for reset are 0.74, 0.57, and 0.59 ns, respectively, and for set are 0.62, 0.58, and 0.60 ns, respectively. Delay0 of reset is larger

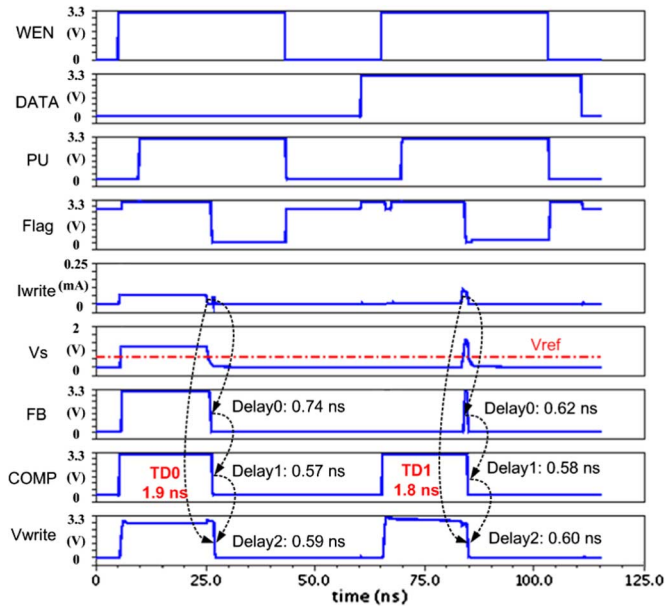


Fig. 6. Simulation waveforms of the write critical path employing the proposed SAWM.

than that of set because Vs falls more slowly for a smaller Iwrite after the cell switches to R_{off} during reset.

III. Self-Adaptive Read Mode

SARM is based on the dummy row to generate a dynamic reference to maintain sufficient sense margin for read operation even at high temperature. Fig. 7 gives the employed block architecture with the cell array of 258 rows multiplied by 256 columns. Unlike the reference array which is independent from the main array [10], two dummy rows divide one block into upper and lower halves and share the same column selector and write driver with the main array, which can ensure lower peripheral overburden and more accurate tracking of the cell resistance variation in the main array. The cells in the dummy rows are configured as R_{on} or R_{off} according to resistance distribution. Twisted bitline architecture is employed to supply separate read path for signal and reference [14]. According to the most significant bit (MSB) of row address in the selected block, a read operation activates a row in one half and enables a corresponding dummy row in the other half. The BLs/BLBs of the selected dummy row are shorted by activating the corresponding equalization signal (EQ0 for the lower dummy row/EQ1 for the upper dummy row).

The equivalent circuit of the dummy row reference generation is shown in Fig. 8(a), where the equivalent resistances of the equalization transistor and the access transistor are modeled as R_{EQ} and R_{AT}, respectively. Each BL/BLB has a bias current Ibias from the SA to produce a BL/BLB voltage during read. Because the role of equalization transistors is to short BLs/BLBs, its size is considered to make R_{EQ} negligible. R_{AT} is also negligible compared with the cell resistance R_{on} or R_{off}. Assuming that the ratio between R_{off} and R_{on} cells is (N-1), the equivalent circuit can be simplified by dividing all the BLs/BLBs into 256/N groups as shown in Fig. 8(b), where (N-1) R_{off} cells and one R_{on} cell can be combined as a resistor with a current of $N * Ibias$ passing, where the resistance is equal to $R_{off}/(N-1)\|R_{on}$. Thus, the reference voltage can be approximately calculated as

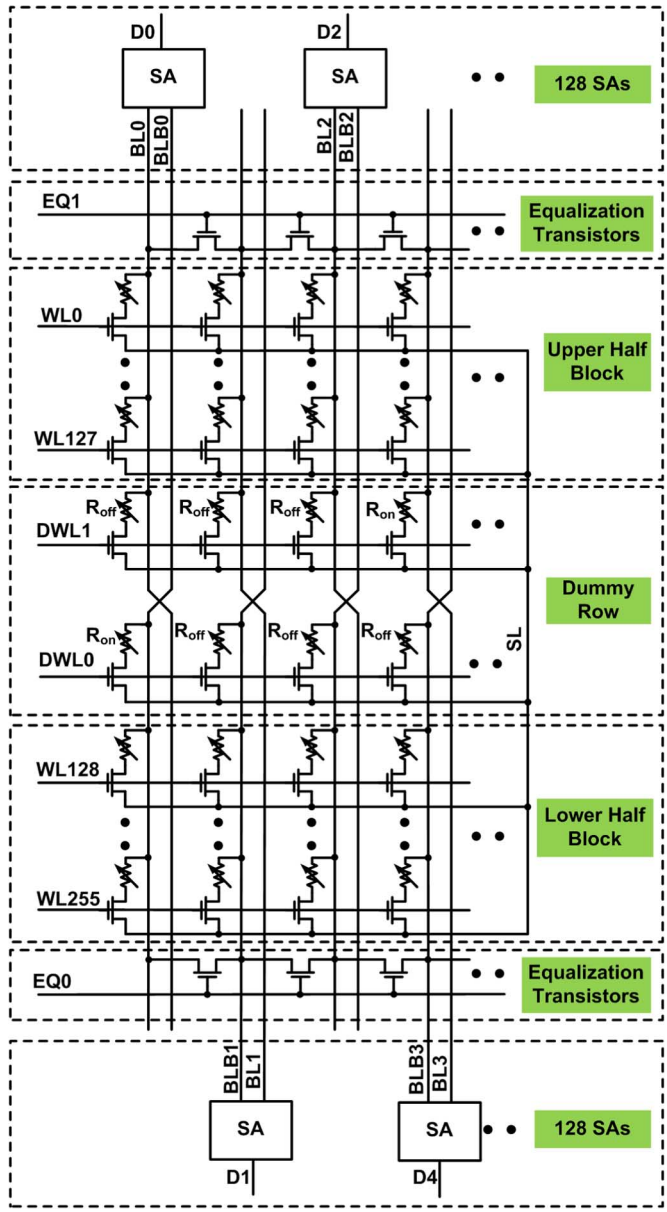


Fig. 7. $256 * 256$ block architecture having two dummy rows and on-pitch SA for SARM.

$$Vref = \left(\frac{R_{off}}{N-1}\|R_{on}\right) * N * Ibias \quad (1)$$

The sufficient cells in the dummy row can keep the reference voltage from being affected by rare tail bits. Moreover, the reference voltage can adaptively move toward R_{on} because the resistance of R_{off} cells will decrease significantly when the temperature rises.

The voltage sensing SA with a width of only two adjacent columns, as shown in Fig. 9, is embedded on-pitch to generate the BL/BLB read voltage for the cells in the selected normal and dummy rows. The high area efficiency of SA also makes it possible to read out all the 256 cells in the selected row at a time and provide high bandwidth throughput. The on-pitch SA

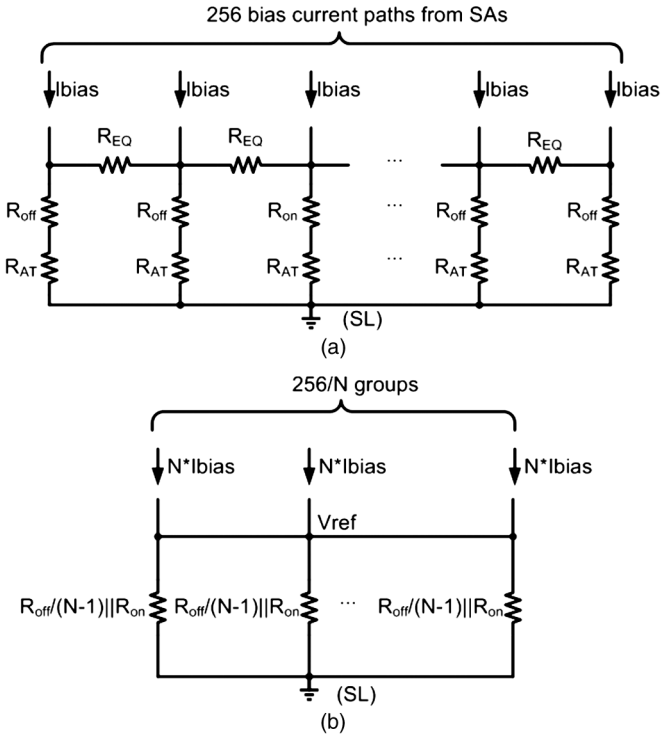


Fig. 8. (a) Equivalent circuit of dummy row, equalization transistors for reference generation, and (b) the corresponding simplified circuit.

consists of a latch amplifier (M11–M15), clamping transistors M3–M4, load transistors formed by current mirror (M6–M7), as well as equalization transistor M0 and precharge transistors M1–M2. Ibias of about 1 μA is forced into the cells in the selected normal and dummy rows via the current mirror to produce a read voltage on each BL/BLB. As shown in Fig. 1, there is no read disturbance in the positive voltage direction, and this advantage is employed to increase the read voltage as high as 0.6 V to obtain large sense margins.

Fig. 10 shows the Monte Carlo simulation result for SARM based on 1000 samples at 25°C and 125°C. For typical R_{on} ranging from 35 KΩ to 45 KΩ and R_{off} of 20 MΩ at room temperature, the dummy row should be configured as one R_{on} every 7 R_{off}s to produce a reference voltage located between R_{on} and R_{off}. From (1), Vref can be calculated as

$$Vref = \left(\frac{20\ \mathrm{M\Omega}}{7} \| 40\ \mathrm{K\Omega}\right) * 8 * 1\ \mu\mathrm{A} \approx 0.32\ \mathrm{V} \quad (2)$$

which is almost at the middle of the read voltages for R_{on} and R_{off}. Hence large sense margins are acquired for both R_{on} and R_{off}. In addition, the reference voltage moves dynamically toward R_{on} by about 0.1 V at 125°C to maintain adequate sense margins.

Fig. 11 shows the simulation result of reading R_{off} and R_{on} cells. The read operation begins with BLs and BLBs being precharged to Vref, which is about 0.32 V at room temperature. Then the selected WL and corresponding DWL, for example, WL0 and DWL0, are then activated to evaluate BL and BLB voltages under the bias current Ibias. When the voltage difference between BL and BLB reaches an adequate margin, the

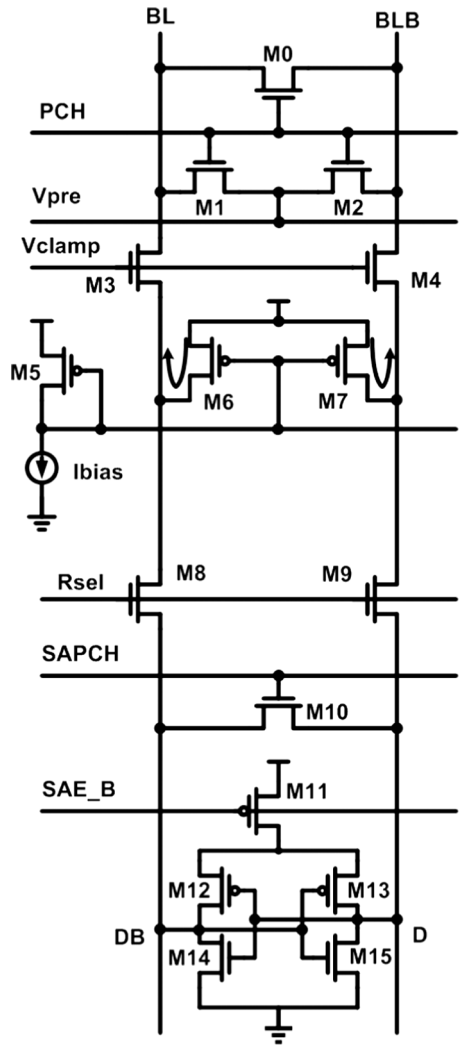


Fig. 9. Voltage-sensing SA is embedded on-pitch to get high array efficiency and support high bandwidth read.

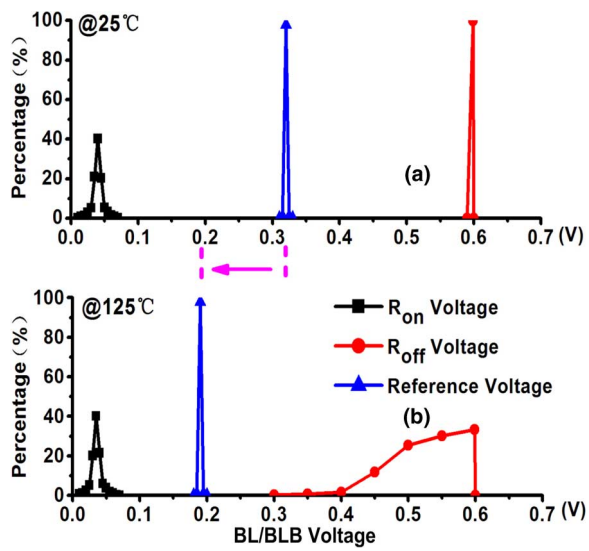


Fig. 10. Monte Carlo simulation for SARM based on 1000 samples (a) @25°C and (b) @125°C.

latch SA is turned on by activating SAE_B to resolve the sense nodes Dx and DBx. By simulation, the read access time for

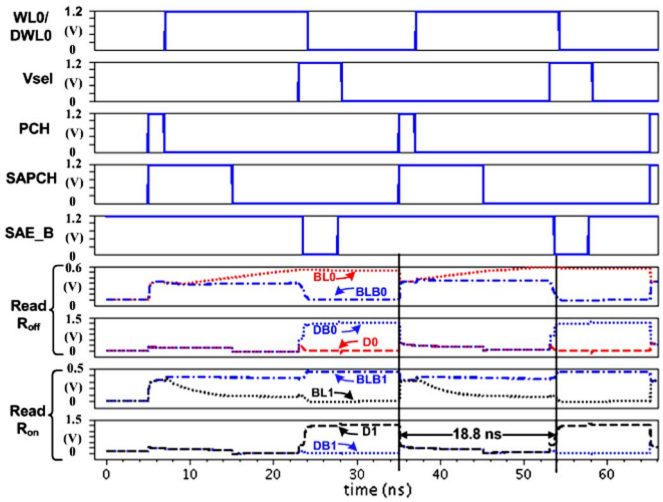


Fig. 11. Simulation results for reading R_{on} and R_{off} cells.

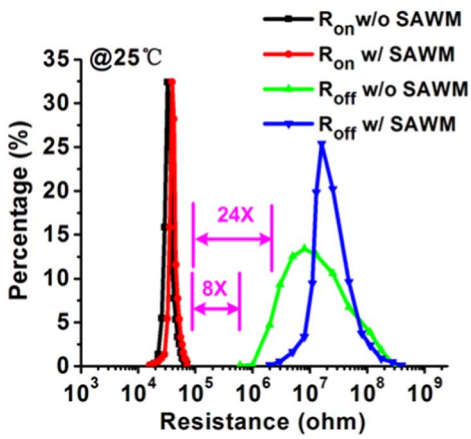


Fig. 12. SAWM for reset with RPS together significantly concentrates R_{off} distribution. Hence R_{off}/R_{on} window is increased from 8X to 24X.

reading R_{off} and R_{on} cells is about 18.8 ns from the beginning of bitline precharging to the appearance of valid data in the SA.

IV. Measurement Results

An 8 Mb Cu_xSi_yO ReRAM test chip is fabricated based on 0.13 μm logic process like our previous work [13]. Based on 8 Mb per chip, the measurement results demonstrate the effectiveness of SAWM and SARM proposed in this paper. The measured cell resistance distribution in Fig. 12 shows that SAWM helps to concentrate R_{off} distribution significantly and the R_{off}/R_{on} window is also increased from 8X to 24X. Fig. 13 shows that SAWM improves the reset bit yield from 61.5% to 100%, and SARM improves the read bit yield from 98% to 100%. By monitoring Iwrite and Vwrite when COMP is active during set/reset, the energy consumption for writing a bit can be estimated using the following equation

$$E \approx \int_{\mathrm{Tcomp}} Iwrite * Vwrite * dt \qquad (3)$$

Where, Tcomp is the duration time of COMP being "1". Fig. 14 shows the average energy consumptions are decreased by 40.6% and 99.1% for reset and set, respectively. The energy reduction percentage for set is much more remarkable than that for reset

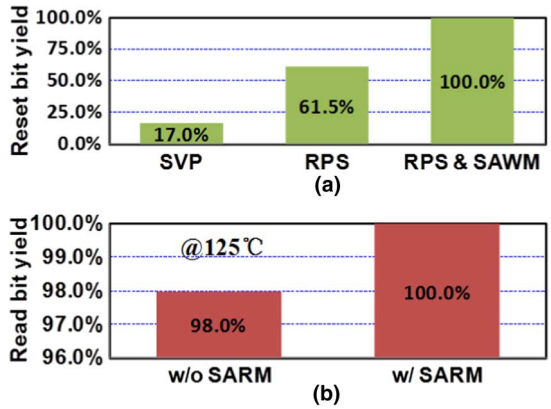


Fig. 13. (a) SAWM with RPS together fixes reset bit yield issue; (b) SARM fixes read bit yield issue at 125° C.

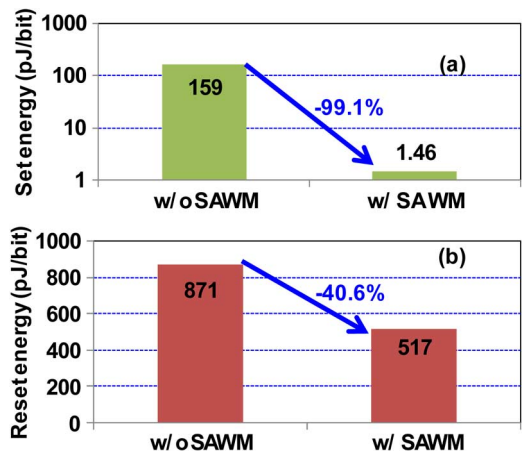


Fig. 14. (a) Set energy and (b) reset energy are remarkably saved with SAWM.

TABLE I
Key Parameters and Design Techniques of Test Chip

Process	0.13μm Logic based
Storage media	Cu_xSi_yO
Capacity	8Mb
Die size	7.5*6.9mm^2
Cell size	0.46*0.74μm^2 (20F^2)
Organization	256 row * 256 column * 8 block * 16 plane , dummy rows for SARM embedded in block array
Supply power	1.2V / 3.3V
Read access time	21ns typically
Reset yield enhancement feature	SAWM, reset bit yield improves from 61.5% to 100%
Set power reduction feature	SAWM for set
Read yield enhancement feature	SARM, read bit yield improves from 98% to 100% at 125 °C.

because a large unnecessary current flows through the cell when it switches to R_{on} during set, i.e. the set power consumption issue. Moreover, it can be expected that power will also be saved by SAWM whenever the set/reset time presents certain drift or variation, and that the more serious the drift or variation is, the

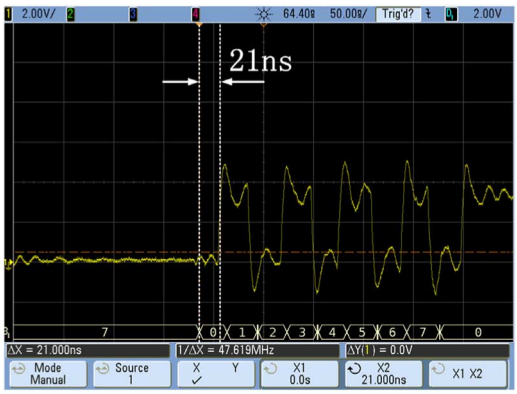
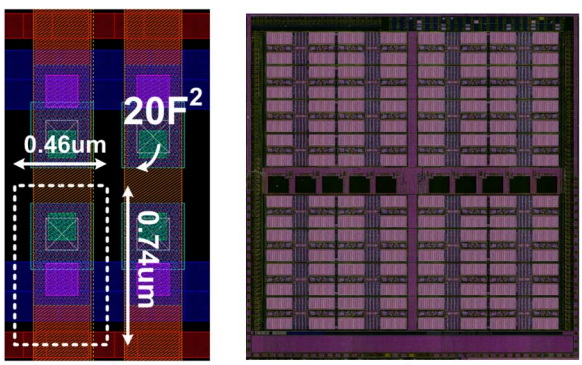


Fig. 15. Measured read access time is 21 ns in typical case.



(a) (b)

Fig. 16. (a) 1T1R cell layout with cell size of 20 F^2, (b) die micrograph.

more power can be saved. The key parameters and design techniques of the test chip are summarized in Table I. Fig. 15 shows that the measured read access time is 21 ns, which is larger than the simulation result due to the path delay from SA to IO pad. Fig. 16 shows the cell layout and die micrograph.

V. Conclusion

In this study, self-adaptive write and read assist circuits are proposed and successfully implemented in a 0.13 μm 8 Mb Cu_xSi_yO ReRAM test macro. The yield and power consumption issues arising from large variations in set/reset time and high-temperature cell resistance are resolved. SAWM can detect the cell resistance switch during set/reset and turn off the write stimulus in less than 2 ns, thereby improving the reset yield and lowering the required operation power. SARM uses the dummy row embedded in the main array to generate an adaptive dynamic reference voltage with on-pitch voltage SA. The reference can move toward R_{on} at high temperature to get adequate sense margins, thereby improving the read yield. The on-pitch SA structure also offers the potential benefit of high-bandwidth read throughput with a measured read access time of 21 ns. With its excellent compatibility with logic process and outstanding scalability, Cu_xSi_yO ReRAM exhibits great potential to replace e-Flash as embedded nonvolatile memory in SOC applications where the storage capacity ranges from tens of kilobits to several megabits.

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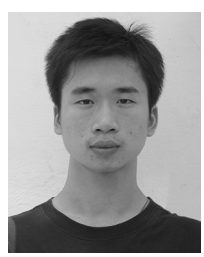
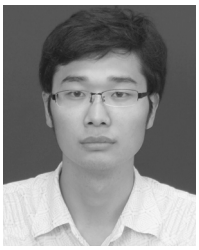


Wenxiang Jian received the B.S. and M.S. degrees from Huazhong University of Science and Technology, Wuhan, China, in 2006 and 2008, respectively. He is currently working toward the Ph.D. degree in microelectronics at Fudan University Shanghai, China.

His research interests include volatile and nonvolatile memory circuit test, built-in self-test, memory yield optimization, and design for test.



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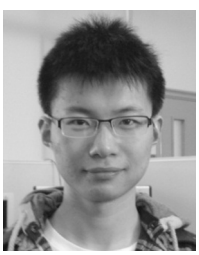
His research interests include volatile and nonvolatile memory circuit designs and high performance analog circuit design.



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His research interests include nonvolatile memory circuit design.

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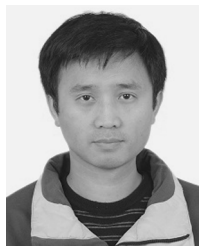

Ryan Huang received the B.S. degree in micro-electronics and solid electronics from Nanjing University, Nanjing, China, in 2002.

He joined Semiconductor Manufacture International Corporation (SMIC) in 2003 and has been focusing on technology development. He firstly took part in 0.13 um CIS/0.11 um Flash development, and then joined the team for RRAM development. Now, he is working on 28 nm HKMG logic technology development.

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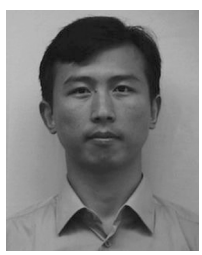
In 2008, he joined the technology development and research center in SMIC. He has been focusing on the memory technology research, including DRAM, RRAM.



Jingang Wu obtained his Bachelor degree in Huazhong University of Science and Technology in 1988 and his Ph.D. in Chinese Academy of Sciences in 1994.

He worked in AIST, Japan, as a NEDO fellow from 1995 to 2001. He joined SMIC in 2001 and was responsible for CMOS image sensor and memory development, led 0.13 um FCRAM development and 0.18 μm/0.11 μm CIS programs, and transferred the technologies to Fab for mass production. Currently he manages SMIC 28 nm High-K/Metal gate process development program, and also acts as senior director of advanced module division. He is also responsible for emerging memory technology development (RRAM).