Introduction to the Special Issue on the IEEE 2012 Custom Integrated Circuits Conference

THIS Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is comprised of 20 papers selected from the 2012 IEEE Custom Integrated Circuits Conference (CICC). The issue spans contributions in RF/wireless, high-speed I/O, and analog/mixed-signal including PLLs, data converters, power management, digital systems and analog techniques. The selected papers demonstrate state-of-the-art performance in power, area, or integration along with innovative circuit implementations and techniques.

Five papers selected from the analog and data converters papers were submitted to the journal. The first paper, by Balmelli *et al.*, describes a 3W class-D amplifier with improved linearity that reduces external filtering required for EMI protection by controlling the slew rate of the driver amplifier and digital modulation to spread the PWM common mode signal to place a null at the victim channel. The 110 nm CMOS design achieves SNR of 95 dB at 85% efficiency. The next paper, by Wong *et al.*, reports a 2.3 mW 10-bit 170 MS/s ADC in 65 nm CMOS using a two-step binary-search assisted time-interleaved SAR architecture. The third paper, by Nandi *et al.*, presents a continuous-time sigma-delta ADC with a switched-capacitor return-to-zero DAC that helps to reduce sensitivity to clock jitter and improves linearity. The prototype ADC designed in a 180 nm process achieves an SNDR of 82.3 dB for a 2 MHz bandwidth while consuming 16.5 mW and reduces clock jitter sensitivity by 28 dB. The fourth paper, by Razavi, presents a comprehensive design considerations for interleaved ADCs and proposes a background timing mismatch calibration technique to reduce the image to -75 dB for input frequencies more than 500 MHz. The final paper in the section, by Wu *et al.*, describes a 40 nm 2.1 GS/s 2x time-interleaved pipeline ADC that uses a digital MDAC equalization techniques using FIR filters. The 12-bit design achieves SNDR of 52 dB while consuming 240 mW.

The next four papers cover various topics in RF design. The first paper in the section, by Samarah and Chan Carusone, describes a digital PLL that uses a coarse/fine TDC. The fine TDC is implemented using stochastic techniques to achieve overall TDC resolution of 4 ps. The concept is demonstrated in a 130 nm 1.99–2.5 GHz PLL with 213 fs rms integrated jitter. The second paper, by Ghilioni *et al.*, describes dynamic latches, where the regenerative cross-coupled pair is removed for maximum speed, demonstrated in prototypes of divide-by-4 circuits in 32 nm CMOS operated between 14 GHz and 70 GHz. The next paper, by Yin and Luong, presents a switched-triple-shielded transformer technique to realize a wideband CMOS VCO that can tune from 57.5 GHz to 90.1 GHz. The last paper in the RF section, by Rafi and Viswanathan, reviews techniques for improved harmonic reject mixers using clock gating that allow better than 52 dB rejection for 3rd/5th/7th LO harmonics without any calibration.

The next three papers were selected from papers presented on wireline topics at the conference. Kocaman *et al.* present a reference-less CDR for SONET transceivers that uses an algorithmic frequency acquisition without using a training sequence. The concept is demonstrated on a 65 nm transceiver that achieves 400 μs acquisition time and a jitter tolerance of 0.5 UI for 10 mVppd input sensitivity. The second paper, by Tabasy *et al.*, describes a 20 mW 6b 1.6 GS/s ADC with embedded partial equalization using a 1-tap DFE for serial receivers. The prototype receiver is demonstrated at 1.6 GS/s over 46-inch FR4 link with 14 dB loss while achieving a 0.2 UI timing margin. In the next paper, Lu *et al.* present a 10 Gb/s 2-tap reconfigurable pre-emphasis transmitter that consumes 10 mW in a 65 nm LP CMOS.

The next section presents three papers that describe advances in power management techniques especially for SoC applications reported at the conference. The first paper in the section, by Kudva and Harjani, proposes an adaptive all-digital ripple mitigation technique for fully integrated capacitive DC-DC converters. Coarse ripple control is achieved by varying the size of the bucket capacitance, and fine control by time modulation of the charge/discharge charge transfer capacitors. The 130 nm design presented achieves $\sim$3x ripple reduction, 70% efficiency, and 24.5 mW/mm^2 maximum power density. The next paper, by Alioto *et al.*, presents a power management unit with a reconfigurable switched-capacitor converter in 65 nm CMOS to reduce the energy cost with sleep-to-active and active-to-sleep transitions by 64%. This energy reduction comes at small area overhead (lower than 1%) and no penalty in active mode. The third paper in the section, by Nakase *et al.*, presents a 190 nm CMOS, 87% efficiency, 0.75 mm^2 on-chip feed-forward single-inductor dual-output (SIDO) boost DC-DC converter for battery and solar cell operation with 0.5 V startup.

The next section presents five papers that extend the state of the art in design of SoC and processors. The first paper in the section, by Painkras *et al.*, presents a 130 nm SoC with 18 cores, 100 million transistors in a 102 mm^2 die, that achieves a peak performance of 3.96 GIPS for 1 W peak power. The next paper, by Huang *et al.*, presents energy-efficiency techniques used to reduce power consumption of a 20 MB L3 cache used in the Xeon© E5 processor family. The next paper, by Raychowdhury *et al.*, describes a power-efficient voice-activity-detector-based audio front-end for context-aware SoC applications in 32 nm CMOS that consumes 2.3 nJ per frame. The design achieves ultra-low power by employing multi-frequency operation with dual supplies that allow CMOS operation in the near threshold regime. The fourth paper, by Kim *et al.*, describes a 90 nm CMOS, 1 mJ/frame unified media application processor with a 179.7 pJ mixed-mode feature extraction engine for em-

Digital Object Identifier 10.1109/JSSC.2013.2264612

bedded 3D media content processing. The last paper, by Fuketa *et al.*, presents an analysis and model of the increase of crosstalk noise due to imbalanced threshold voltage between NMOS and PMOS in subthreshold logic circuits.

The guest editors of the issue would like to thank the authors for the timely high quality of submissions and the reviewers whose effort ensured that the papers met the high quality levels required by the journal. We hope you enjoy reading it!

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