Cancellation of OpAmp Virtual Ground Imperfections by a Negative Conductance Applied to Improve RF Receiver Linearity

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***Abstract*—High linearity CMOS radio receivers often exploit linear V-I conversion at RF, followed by passive down-mixing and an OpAmp-based Transimpedance Amplifier at baseband. Due to nonlinearity and finite gain in the OpAmp, virtual ground is imperfect, inducing distortion currents. This paper proposes a negative conductance concept to cancel such distortion currents. Through a simple intuitive analysis, the basic operation of the technique is explained. By mathematical analysis the optimum negative conductance value is derived and related to feedback theory. In- and out-of-band linearity, stability and Noise Figure are also analyzed. The technique is applied to linearize an RF receiver, and a prototype is implemented in 65 nm technology. Measurement results show an increase of in-band IIP_3 from 9 dBm to >20 dBm, and IIP2 from 51 to 61 dBm, at the cost of increasing the noise figure from 6 to 7.5 dB and <10% power penalty. In 1 MHz bandwidth, a Spurious-Free Dynamic Range of 85 dB is achieved at <27 mA up to 2 GHz for 1.2 V supply voltage.**

***Index Terms*—Receiver linearity, interference robustness, compression, blocking, in-band and out-band IIP_3, IIP_2, mixer-first receiver architecture, transimpedance amplifier (TIA), negative conductance technique, CMOS, wideband base station receiver, software radio, software defined radio, cognitive radio.**

I. Introduction

LINEARITY requirements on radio receivers become increasingly challenging, as the radio spectrum becomes more crowded. Moreover, there is a trend towards more wideband and more flexible radio hardware with less dedicated RF filtering ("Software Defined Radio"). As an example, Fig. 1 plots IIP_3 requirements calculated for E-UTRA for a wideband base station receiver in three scenarios: wide area, local area and home [1]. Apart from the high 100 MHz bandwidth, note the sudden step in IIP_3 requirements at the band-edge. Also note that less coverage area (home versus wide area), corresponds to higher in-band IIP_3 but a smaller step to out-of-band IIP_3 (i.e., around 16 dB for home area versus 40 dB for wide area). As a consequence of the lack of a reasonable transition band, on-chip analog filtering is ineffective to relax the IIP_3 requirement, and off-chip filters are expensive. Depending on the blocker scenario, compression point requirements may or may not be affected. In this paper, we propose a circuit technique that can increase IIP_3 simultaneously for in- and out-of-band, at roughly constant compression point. Receivers with high IIP_3 are also very important for opportunistic dynamic spectrum access via a cognitive radio, as is exemplified in Fig. 2 for a Digital TV band. Strong interferers (incumbent TV signals) may be present in directly adjacent channels, again making on-chip RF filtering ineffective. Again, high linearity is required also to prevent cross-modulation effects [2] from desensitizing the receiver. A part from the RF receivers, the spectrum sensing front-end also requires high in-band IIP_3 in order to minimize the errors in detecting the empty channels in the spectrum.

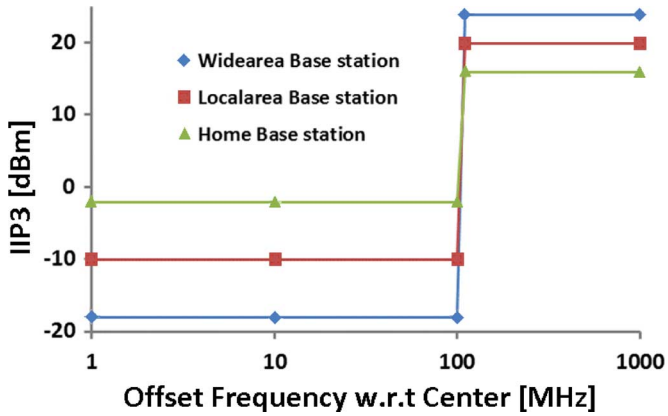

Fig. 1. Example IIP_3 requirement for E-UTRA [1].

Strong RF interference can easily clip baseband amplifiers, while higher required bandwidths limit the amount of available loop-gain for negative feedback. When pushing linearity, avoiding voltage gain at RF (See Fig. 3) is instrumental [3]–[8]. Exploiting RF V-I conversion followed by passive down-mixing and then simultaneous I-V conversion and filtering at IF/baseband with OpAmps, an out-of-band IIP_3 of up to $+18$ dBm has been shown [3], [4]. Passive mixer-first architectures can even achieve up to $+25$ dBm out-of-band

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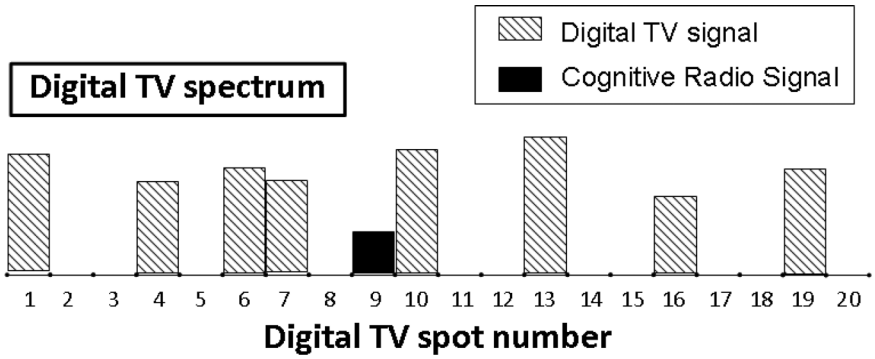

Fig. 2. Digital TV spectrum [2] in which a cognitive radio operates in an adjacent channel.

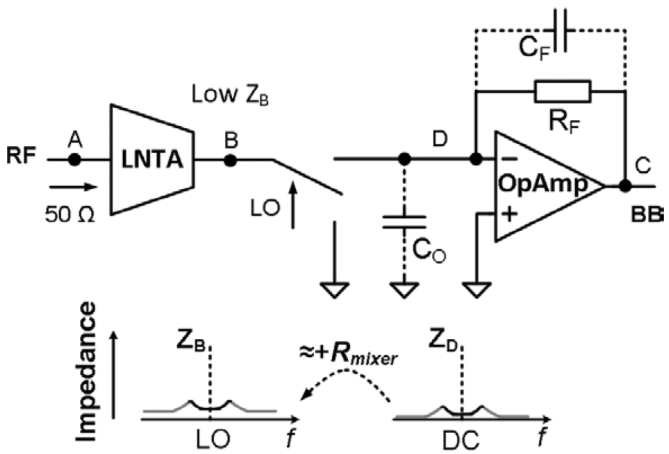

Fig. 3. High blocker tolerant linear receiver.

$\mathrm{IIP_3}$ [7]. However in-band $\mathrm{IIP_3}$ is much worse, certainly at high gain. The best in-band $\mathrm{IIP_3}$ results that we found for receivers were $+3.5$ dBm for [3] at 34 dB gain and $+11$ dBm for [6] at 19 dB gain. Analysis shows that finite OpAmp gain can be a bottleneck, as a non-zero virtual ground node voltage can result in distortion currents. In [9], we recently proposed to exploit a negative conductance technique to cancel distortion currents. In this way, the design of the OpAmp is relaxed and its performance no longer needs to be a bottleneck. The use of a negative conductance has been proposed in [10] to realize TIA flicker noise shaping. Paper [10] also briefly mentions linearity improvement, but linearity benefits were not the focus there. In this paper we will analyze the benefits of a negative conductance, compare analysis to measurements and report some extra experimental results in addition to [9]. Section II presents an intuitive model to understand the basic distortion cancellation concept. Additionally, the optimum negative conductance value is derived by mathematical analysis and related to negative feedback theory. Section III analyses stability issues related to this negative conductance technique. A receiver design, in which the concept is exploited, is discussed in Section IV. The receiver noise figure analysis including the negative conductance contribution is discussed in Section V. The analysis is verified by measurements in Section VI, while results are also benchmarked to other high linearity receivers. Finally, Section VII presents conclusions.

II. Linearization Concept

To understand the OpAmp linearity limitation and the distortion cancellation technique intuitively, it is instructive to follow a 4-step approach to analyze what happens at the virtual ground node "VGND", as illustrated in Figs. 4 to 8:

Step 1: Assume the RF V-I conversion and mixing are perfectly ideal (i.e., linear and infinite current source resistance for GM), we can use the equivalent baseband model in Fig. 4 (omitting the downconversion for simplicity). Assuming a 2-tone input signal $\mathrm{V_S(f)}$, the injected current $\mathrm{I_S(f)}$ to the VGND node is linear, so without $\mathrm{IM_3}$ tones. Now, if the OpAmp handles large signals at a high but finite gain, its output stage will produce $\mathrm{IM_3}$ products at the OUT node, i.e., $\mathrm{V_{OUT}(f)}$. However, as $\mathrm{I_S(f)}$ has no $\mathrm{IM_3}$ and the feedback resistor $\mathrm{R_F}$ is linear, the voltage over $\mathrm{R_F}$ does not contain $\mathrm{IM_3}$ (assuming negligible OPAMP input current). Consequently, the $\mathrm{IM_3}$ products of $\mathrm{V_{VGND}(f)}$ are in absolute sense equal to those of $\mathrm{V_{OUT}(f)}$ both in magnitude and phase. Let us denote this "$\mathrm{IM_3}$ copy" effect in Fig. 4 as "problem A". Note that the two main tones of $\mathrm{V_{VGND}(f)}$ are much smaller than that of $\mathrm{V_{OUT}(f)}$, as the ratio $\mathrm{V_{OUT}(f)/V_{VGND}(f)}$ for linear terms is equal to the loop gain. As a consequence the ratio between the linear terms and the $\mathrm{IM_3}$ products at VGND node is *much worse* than at the OUT node, causing a more serious problem discussed next.

Step 2: Assume we add a finite output resistance $\mathrm{R_O}$ as shown in Fig. 5. The nonlinear voltage $\mathrm{V_{VGND}(f)}$ over $\mathrm{R_O}$ now generates a nonlinear current $\mathrm{I_O(f)}$, and hence $\mathrm{I_F(f)}$ becomes nonlinear. This current is absorbed by the OpAmp output stage and increases $\mathrm{IM_3}$ at both $\mathrm{V_{OUT}(f)}$ and $\mathrm{V_{VGND}(f)}$. We will denote this "$\mathrm{R_O}$ loading" effect on the VGND node in Fig. 5 as "problem B".

Step 3: Once one realizes the main cause for distortion current is $\mathrm{V_{VGND}(f)/R_O}$, it is easy to verify that adding a negative conductance with value $\mathrm{G_O = 1/R_O}$ between VGND and ground can be a solution (see Fig. 6). The negative conductance senses $\mathrm{V_{VGND}}$ and generates a copy of the distorted current $\mathrm{I_O(f)}$, which now flows in a "local circle"

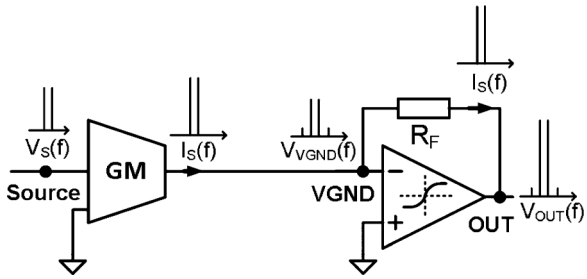

Fig. 4. OpAmp nonlinearity problem A: IM_3 is copied from the OUT node to the VGND node.

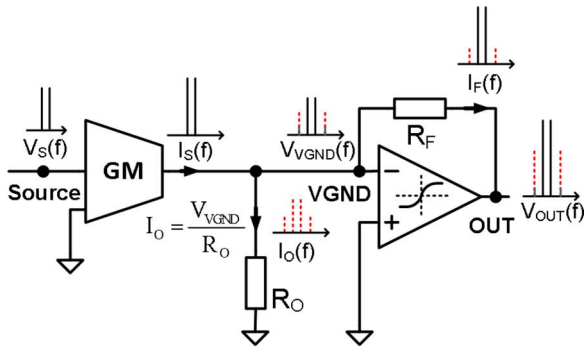

Fig. 5. OpAmp nonlinearity problem B: R_O loads the VGND node.

via the ground. Consequently, the current injected to the VGND node becomes linear again and we are back at the circuit of problem A, having solved problem B.

Step 4: Still, the OpAmp output voltage contains some IM_3, equal to that on the VGND node. By slight overcompensation this IM_3 contribution can also be cancelled. To show this, it is useful to model the floating resistor R_F with an equivalent network consisting of four single-ended linear transconductor blocks G_F ($G_F = 1/R_F$), all referred to ground as shown in Fig. 7(a). The two shorted G_F blocks, indicated with a dashed ellipse, can be replaced by a simple R_F resistor to the ground (see Fig. 7(b)). Thus Fig. 7(c) results with R_{F-VGND} and R_{F-OUT}, (loading resistances at the VGND node and the OUT node, respectively), G_{F-VGND} (the transconductance sensing V_{OUT} and injecting current to the VGND node), and G_{F-OUT} (the transconductance sensing V_{VGND} and injecting current to the OUT node). We assigned different names to G_F and R_F blocks in order to distinguish between their effects on nonlinearity at the VGND node and the OUT node separately. Fig. 7(c) clearly shows the loading effect of R_F (i.e., R_{F-VGND}) at the VGND node. Now, when the negative conductance cancels this loading effect (see Fig. 8), the injecting current of G_{F-VGND} becomes equal to the linear current I_S. As $V_{OUT} = I_S/G_{F-VGND} = -I_S \cdot R_F$, the OpAmp output voltage V_{OUT} becomes linear. This way problem A is solved as well.

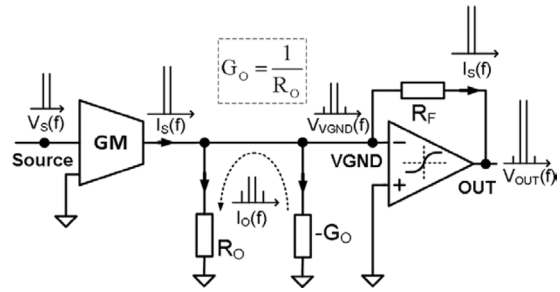

Fig. 6. Solving problem B via negative conductance with $G_O = 1/R_O$.

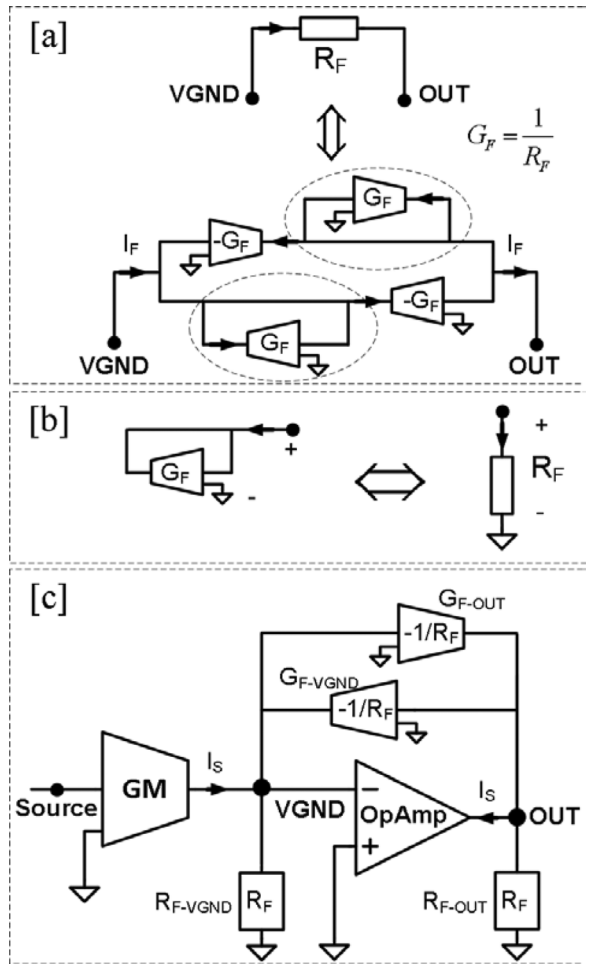

Fig. 7. Equivalent model of the effect that R_F has on the OUT node and the VGND node.

Overall, combining the solutions for problem A and B, the optimal total negative conductance is: $G_{TOTAL} = 1/R_O + 1/R_F$. To mathematically prove this optimum cancellation condition, the OpAmp (see Fig. 9) is modeled as an OTA with nonlinear transconductance and also a nonlinear output resistance because we aim for high output swing:

$$I_F = gm_1 V_{IN} + gm_3 V_{IN}^3 + go_1 V_O + go_3 V_O^3 \qquad (1)$$

In the model, we assume that the third order nonlinearities are more pronounced than the second order nonlinear terms, which is reasonable considering the OpAmp will be implemented in fully differential form. In the Appendix A, the nonlinear relation

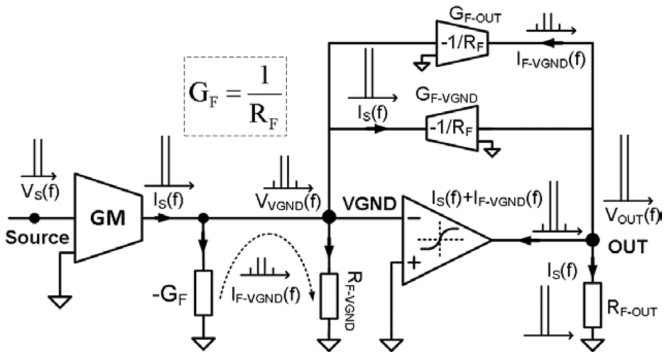

Fig. 8. Solving problem A via negative conductance with $G_F = 1/R_F$.

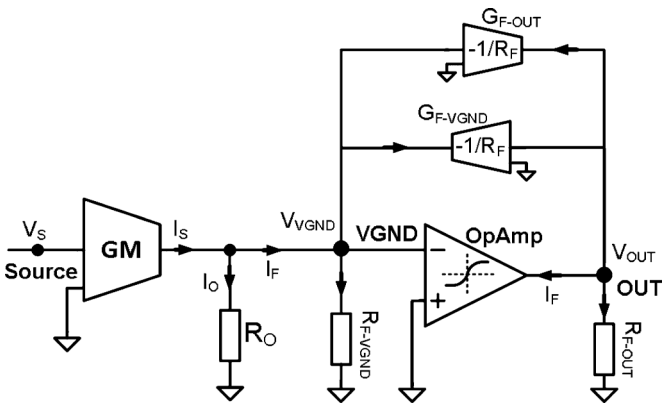

Fig. 9. Baseband model with R_O and the extended R_F for nonlinearity derivations.

between V_{OUT} and signal current I_S is derived using the model in Fig. 9. It can be expressed in terms of a linear (Ω_1) and third-order nonlinear (Ω_3) coefficient:

$$V_{OUT} = \Omega_1 I_S + \Omega_3 I_S^3 \tag{2}$$

The linear coefficient Ω_1 is the I/V conversion gain:

$$\Omega_1 = \frac{1}{\left[\frac{1}{a}\left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right) + G_{F-VGND}\right]} \tag{3}$$

Where (a) is a function of the linear terms of the OpAmp model (i.e., gm_1, go_1) and the R_F effects at the OUT node (i.e., R_{F-OUT} and G_{F-OUT}). For very high gm_1, (a) reaches $-\infty$. Consequently, the I/V conversion gain of (3) becomes $1/G_{F-VGND} = -R_F$.

The third-order distortion coefficient (Ω_3) is:

$$\Omega_3 = \frac{NL_3\left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right)}{\left[\frac{1}{a}\left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right) + G_{F-VGND}\right]^4} \tag{4}$$

where (NL_3: see Appendix A) is related to the nonlinear terms of the OpAmp model and is a function of (i.e., gm_1, gm_3, go_1 and go_3) and the effect of R_F on the OUT node (i.e., R_{F-OUT} and G_{F-OUT}). Now, if the *negative conductance technique cancels* $1/R_O + 1/R_{F-VGND}$ from (3) and (4) we see that Ω_1 reaches $1/G_{F-VGND} = -R_F$ and Ω_3 becomes zero (distortion is cancelled) Note that since the voltage swing at the VGND node is small, the effect of negative conductance nonlinearity can be very small.

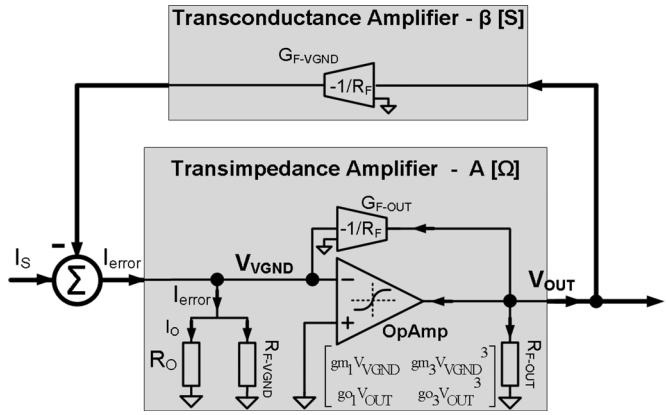

Fig. 10. Applying feedback theory to Fig. 9, excluding GM.

The linearity benefit can also be verified by applying feedback theory to Fig. 9 as shown in Fig. 10, excluding GM. The feedback topology of the circuit is Voltage-Current Feedback [11]. The output voltage (i.e., V_{OUT}) is sensed and converted to a proportional feedback current βV_{OUT}, where $\beta = G_{F-VGND}$ (in Siemens). This feedback current is subtracted from the input current I_S resulting in an error current $I_{error} = I_S - \beta V_{OUT}$ to be amplified by the block A. Here, $A = V_{OUT}/I_{error}$, where A has the dimension of a transimpedance [Ω]. It consists of all the blocks of Fig. 9, excluding GM and G_{F-VGND}. Actually for finite A, there will be a non-zero I_{error} due to the loading effect of R_O and R_{F-VGND} on the VGND node. Now the negative conductance increases the input impedance of the A block to infinity by cancelling R_O and R_{F-VGND}, so that I_{error} becomes zero and $A = V_{OUT}/I_{error} = \text{infinity}$. Consequently, loopgain $A\beta$ goes to infinity and V_{OUT}/I_S achieves its ideal value $1/\beta = R_F$, i.e., perfect linearity. We conclude that the negative conductance technique increases the loop gain by increasing the value of A. Also note that only a finite value for G_O is needed to make the loopgain theoretically approach infinity, which is not possible by increasing gm_1 in the gain block. Although the feedback theory puts the application of a negative conductance technique in the right context, however the problem with control theory is that it assumes blocks with unilateral operation, which are sometimes not easy to identify (e.g., see Fig. 10: feedback resistor R_F which is supposed to realize the β block also becomes part of the A block). In compare to the feedback analysis, our analysis explains in a simple way how IM_3 is affected by R_O and R_F.

To verify the OpAmp model, we fitted the model derived above to simulations done for the OpAmp that will be introduced later in this paper. Fig. 11 shows a close agreement.

Now, before we proceed with detailed circuits design, we will first deal with a potential caveat of negative conductance: the risk of instability.

III. Stability Analysis

We will consider two stability aspects: 1) the risk of oscillation, based on a small signal model, and 2) the risk of latch-up.

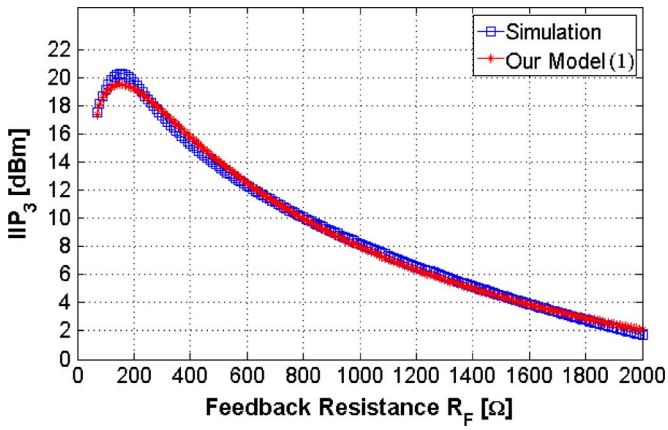

Fig. 11. OpAmp model (1) verification.

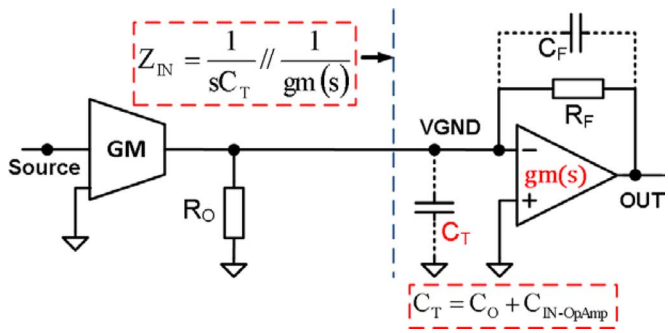

Fig. 12. Circuit diagram for small signal stability analysis.

Let us first look at the small signal behavior, referring to Fig. 12. As the low-pass filtering is desired, C_F is added as feedback capacitor. Capacitor C_T models the total input capacitance to ground of the OpAmp $C_{IN-OpAmp}$ and other capacitance C_O at the VGND node (see Fig. 3). For simplicity, the OTA is modeled as a frequency dependent transconductance with a dominant pole at ω_O and infinite output impedance:

$$gm(s) = \frac{gm_O}{1 + \frac{s}{\omega_O}} \tag{5}$$

Assuming no further loading at the OUT node, looking into the VGND node (see Fig. 12), the impedance (Z_{IN}) consists of the reactance of C_T in parallel to $1/gm(s)$:

$$\begin{aligned} Z_{IN} &= \frac{1}{s\,C_T} /\!/ \frac{1}{gm(s)} \\ &= \frac{1}{s\,C_T} /\!/ \left[\underbrace{\frac{1}{gm_O}}_{\text{Resistance}} + \underbrace{\frac{s}{gm_O \omega_O}}_{\text{Inductance (L)}} \right] \end{aligned} \tag{6}$$

Therefore, a parallel RLC tank is seen looking into the VGND node. If the negative conductance would both cancel $1/R_O$ and gm_O, then oscillation would happen at a resonance frequency that depends on the value of C_T and L (i.e., $f_{res} = 1/(2\pi\sqrt{C_T L})$). However, note that the typical virtual ground impedance $1/gm_O$ will normally be much lower than R_O and R_F. Thus, as the negative conductance G_{Total} is designed to cancel $1/R_O$ and $1/R_F$, the point of small signal instability can be designed to be safely far away.

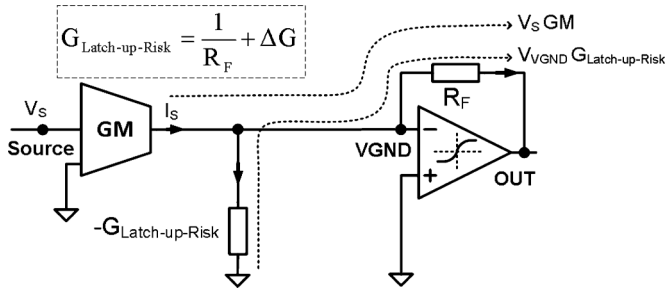

Fig. 13. Latch-up problem at the OUT node.

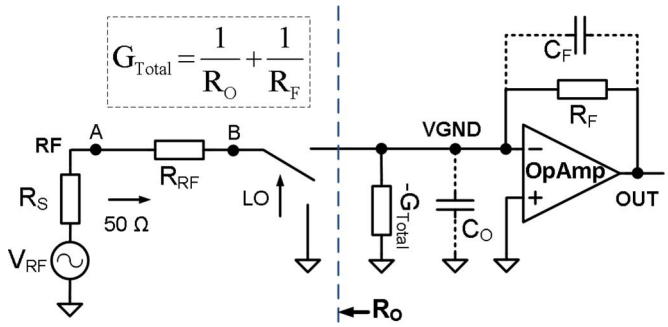

Fig. 14. Replacing the LNTA (GM) of Fig. 3 by a linear resistance R_{RF}.

Let us now look at the potential of latch-up of the OpAmp for a case that the negative conductance is too strong, i.e., it produces more current than needed after compensating the current in R_O. As shown in Fig. 13, the negative conductance injects current via R_F (i.e., $V_{VGND}G_{Latch-up-Risk}$) that needs to be handled by the OpAmp output stage in addition to the main current coming from GM (i.e., I_S):

$$\begin{aligned} &I_{OpAmp-Latch-up-Risk} \\ &\quad = I_S + V_{VGND}G_{Latch-up-Risk} \\ &\quad = I_S + \frac{1}{\left[\left(\frac{1}{R_{F-VGND}} - G_{Latch-up-Risk}\right) + a\,G_{F-VGND}\right]} \\ &\qquad \times I_S G_{Latch-up-Risk} \end{aligned} \tag{7}$$

Where the relation between V_{VGND} and I_S is derived in Appendix B. Referring to Fig. 13 and substituting $G_{Latch-up-Risk} = (1/R_F) + \Delta G$, in (7) gives the following relation:

$$I_{OpAmp-Latch-up-Risk} = I_S \left[1 - \frac{\Delta G + \frac{1}{R_F}}{\left(\Delta G + \frac{a}{R_F}\right)}\right] \tag{8}$$

The OpAmp output stage current flows throw R_F and make a voltage drop. The peak of this voltage drop is around $VDD/2 - V_{OpAmpOutputStage-OV}$, where $V_{OpAmpOutputStage-OV}$ is the over drive voltages of the OpAmp output stage transistors. Hence, if very strong negative conductance has been used (i.e., high ΔG in (8)), then the current of (8) becomes higher than the OpAmp output stage current capability and the latch-up occur.

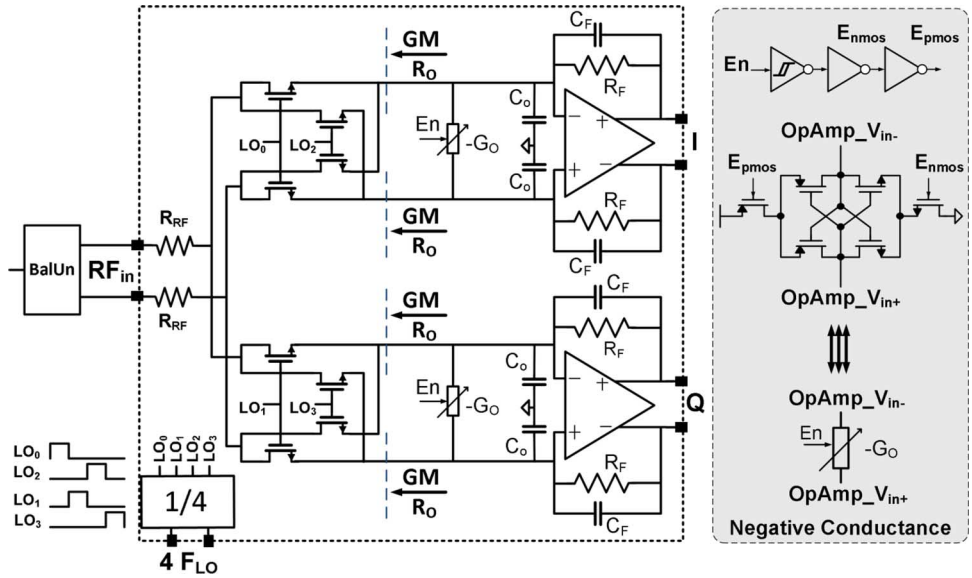

Fig. 15. Complete receiver with distortion compensation by $-G_O$.

IV. Receiver Design

We will now apply the negative conductance idea to a high linearity zero-IF radio receiver architecture of Fig. 3. To demonstrate the linearity potential of this technique, we will replace the active V-I conversion by a more linear fully passive mixer with resistors in series [4], as shown in Fig. 14. Fig. 15 shows the complete front-end IC schemati including the negative conductance. Using the equivalent model in Fig. 5, we can model the RF part of each branch in I and Q as a grounded resistor R_O and a transconductor GM referred to ground as denoted in Fig. 15. However, as resistor R_{RF} is in series with the mixer on-resistance $R_{ON-MIXER}$ and the virtual ground impedance R_{VGND} of the OpAmp, the equivalent GM now equals $1/(R_{RF} + R_{ON-MIXER} + R_{VGND})$. This is chosen to be 20 mS to realize RF input impedance matchingof 50 Ω, assuming perfect non overlapping 25% duty-cycle clocks, so the RF-input continuously sees a conduction path to ground. The equivalent output impedance of the mixer at baseband now is $R_O = 2\,(R_{BalUn} + R_{RF} + R_{ON-MIXER})$, where the factor 2 is due to the quadrature mixer with 25% duty cycle, connecting each I and Q baseband part to RF two times per LO cycle. To understand this point, let us derive R_O from the power that is delivered by a test voltage source (i.e., $V_{test} = V_a \cos(\omega_{LO} t)$) "looking back" in R_O as shown in Fig. 16. This source is connected to the first branch of the I-path. The current I_{test} will flow through $R_{ON-MIXER} + R_{RF} + R_{BalUn}$ two times LO-cycle, hence we get:

$$P = \frac{1}{T_{LO}}\left[\int_0^{\frac{T_{LO}}{4}} V_{test} I_{test}\,dt + \int_{\frac{T_{LO}}{2}}^{\frac{3T_{LO}}{4}} V_{test} I_{test}\,dt\right] = \frac{V_a^2}{4\,(R_{ON-MIXER} + R_{BalUn} + R_{RF})} \tag{9}$$

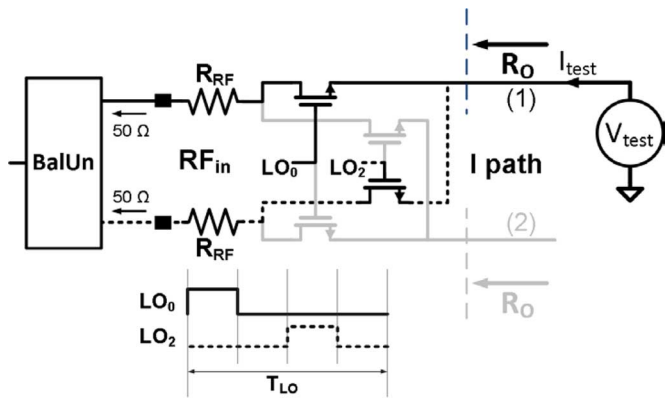

Fig. 16. Derivation of R_O.

This power must be equal to the power dissipation in R_O:

$$P = \frac{1}{T_{LO}} T_{LO} \int_0^{T_{LO}} \frac{V_{test}^2}{R_O}\,dt = \frac{V_a^2}{2R_O} \tag{10}$$

By equating (9) and (10), the following R_O is derived:

$$R_O = 2(R_{ON-MIXER} + R_{BalUn} + R_{RF}) \tag{11}$$

In the derivation of R_O, the power is only balanced with the fundamental, while the effect of the 3rd and higher harmonics are neglected due to the existence of C_O (see Fig. 15).

Now, the 50 Ω input impedance matching is implemented as a combination of series resistances $R_{RF} \approx 12\ \Omega$, the up-converted impedances of the passive mixer switches $R_{ON-MIXER} \approx 28\ \Omega$ plus the VGND impedance $R_{VGND} \approx 7\ \Omega$. The passive mixer consists of simple NMOS switches. $C_O = 8$ pF effectively shorts the LO leakage and high IF frequency components to ground. The TIA consists of a class-A input stage and a class-AB output stage, to maximize output swing (see Fig. 17, [12] and [3]). Common mode feedback ensures biasing at VDD/2. The feedback impedance is

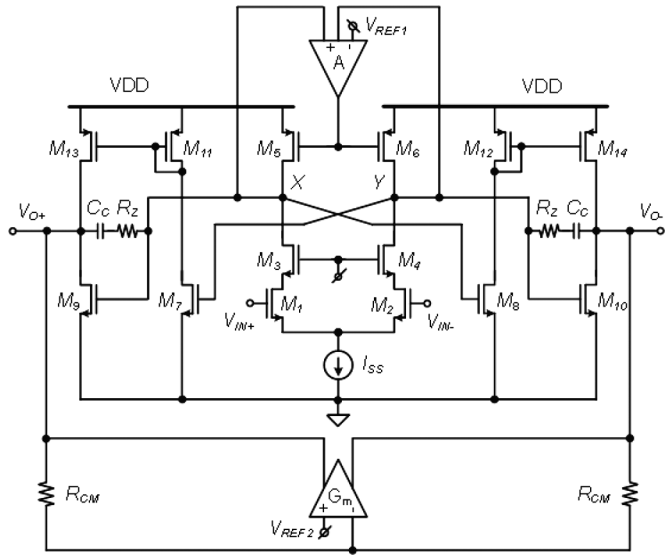

Fig. 17. Circuit diagram of the fully differential OpAmp design [12].

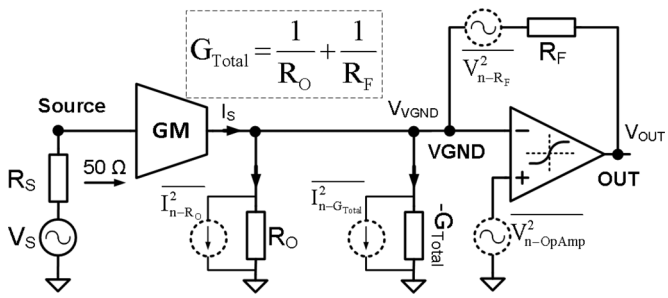

Fig. 18. Equivalent baseband model for noise figure analysis.

$R_F = 1.5$ kΩ and $C_F = 8$ pF, to obtain 26 dB voltage gain and a -3 dB-bandwidth of 12 MHz. The differential topology allows for a simple differential implementation of the negative conductance (right part of Fig. 15) and high IIP_2. To be able to measure what is the effect of different negative conductance values, $-G_O$ is implemented as a parallel array of identical "unit-transconductors", digitally controllable via multiplier M, with transconductance steps of 0.2 mS. Thus $M = 28$ renders $G_O = 5.6$ mS to compensate the nominal value of $R_O = 180\ \Omega$ ($R_O = 2\,(R_{BalUn} + R_{RF} + R_{ON-MIXER}) = 2(50 + 12 + 28) = 180\ \Omega$).

We will now consider the noise degradation resulting from the introduction of the negative conductance. Actually this noise can be cancelled by a noise cancellation path [4], [13], however this is expected to result in a linearity bottleneck in the auxiliary noise cancellation path. Hence we will analyze the noise figure degradation and aim for minimizing the noise penalty.

V. Noise Figure Analysis (NF)

Receiver topologies with a passive mixer and transimpedance amplifier (TIA), can suffer from amplification of OpAmp noise [14]. The output referred OpAmp noise contribution can be written as:

$$\overline{V^2_{n-OUT}} = \left(1 + \frac{R_F}{R_O}\right)^2 \overline{V^2_{n-OpAmp}} \tag{12}$$

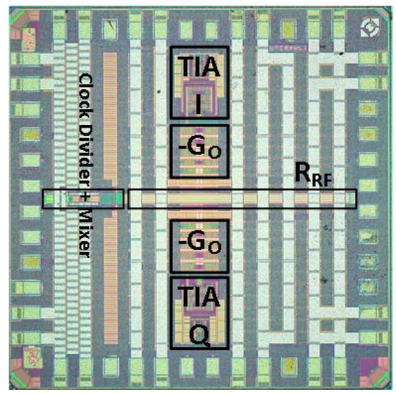

Fig. 19. Die photograph (65 nm CMOS, 1.45 mm × 1.45 mm).

Where $V_{n-OpAmp}$ refers to the (equivalent) input noise voltages of the OpAmp, R_O and R_F are as used in Fig. 5. For our design $R_F = 1.5$ kΩ and $R_O = 180\ \Omega$, then the amplification factor is equal to $(1 + R_F/R_O)^2 = 87$. Often a high RF V/I conversion (GM-value) is used to achieve an overall noise figure around or below 3 dB. Here we will use 20 mS, the value desired for input impedance matching. Fig. 18 shows a baseband model of Fig. 14 with noise sources added. The noise of GM is represented by the current noise source (I_{n-Ro}) of R_O. The noise of R_F is modeled via voltage noise source V_{n-RF}, while $I_{n-GTotal}$ represents the current noise source of the negative conductance. For simplicity, the OpAmp is modeled as a simple Transconductance (gm). To analyze the noise contributions of I_{n-Ro} and $I_{n-GTotal}$ to the output voltage, Ω_1 (i.e., the I/V conversion of the TIA (3)) is useful. The straightforward NF analysis shows:

$$NF = 1 + \frac{1}{\left(\frac{1}{2}\Omega_1 GM\right)^2 R_S}\left[\underbrace{\Omega_1^2\left(\frac{1}{R_O} + \gamma G_{Total}\right)}_{\text{First Term}} + \underbrace{\frac{\overline{V^2_{n-OpAmp}}}{\overline{I^2_{n-R_O}}}\frac{1}{R_O}\left(1 + R_F\left(\frac{1}{R_O} - G_{Total}\right)\right)^2}_{\text{Second Term}} + \underbrace{R_F\left(\frac{1}{gm\,R_F} - 1\right)^2}_{\text{Third Term}}\right] \tag{13}$$

The first term between the square brackets in (13) shows that the negative conductance G_{Total} has a direct noise contribution to the output. Its noise contribution is scaled by $\gamma/(((1/2)\,GM)^2 R_S)$. The "noise excess factor" γ can be minimized to around 2/3 (i.e., theoretically) by choosing a non-minimum channel length for the negative conductance transistors. Long-channel transistors are preferred for 1/f noise. We used 1 μm channel length in this design. The second term is the mentioned amplification factor (12) of OpAmp noise including the negative conductance effect (G_{Total}). It is interesting to observe that this term reaches zero when the negative conductance reaches G_{Total}. However, the direct

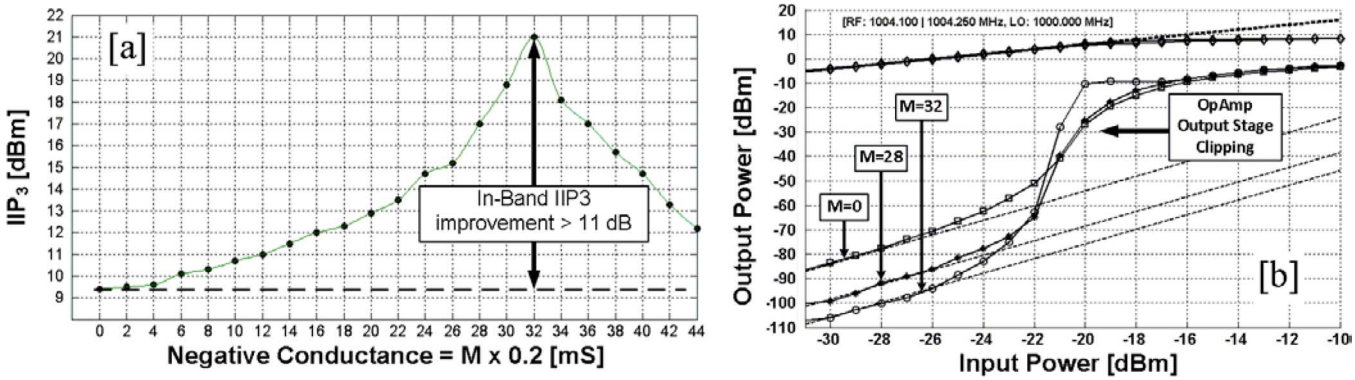

Fig. 20. Measurements: (a) In-band $\mathrm{IIP_3}$ vs. the number of parallel Negative Conductance Unit-Cells M (b) $\mathrm{IM_3}$ versus input power for three M settings, with $\mathrm{LO} = 1$ GHz.

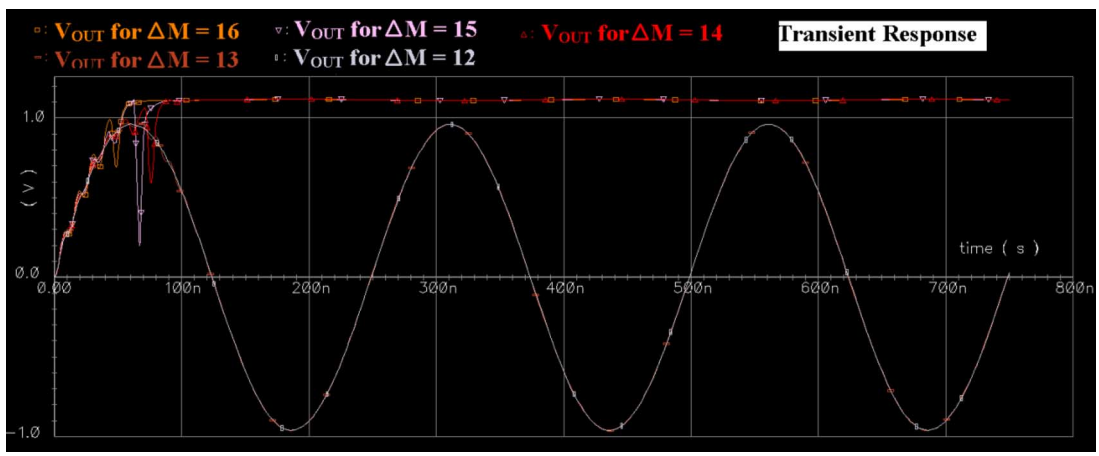

Fig. 21. Latch-up simulation of $\mathrm{V_{OUT}}$, input power of -16 dBm.

noise contribution of the negative conductance is much higher than the canceled OpAmp noise contribution, hence the total noise figure of the circuit increases. We verified (13) by noise simulations using the OpAmp circuit of Fig. 17. The NF is increased from 6 to 7.5 dB given that GM is equal to 20 mS. Note that it is also possible to apply the negative conductance in combination with an LNTA with higher GM and hence lower NF. In that case, the negative conductance can be lower, as $\mathrm{R_O} > 1/\mathrm{GM}$. However, then $\mathrm{IIP_3}$ of the LNTA becomes a bottleneck.

VI. Measurement Results and Benchmarking

Fig. 19 shows a photo of the implemented 65 nm IC. The active area is <0.2 mm^2 including the clock circuit. Thick metal was used for $\mathrm{R_{RF}}$ for high linearity and low spread.

The front-end achieves 26 dB gain (BalUn losses are de-embedded) at 1 GHz LO, over 24 MHz bandwidth (BW), 12 MHz on either side of LO. To demonstrate distortion cancelling, Fig. 20(a) shows the measured in-band $\mathrm{IIP_3}$ at 150 kHz tone spacing ($\mathrm{f_1} = 1004.1$ MHz and $\mathrm{f_2} = 1004.25$ MHz) vs. M. $\mathrm{IIP_3}$ clearly improves from around $+9$ dBm to $+21$ dBm!

The optimum $\mathrm{IIP_3}$ of $+21$ dBm is located at $\mathrm{M} = 32$, which fits to our theory $\mathrm{G_{Total}} = 1/\mathrm{R_O} + 1/\mathrm{R_F} = 1/1500 + 1/180 = 6.22$ mS so $\mathrm{M} = 6.22\ \mathrm{mS}/0.2\ \mathrm{mS} = 31$ very well. Fig. 20(b) shows the $\mathrm{IM_3}$ curves versus power for three cases: $\mathrm{M} = 0$ (off), $\mathrm{M} = 28$ (cancelling of $\mathrm{I_O}$, Fig. 6) and $\mathrm{M} = 32$ (overall optimum $\mathrm{IIP_3}$). Up to -22 dBm input power (note: this power is high for an in-band signal), $\mathrm{IM_3}$ improves. The rise of distortion for high input powers > -23 dBm is due to the clipping of the OpAmp output stage to its 1.2 V supply. The negative conductance was pushed to instability (i.e., latch-up of OpAmp output stage). This occurs at $\mathrm{M} = 45$ (see (8) $\Delta\mathrm{G} = \Delta\mathrm{M} \times 0.2$ mS), safely away from the optimum point by $\Delta\mathrm{M} = 45 - 32 = 13$. This shows a close agreement with our explanation in Section III and with the simulations in Fig. 21, which is done for the circuit of Fig. 13. One tone input signal with power of -16 dBm is used. Around this input power, the OpAmp output stage begins to clip. According to our simulation, the latch-up occurs for $\Delta\mathrm{M} \geq 14$. The same mechanism, discussed in Section II, of this technique also improves $\mathrm{IIP_2}$ by more than 10 dB as shown in Fig. 22 Table I compares/summarizes the $\mathrm{IIP_2}$ and $\mathrm{IIP_3}$ improvement for three M settings 0, 28 en 32. Note that the optimum linearity point will vary somewhat with Process, Voltage and Temperature (i.e., PVT). The analysis in this paper gives the relation between the required negative conductance and the resistance values $\mathrm{R_O}$ and $\mathrm{R_F}$, which can be a basis for designing an automatic PVT correction circuit.

Fig. 23 provides $\mathrm{IIP_3}$ curves versus the frequency offset $\Delta\mathrm{f}$, with fixed 3.95 MHz in-band $\mathrm{IM_3}$ position. The negative conductance clearly increases the $\mathrm{IIP_3}$ both in- and out-of-band

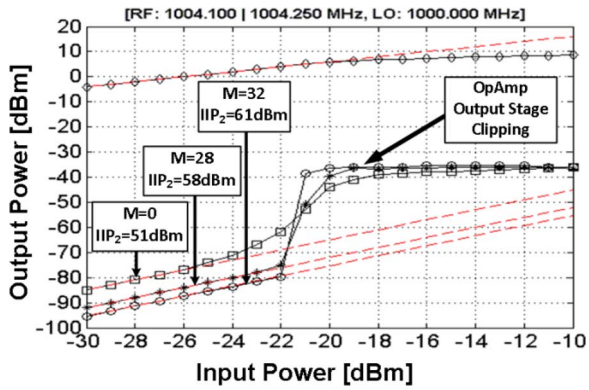

Fig. 22. Measurements: $\mathrm{IM_2}$ versus input power for three M settings, with $\mathrm{LO} = 1$ GHz.

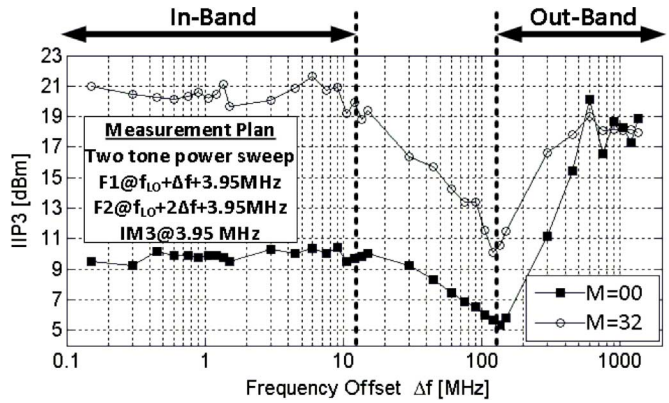

Fig. 23. 2-tone $\mathrm{IIP_3}$ measured at $\mathrm{IM_3} = 3.95$ MHz versus tone spacing Δf, with $\mathrm{LO} = 1$ GHz.

TABLE I
$\mathrm{IIP_2}$ AND $\mathrm{IIP_3}$ IMPROVEMENT

M	IIP2 [dBm]	IIP3 [dBm]
0	51	9.4
28	58.4	17
32	61.2	21

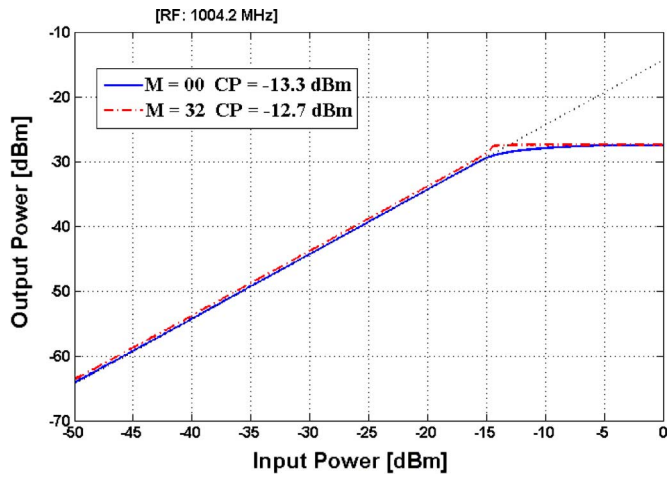

Fig. 24. Compression point.

(all-Band) with a worst case $\mathrm{IIP_3} > +10$ dBm. The reason behind less linearity improvement in the transition band can be understood considering the equivalent circuit earlier derived for stability analysis in Fig. 12. The negative conductance cancels only the loading of $\mathrm{R_O}$ and $\mathrm{R_F}$. However, $\mathrm{gm(s)}$, $\mathrm{C_F}$ and $\mathrm{C_T}$ introduce frequency dependences. Consequently, the "loading effect" on the VGND node (see Fig. 5) becomes frequency dependent and will introduce a phase shift compared with the (frequency independent) current generated by the negative conductance. This results in imperfect cancellation, i.e., less linearity improvement at high frequencies. This may be improved in the future by designing the negative conductance to be frequency dependent as well. Up to 10 MHz, in-band $\mathrm{IIP_3}$ is $> +20$ dBm, i.e., >10 dB improvement thanks to the negative conductance. Then the $\mathrm{IIP_3}$ declines from 12 MHz to 135 MHz, on the one hand because the OTA gain and hence its linearity degrades, but on the other hand also because the benefit from cancellation drops (the top line in Fig. 23 drops faster, versus Δf, than the bottom line). Note that the out-of-band $\mathrm{IIP_3}$ at $\Delta\mathrm{f} > 450$ MHz is again high, $+18$ dBm. This is because at high Δf (i.e., spacing between the carriers) the carriers are filtered due to the low pass filtering by $\mathrm{C_F}, \mathrm{R_F}$ and $\mathrm{C_O}$, hence less $\mathrm{IM_3}$ products. In this region the negative conductance doesn't result in any benefit anymore.

The compression point (CP) is around -13 dBm (hardly affected by M as shown in Fig. 24). Due to the virtual ground, $\mathrm{S_{11}}$ is hardly affected by the negative conductance and Fig. 25(a) shows that $\mathrm{S_{11}} < -25$ dB. Noise is more worrisome, but depending on the application some degradation may be acceptable, provided that the overall SFDR still improves (i.e., $\mathrm{IIP_3}$ in dBm should improve more than NF in dB degrades). Fig. 25(b) shows that NF increases from 6.2 dB at $\mathrm{M} = 0$ to 7.5 dB at $\mathrm{M} = 32$. This result is close to the NF prediction in the previous section. The 1/f corner was around 2 MHz.

The current consumption without the negative conductance at 1 GHz LO is 18 mA (including 8 mA of clock circuitry (i.e., on-chip drivers and divider)), and 1.6 mA more for $\mathrm{M} = 32$. The clock divider frequency range (i.e., also the receiving RF frequency) is 0.2–2.6 GHz, where it consumes 2.8–19 mA. The maximum gate-source voltage of the mixer switches is equal to the 1.2 V supply. The LO leakage to the RF port is less than -75 dBm. The optimum $\mathrm{IIP_3}$ has been measured for 5 samples. The optimum in-band $\mathrm{IIP_3}$ varies ± 1 dB around $+21$ dBm and the corresponding M varies ± 2 around $\mathrm{M} = 32$.

Table II benchmarks this work to other state-of-the-art receivers with high linearity and/or SFDR. Our front-end is more linear than [3] and [5], where active RF blocks are present. Even compared to the mixer-first designs [6], [7], we achieve better in-band $\mathrm{IIP_3}$ while our SFDR in 1 MHz of 85 dB is the highest.

VII. CONCLUSION

Due to the strong relationship between linearity and voltage swing, it is challenging to improve linearity in advanced CMOS technologies with low supply voltages. Architectures with RF V-I conversion followed by a passive mixers and an OTA-RC

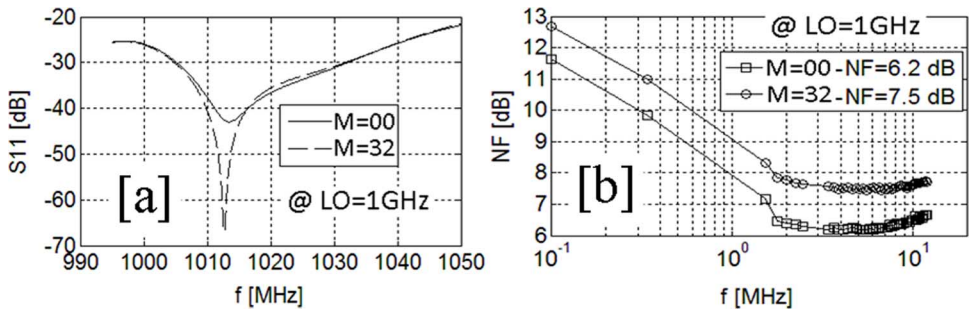

Fig. 25. Measurements (a) S_{11} (b) Noise Figure, with $\mathrm{LO} = 1$ GHz.

TABLE II
SUMMARY OF MEASUREMENT RESULTS AND COMPARISON TO OTHER STATE-OF-THE-ART RECEIVERS

	This work	Ru [3]	Murphy [4]	Youssef [5]	Soer [6]	Andrews [7]	units
Linearization Technique	Negative GO	Partial cancel Noise/Distortion	Cancel Noise	Freq. Translated Active feedback	Feedback + N-path filter	Feedback + N-path filter	
Matching	Switch-R	Common-gate	Switch-R	R	-	via TIA	
Mixer type	Switch-R	Switch-I	Switch-R&I	Gm + Switched-I	Switch-RC	Switch-RC	
Baseband-stage	TIA + RC	TIA+RC	TIA + RC	Inverter-RC	Voltage Amp	TIA+RC	
CMOS Techn.	65nm	65nm	40nm	65nm	65nm	65nm	
Active Area	< 0.2	< 1	1.2	< 0.06	< 0.13	0.75	mm2
RF Frequency	0.2-2.6	0.4-0.9	0.08-2.7	1.0-2.5	0.2-2.0	0.1-2.4	GHz
Gain	26.5	34	70	30	19	40-70	dB
In-band BW[1]	24	24	4	5	50	1.6	MHz
NF	7.5	4	2	7.25-8.9	6.5	4	dB
In-band IIP_3	**> +20**	+3.5	-22	-20	+11	-67	dBm
SFDR @ 1MHz bandwidth	**85**	75	60	57	79	29	dB
Wide-Band IIP_3 @2-tone Δf	≥+18 @ >450 >+10 @ All Δf	+18 @ Δf>800	+13.5 @Δf>40	> +12 @ Δf>60	Not measured	+25 @ Δf>50	dBm @ MHz
Supply Voltage	1.2	1.2	1.3	1.2	1.2	1.2 / 2.5	V
Power Consumption	13.9	39.6	15.6	62	60	< 70[2]	mW

[1] In-band BW is twice the zero-IF bandwidth around the LO frequency [2] Includes the clock circuitry

Transimpedance Amplifier perform relatively well. In such architectures, the OpAmp can become the bottleneck, especially for wide channel bandwidth, where the amount of loop gain available for negative feedback is limited. Still high linearity is wanted, not only out-of-band but also in-band, as RF-filtering often is ineffective for close-in interferers. This paper shows how virtual ground imperfections due to OTA nonlinearity lead to distortion currents, which can be cancelled exploiting a negative conductance in parallel to the virtual ground node. Although the technique results in slightly degraded noise figure from 6 to 7.5 dB the in-band IIP_3 (and IIP_2) is improved by much more (>10 dB), resulting in-band $\mathrm{SFDR} = 85$ dB in 1 MHz bandwidth.

APPENDIX A

In this section, a 3rd order Taylor approximation of V_{OUT} versus I_S (i.e., $V_{OUT} = V_{OUT}(I_S, I_S^3)$) of the transimpedance amplifier in Fig. 9 will be derived. The following procedure will be applied:

1. V_{OUT} is derived as a function of V_{VGND}, V_{VGND}^3 and $V_{OUT}^3 \rightarrow V_{OUT} = V_{OUT}(V_{VGND}, V_{VGND}^3, V_{OUT}^3)$.
2. The resulting relationship is rewritten as a function of V_{VGND} and V_{VGND}^3, by using the definition of the 3rd order Taylor coefficients $\rightarrow V_{OUT} = V_{OUT}(V_{VGND}, V_{VGND}^3)$.
3. The inverse function, V_{VGND} as a function of V_{OUT} and V_{OUT}^3, is written as a 3rd order Taylor function by using the procedure explained in [15] $\rightarrow V_{VGND} = V_{VGND}(V_{OUT}, V_{OUT}^3)$.
4. I_S is rewritten as a function of V_{VGND} and $V_{OUT} \rightarrow I_S = I_S(V_{VGND}, V_{OUT})$.
5. Substituting V_{VGND} of step 3 in I_S of step 4 makes I_S to be a function of V_{OUT} and $V_{OUT}^3 \rightarrow I_S = I_S(V_{OUT}, V_{OUT}^3)$.
6. Finally, by repeating the procedure explained in [15], the function of step 5 is inversed to obtain V_O as a function of I_S and $I_S^3 \rightarrow V_{OUT} = V_{OUT}(I_S, I_S^3)$.

Step 1 $\rightarrow V_{OUT} = V_{OUT}(V_{VGND}V_{VGND}^3, V_{OUT}^3)$: We begin the derivation by expressing the feedback current I_F at the VGND node and the OUT node (see Fig. 9) as follows:

$$\text{At VGND node}: \; I_F = \frac{V_{VGND}}{R_{F-VGND}} + G_{F-VGND}V_{OUT} \tag{14}$$

$$\text{At OUT node}: \; I_F = -\frac{V_{OUT}}{R_{F-OUT}} - G_{F-OUT}V_{VGND} \tag{15}$$

Referring to the OpAmp nonlinear model, we equate the I_F in (1) to I_F in (15) as follows:

$$\begin{aligned} &gm_1 V_{VGND} + gm_3 V_{VGND}^3 + go_1 V_{OUT} + go_3 V_{OUT}^3 \\ &\quad = -\frac{V_{OUT}}{R_{F-OUT}} - G_{F-OUT} V_{OUT} \\ &V_{OUT} = \underbrace{-\frac{(gm_1 + G_{F-OUT})}{\left(go_1 + \frac{1}{R_{F-OUT}}\right)}}_{a} V_{VGND} \\ &\quad \underbrace{-\frac{gm_3}{\left(go_1 + \frac{1}{R_{F-OUT}}\right)}}_{b} V_{VGND}^3 \underbrace{-\frac{go_3}{\left(go_1 + \frac{1}{R_{F-OUT}}\right)}}_{c} V_{OUT}^3 \end{aligned} \tag{16}$$

Step 2 $\rightarrow V_{OUT} = V_{OUT}(V_{VGND}, V_{VGND}^3)$: V_{OUT} is defined as: $V_{OUT} = \beta_1 V_{VGND} + \beta_2 V_{VGND}^2 + \beta_3 V_{VGND}^3$, which is a 3rd order Taylor approximation around $V_{VGND} = 0$, where β_1, β_2 and β_3 are the Taylor coefficients:

$$\beta_{n=1,2,3} = \frac{1}{n!} \left(\frac{\partial^n V_{OUT}}{\partial V_{VGND}^n}\right)\Bigg|_{V_{VGND}=0}$$

To derive β_1, we differentiate (16) with respect to V_{VGND} as follows:

$$\begin{aligned} \frac{\partial V_{OUT}}{\partial V_{VGND}} &= a + 3bV_{VGND}^2 + 3cV_{OUT}^2 \frac{\partial V_{OUT}}{\partial V_{VGND}} \Rightarrow \frac{\partial V_{OUT}}{\partial V_{VGND}} \\ &= \frac{a + 3bV_{VGND}^2}{1 - 3cV_{OUT}^2} \\ \therefore \beta_1 &= \left(\frac{\partial V_{OUT}}{\partial V_{VGND}}\right)\Bigg|_{V_{VGND}=0} \\ &= a = -\frac{(gm_1 + G_{F-OUT})}{\left(go_1 + \frac{1}{R_{F-OUT}}\right)} \end{aligned}$$

The same procedure is used to derive β_2 and β_3:

$$\begin{aligned} \beta_2 &= \frac{1}{2}\left(\frac{\partial^2 V_{OUT}}{\partial V_{VGND}^2}\right)\Bigg|_{V_{VGND}=0} = 0 \text{ and} \\ \beta_3 &= \frac{1}{6}\left(\frac{\partial^3 V_{OUT}}{\partial V_{VGND}^3}\right)\Bigg|_{V_{VGND}=0} = b + a^3 c \\ V_{OUT} &= \underbrace{a}_{\beta_1} V_{VGND} + \underbrace{(b + a^3 c)}_{\beta_3} V_{VGND}^3 \end{aligned} \tag{17}$$

Step 3 $\rightarrow V_{VGND} = V_{VGND}(V_{OUT}, V_{OUT}^3)$: We write the inverse of (17) in the Taylor series form: $V_{VGND} = \alpha_1 V_{OUT} + \alpha_2 V_{OUT}^2 + \alpha_3 V_{OUT}^3$. Deriving α_1, α_2 and α_3 can be done by the procedure below.

First, let us substitute (17) into its abovementioned inversed form as follows:

$$\begin{aligned} V_{VGND} &= \alpha_1 \left(\beta_1 V_{VGND} + \beta_3 V_{VGND}^3\right) \\ &+ \alpha_2 (\beta_1 V_{VGND} + \beta_3 V_{VGND}^3)^2 + \alpha_3 (\beta_1 V_{VGND} + \beta_3 V_{VGND}^3)^3 \end{aligned}$$

By equating the right to the left side of the equation above [15], the coefficients α_1, α_2 and α_3 are derived:

$$V_{VGND} = \underbrace{\frac{1}{a}}_{\alpha_1} V_{OUT} \underbrace{-\frac{(b + a^3 c)}{a^4}}_{\alpha_3} V_{OUT}^3 \tag{18}$$

Step 4 $\rightarrow I_S = I_S(V_{VGND}, V_{OUT})$: Referring to I_S in Fig. 9, we substitute the I_F (14) at the VGND node in the following equation:

$$\begin{aligned} I_S = I_O + I_F &= \left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right) V_{VGND} \\ &\quad + G_{F-VGND} V_{OUT} \end{aligned} \tag{19}$$

Step 5 $\rightarrow I_S = I_S(V_{OUT}, V_{OUT}^3)$: By substituting (18) into (19), the following equation is obtained:

$$\begin{aligned} I_S &= \left[\frac{1}{a}\left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right) + G_{F-VGND}\right] V_{OUT} \\ &\quad - \frac{(b + a^3 c)}{a^4}\left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right) V_{OUT}^3 \end{aligned} \tag{20}$$

Step 6 $\rightarrow V_{OUT} = V_{OUT}(I_S, I_S^3)$: Finally, by inversing (20), we reach (21), shown at the bottom of the page, where $NL_3 = ((b + a^3 c))/(a^4)$ is related to the nonlinear terms of the OpAmp model.

Appendix B

In this section, the relation between V_{VGND} and I_S is derived to be used in the latch-up analysis section. In order to simplify this analysis, we assume a linear OpAmp (i.e., $gm_3 = go_3 = 0$). Consequently, (16) and (21) can be simplified as follows:

$$V_{VGND} = \frac{1}{a} V_{OUT} \tag{22}$$

$$V_{OUT} = \Omega_1 I_S \tag{23}$$

$$\boxed{V_{OUT} = \underbrace{\frac{1}{\left[\frac{1}{a}\left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right) + G_{F-VGND}\right]}}_{\Omega_1} I_S + \underbrace{\frac{NL_3 \left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right)}{\left[\frac{1}{a}\left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right) + G_{F-VGND}\right]^4}}_{\Omega_3} I_S^3} \tag{21}$$

Combining (22) and (23), gives the following relation:

$$V_{VGND} = \frac{\Omega_1}{a} I_S = \frac{1}{\left[\left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right) + a\, G_{F-VGND}\right]} I_S \tag{24}$$

After that the negative conductance cancels the loading effect of R_O on the VGND node, it injects current via R_F that needs to be handled by the OpAmp output stage (see Figs. 13 and 17). Now if the negative conductance becomes too strong then the potential latch-up becomes a real risk. For the case of latch-up, (24) can be further elaborated to obtain the following equation:

$$V_{VGND} = \frac{1}{\left[\left(\frac{1}{R_{F-VGND}} - G_{Latch-up}\right) + a\, G_{F-VGND}\right]} I_S \tag{25}$$

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REFERENCES

[1] 3GPP TS 36.104:, "Evolved universal terrestrial radio access (E-UTRA); Base station (BS) radio transmission and reception," [Online]. Available: http://www.3gpp.org

[2] D. H. Mahrof, E. A. M. Klumperink, J. Haartsen, and B. Nauta, "On the effect of spectral location of interfererson linearity requirements for wideband cognitive radio receivers," in *IEEE Symp. New Frontiers in Dynamic Spectrum Access Networks (DySPAN)*, Apr. 2010, pp. 1–9.

[3] Z. Ru, E. A. M. Klumperink, and B. Nauta, "A software-defined radio receiver architecture robust to out-of-band interference," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 230–231.

[4] D. Murphy, A. Hafez, A. Mirzaei, M. Mikhemar, H. Darabi, M. F. Chang, and A. Abidi, "A blocker-tolerant wideband noise-cancelling receiver with a 2 dB noise figure," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 74–76.

[5] S. S. T. Youssef, R. A. R. van der Zee, and B. Nauta, "Active feedback receiver with integrated tunable RF channel selectivity, distortion cancelling, 48 dB stop-band rejection and > + 12 dBm wideband IIP3, occupying < 0.06 mm^2 in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 166–168.

[6] M. C. M. Soer, E. A. M. Klumperink, Z. Ru, F. E. van Vliet, and B. Nauta, "A 0.2-to-2.0 GHz 65 nm CMOS receiver without LNA achieving >11 dBm IIP3 and <6.5 dB NF," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 222–223.

[7] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.

[8] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "The Blixer, a wideband balun-LNA-I/Q-mixer topology," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2706, 2715, Dec. 2008.

[9] D. H. Mahrof, E. A. M. Klumperink, M. S. Oude Alink, and B. Nauta, "A receiver with in-band IIP3 > 20 dBm, exploiting cancelling of OpAmp finite-gain-induced distortion via negative conductance," in *IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, 2013, pp. 601–604.

[10] J. Deguchi *et al.*, "A fully integrated 2 × 1 dual-band direct-conversion mobile WiMAX transceiver with dual-mode fractional divider and noise-shaping transimpedance amplifier in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2774–2784, Dec. 2010.

[11] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ, USA: Prentice Hall, 1998.

[12] Z. Ru, "Frequency translation techniques for interference-robust software-defined radio receivers," Ph.D. dissertation, Univ. Twente, Enschede, The Netherlands, 2009.

[13] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Noise cancelling in wideband CMOS LNAs," in *IEEE ISSCC Dig. Tech. Papers*, 2002, pp. 406–407.

[14] W. Redman-White and D. M. W. Leenaerts, "1/f noise in passive CMOS mixers for low and zero IF integrated receivers," in *Proc. ESSCIRC*, 2001, pp. 18–20.

[15] E. A. M. Klumperink, "Transconductance based CMOS circuits" Ph.D. dissertation, Univ. Twente, Enschede, The Netherlands, 1997 [Online]. Available: http://jive.el.utwente.nl/home/erick/Klumperink-PhD-Thesis.pdf?

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