Introduction to the Special Section on the 2013 IEEE Bipolar/BiCMOS Circuits and Technology Meeting

THIS Special Section of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is a selection of papers presented at the 2013 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) held from September 30th to October 3rd in Bordeaux, France. The five papers selected reflect the recent advances in IC designs implemented in BiCMOS and SiGe technologies.

The Special Section starts with the paper by El-Chammas *et al.*, which depicts a 12 bit 1.6 GS/s pipeline ADC designed in a 18 nm SiGe BiCMOS, consisting of a 4-way time-interleaved hierarchical structure and a master-slave T/H for improved dynamic performance of sub-ADCs and reduced error rate, resulting in SFDR of 79 dBc and 66 dBc at low/high frequency inputs.

The second paper, by Ritter *et al.*, reports a 6 bit 20 Gs/s flash ADC implemented in a SiGe BiCMOS process featuring a new comparator placing scheme and reference ladder concept to minimize the dynamic reference voltage distortions at high speed. No track-and-hold was used in the ADC, which helps to reduce design complexity and the conversion latency. It achieves an effective resolution 3.7 bits up to 10 GHz signal frequency and 20 GS/s sampling without calibration.

In the third paper, Béraud-Sudreau *et al.* present a 100 Gb/s CDR designed in 130 nm SiGe BiCMOS technology. The key feature is the use of an injection locked oscillator to deliver the 100 GHz clock. In measurement, a 100 GHz clock was extracted from 50 Gb/s input data.

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The fourth paper, presented by Yu *et al.*, describes an X-band chirp radar transceiver with bandwidth reduction for range detection that was designed in a 130 nm SiGe process. It has a Weaver receiver including an ADC, a direct-digital synthesizer based transmitter and a PLL synthesizer. A modified Weaver architecture was used featuring dual downconversions to convert the X-band chirp signal to the baseband signal, which contributes to reduced power and bandwidth without range resolution degradation. The chip consumes 326 mW and 333 mW in receiving and transmitting modes, respectively.

The Special Section concludes with a paper by Elkhouly *et al.*, which presents a 220–245 GHz 4-way Butler Matrix chip designed in a 130 nm SiGe BiCMOS process. The chip includes four 230 GHz amplifiers and a SP4T switch to select the four outputs of a beam-forming network. It exhibits 0 dB of insertion gain and consumes 104 mA at 3.3 V.

The Guest Editor appreciates the authors for their hard work in preparing and revising their manuscripts. The Editor also wishes to express his deepest gratitude to the reviewers for their efforts and dedication to conduct the serious reviews within a short time period. This Special Section would not have been possible without their expert advice.

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Albert Wang (A'95–M'97–SM'00–F'09) received the B.S.E.E. degree from Tsinghua University, China, and the Ph.D. E.E. degree from The State University of New York at Buffalo in 1985 and 1996, respectively.

He was with National Semiconductor Corporation during 1995 to 1998. From 1998 to 2007, he was a Professor of electrical and computer engineering at the Illinois Institute of Technology, Chicago, IL, USA. Since 2007, he has been a Professor of electrical and computer engineering at the University of California, Riverside, CA, USA, where he is Director for the Laboratory for Integrated Circuits and Systems and Director for the University of California System-wide Center for Ubiquitous Communications by Light (UC-Light). His research interests focus on analog/mixed-signal/RF ICs, integrated design-for-reliability, IC CAD and modelling, systems-on-a-chip, and emerging nano devices and circuits.

Prof. Wang received the CAREER Award from the National Science Foundation in 2002. He is the author of the book "On-Chip ESD Protection for Integrated Circuits" (Kluwer, 2002) and about 200 peer-reviewed papers in the field, and he holds seven U.S. patents. He has served as Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, Editor for IEEE ELECTRON DEVICE LETTERS, Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, Guest Editor-in-Chief for the IEEE TRANSACTIONS ON ELECTRON DEVICES and Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS. He is an IEEE Distinguished Lecturer for the Electron Devices Society and the Circuits and Systems Society, and was an IEEE Distinguished Lecturer for the Solid-State Circuits Society. He is President of the IEEE Electron Devices Society for 2014–2015, and Chair of the IEEE CAS Analog Signal Processing Technical Committee (ASPTC). He is a committee member of the SIA International Technology Roadmap for Semiconductor (ITRS) and the IEEE VLSI Technology and Circuits Committee. He is a TPC co-Chair and General Chair for IEEE RFIC Symposium (2014–2016) and served as a committee member for many IEEE conferences, including IEDM, BCTM, ASICON, IEDST, ICSICT, CICC, RFIC, APC-CAS, ASP-DAC, ISCAS, IPFA, ICEMAC, NewCAS, ISTC, IRPS, AP-RASC, MAPE, EDSSC, and MIEL. He is a Fellow of IEEE and a Fellow of AAAS.