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A Wearable 8-Channel Active-Electrode EEG/ETI Acquisition System for Body Area Networks

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Abstract—This paper describes an 8-channel gel-free EEG/electrode-tissue impedance (ETI) acquisition system, consisting of nine active electrodes (AEs) and one back-end (BE) analog signal processor. The AEs amplify the weak EEG signals, while their low output impedance suppresses cable-motion artifacts and 50/60 Hz mains interference. A common-mode feed-forward (CMFF) scheme boosts the CMRR of the AE pairs by 25 dB. The BE post-processes and digitizes the analog outputs of the AEs, it also can configure them via a single-wire pulse width modulation (PWM) protocol. Together, the AEs and BE are capable of recording 8-channel EEG and ETI signals. With EEG recording enabled, ETIs of up to 60 k Ω can be measured, which increases to 550 k Ω when EEG recording is disabled. Each EEG channel has a 1.2 G Ω input impedance (at 20 Hz), 1.75 μ Vrms (0.5-100 Hz) input-referred noise, 84 dB CMRR and $\pm$ 250 mV electrode offset rejection capability. The EEG acquisition system was implemented in a standard 0.18 μ m CMOS process, and dissipates less than 700 μ W from a 1.8 V supply.

Index Terms—chopper amplifier, active electrode, dry electrode, EEG monitoring, electrode-tissue impedance.

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I. INTRODUCTION

The use of dry biopotential electrodes is becoming increasingly popular in personal healthcare applications and in brain-computer-interfaces [1]-[3]. Dry-electrodes eliminate the need for gel/wet electrodes and enable long-term monitoring of brain activity in a user-friendly manner. However, they exhibit significant and variable electrode-tissue impedance (ETI) [4], which means that the cables connecting the electrodes to the readout circuitry can induce motion related artifacts and mains interference [5], thus severely degrading signal quality.

A potential solution to this problem is to bring the readout circuit closer to the electrodes by implementing so-called active electrodes (AEs) with co-integrated pre-amplifiers [6]-[9]. The short connection between electrode and pre-amplifier minimizes noise pick-up, while the pre-amplifier's low output impedance suppresses cable motion artifacts, eliminating the need for shielded wires [5]. Analog buffers have widely been used in AEs, but they only provide the impedance conversion [6], which means that the following circuits must still be designed for low noise. Alternatively, the use of pre-amplifiers with gain significantly relaxes the noise requirement of the succeeding circuits, and thus the overall system power [7]. Pre-amplification also improves the robustness of the AE's output signal to cable interference.

As shown in Table I, however, a robust gel-free EEG monitoring system must also satisfy other challenging requirements [10][11]. To start with, it must be able to cope with large variations in skin-electrode impedance, usually by employing a very high input-impedance pre-amplifier to minimize signal attenuation [12]. Another challenge is the electrode polarization voltage, which can be as large as a few hundreds of mV and

which may reduce the pre-amplifier's headroom or even saturate its output. The pre-amplifier should also be able to handle such DC voltages and maintain its performance. Furthermore, high common-mode rejection ratio (CMRR) is needed to reject mains interference. Since each AE processes signals from one electrode, this can only be achieved by ensuring that any two pre-amplifiers will have well-matched gains. In multi-channel applications, each AE should also employ a minimal number of connecting cables to the outside world in order to reduce the overall cable weight. Last, but not least, the system should consume ultra-low power to maximize battery-life.

This paper presents a low-power 8-channel active-electrode-based EEG/ETI acquisition system [13] to address the aforementioned challenges (Fig. 1). A high input-impedance, low-noise, AC-coupled AE enables the use of dry-electrodes. The CMRR between any two AEs is enhanced by 25 dB through the use of a common-mode feed-forward (CMFF) scheme. A low-power and highly-configurable BE performs analog signal processing and analog-to-digital conversion. A 6-wire interface between the AEs and the BE utilizes a single-wire data communication scheme based on pulse width modulation (PWM), thus reducing the number of cables between each AE and the BE. The other wires are mainly used for power supply and extra functions of the AE, such as synchronized electrode-tissue impedance (ETI) measurements, re-configurability, and CMRR enhancement. The system continuously monitors ETI to facilitate the remote assessment of electrode status and impedance-based motion artifact removal (MAR) [14].

The paper is organized as follows: Section II describes the architecture and system-level highlights. Section III and IV discuss the detailed implementation of the AE and the BE, respectively. Section V presents the results of system characterization and a comparison

table. Section VI describes an integrated wireless EEG headset implemented with the proposed system, and presents the results of gel-free EEG measurement. Section VII concludes the paper.

II. SYSTEM ARCHITECTURE OVERVIEW

The complete 8-channel EEG/ETI acquisition system consists of nine AEs and one BE (Fig. 2). A bipolar measurement can be implemented by taking difference between outputs of two AEs. Each AE chip is responsible for providing high-input impedance, EEG/ETI pre-amplification and electrode offset (EO) rejection. The AE chips receive a 32 kHz master clock (CLK), power supply (VDD and VSS), and digital control bits (PWM) from the BE. They then output analog EEG/ETI signals (ANA) and a common-mode feed-forward (CMFF) signal. Each AE chip utilizes a non-inverting amplifier, equipped with a ripple reduction loop (RRL) to reject chopper ripple [15], and a DC-servo loop (DSL) to reject electrode offset [16]. A built-in AC current source generates a square-wave current that can be injected into the body for ETI measurement [17].

The BE chip is responsible for analog signal processing and digitization. As shown in Fig. 2, the BE employs chopper instrumentation amplifiers, including transconductance (TC) stages to acquire the differential analog outputs from two AEs, and transimpedance (TI) stages to demodulate and separate the EEG signal and complex ETI signals into three channels. After programmable gain amplifiers (PGA), anti-aliasing low-pass filters (LPF), both EEG channel and ETI channels are simultaneously sampled at 500 Hz by sample and hold (S/H) stages. The total 24-channel outputs (8-channel EEG and 16-channel ETI) are multiplexed and digitized by two 12 bit SAR ADCs operating at 1 kSps per channel.

A. EEG and ETI measurement

The system can simultaneously measure EEG and ETI signals (Fig. 3). A DC current (I_{DC}) is up-modulated to the ETI measurement frequency ($f_I = 1$ kHz), and injected into the subject through the biopotential electrodes. This AC current is converted into an AC voltage (ETI_{in}) over the ETI. As a result, the EEG and ETI signals are both present at the input of AE, but are located in different frequency bands. At the output of the EEG channel, the amplified EEG signal is still at baseband, and the ETI signal at f_I can easily be removed by a LPF. On the other hand, ETI-I/Q channel up-modulates the EEG signal to f_I and filters it out, while it demodulates in-phase f_I (0°) and quadrature f_I (90°) components of the ETI_{in} signal back to DC, respectively.

B. CMFF for CMRR enhancement

Gain mismatch typically limits the intrinsic CMRR of a pair of AEs to less than 60 dB. Conventionally, the driven-right-leg (DRL) technique [18] improves CMRR by feeding a CM-canceling signal to the subject's body. This effectively reduces the CM gain and boosts the CMRR. However, the large and uncontrolled ETI of dry electrodes makes such a loop difficult to stabilize. The digitally-assisted DRL technique reported in [19] solves this problem by ensuring that the DRL loop only has gain at the power line frequency, but this is at the expense of additional notch filtering and hence power dissipation. The common-mode feedback (CMFB) technique [7], improves CMRR by feeding the CM signal back to the input of each pre-amplifier. However, the feedback loop requires a summing amplifier and large compensation capacitors for CM extraction and stability, leading to increased area and power consumption.

This work utilizes a CMFF technique for CMRR improvement of multiple AEs [20].

Conventionally, the CMFF nodes of all AEs are connected to ground as reference (Fig. 4a). As a result, the CMRR of a pair of AEs is limited by their gain error, as shown in (1). In CMFF scheme, all CMFF nodes are capacitively connected together to a well-defined DC voltage V_{bias} via a very large bias resistor R_b (Fig. 4b). As a result, CMFF becomes an averaging node of all input signals, i.e. the CM input. It is superimposed on V_{bias} , and no CM current flows through C_{11} and C_{21} . This effectively reduces the CM gain and increases the CMRR of the AE pair, as shown in (2), where G_{AE} is the voltage gain of an AE, and ΔG_{AE} is the gain difference of two AEs.

$$CMRR = 20 \cdot \log \left(\frac{G_{AE}}{\Delta G_{AE}} \right) \quad (1)$$

$$CMRR' = CMRR + 20 \cdot \log \left(1 + \frac{R_b}{sC_1} \right) \quad (2)$$

Ideally, increasing R_b will make CMFF node voltage sensitive to leakage due to the voltage divider formed by R_b and the parasitic resistance R_p (Fig. 4b). Making R_b too large will significantly reduce the DC voltage at CMFF node, thus limiting the maximum CM swing at this node. Therefore, the maximum DC voltage at the CMFF node should be larger than the AE's maximum input CM voltage ($V_{in,pk}$), as given by

$$V_{DC,CMFF} = V_{bias} \cdot \frac{R_p}{R_p + R_b} > |V_{in,pk}| \quad (3)$$

However, decreasing R_b will limit the maximum CMRR improvement, as shown in (2).

This increases the effective high-pass corner of CMFF node, and thus prevents any CM voltage extraction at the CMFF node, e.g. when $R_b = 0$, the CMFF will be biased to ground and the CMFF scheme will stop working. Therefore, $V_{bias}=1.8$ V and $R_b=100$ M Ω are selected to accommodate a CMFF dynamic range up to 50 mV.

The lead-off of any electrode will cause the failure of the CMFF loop, as the floating input of the amplifier pollutes the CM averaging [20]. This problem can be solved by connecting the input of each amplifier to a bias voltage (0.9 V) through a large bias resistor (for instance, 1 G Ω). This will bias the amplifiers in the lead-off condition, while CMFF is then performed among the other amplifiers.

C. PWM communication

The AE receives configuration data to define the gain of the IA, the amplitude and frequency of the AC current source. Data communication between the BE and AE could be done via a 3-wire serial-to-parallel interface (SPI). However, in a multi-channel system, this may lead to an increased number of wires. The system employs a single-wire self-clocked PWM data transmission scheme [21], which reduces the total number of wires required between each AE and the BE from eight to six.

III. ACTIVE ELECTRODE ASIC

A. Instrumentation Amplifier (IA)

As the first stage of the signal chain, the IA consists of a non-inverting AC-coupled chopper amplifier (Fig. 5), which provides voltage gain, high input-impedance, low noise, as well as the capability to reject large electrode offset.

Input Impedance: The use of non-inverting amplifier achieves much higher AC input impedance than inverting amplifiers [7] [16], although chopper modulation and large C_I are utilized in both topologies. The input impedance is dominated by the parasitic switched-capacitor resistance ($>2\text{G}\Omega@20\text{Hz}$) associated with the input chopper and the amplifier's input capacitance, in parallel with the output resistance $R_{out,DC}$ of the current source ($>3.2\text{G}\Omega@20\text{Hz}$).

$$Z_{in} = \left(\frac{1}{2f_c C_p} + \frac{1}{sC_1} \right) // R_{out,IS} \quad (4)$$

Electrode Offset Rejection: To reject large electrode offset (EO), which may saturate the pre-amplifier, the AE implements a continuous-time DC-servo loop (DSL) [16]. The DSL stabilizes the output DC voltage to a reference voltage (V_{ref}) via an active RC integrator, which feeds IA's output offset back to its inverting input via a large pseudo resistor (R_s) [22]. The settling time of the DSL is about 20 seconds, which is dominated by R_{int} and C_{int} . The maximum electrode offset rejection of each AE, i.e. ± 250 mV with respect to subject bias, is ultimately determined by the input biasing range of the core amplifier.

Noise Analysis: The target input-referred noise of EEG channel (including two AEs and BE) is $75\text{nV}/\sqrt{\text{Hz}}$. Neglecting the noise contribution from the BE, the input-referred noise of a single AE should be about $53\text{nV}/\sqrt{\text{Hz}}$, which comes from three major contributors (Fig. 6): the core amplifier, the ripple reduction loop (RRL), and the DC-servo loop (DSL).

$$\overline{V_{ni,AE}^2} = \overline{V_{ni,IA}^2} + \overline{V_{ni,RRL}^2} + \overline{V_{ni,DSL}^2} \quad (5)$$

The noise contribution of the core IA can be expressed by:

$$\overline{V_{ni,IA}^2} = \overline{V_{ni,OP1}^2} \cdot \left[1 + \frac{C_2}{C_1} + \left(\frac{f_c}{f_{in}} + 1 \right) \frac{C_p}{C_1} \right]^2 + \overline{I_{ni,OP1}^2} \cdot \left(\frac{1}{2\pi f_{in} C_2} \right)^2 \quad (6)$$

Where $V_{ni,OP1}$ and $I_{ni,OP1}$ are the input-referred voltage density and current noise density of the core amplifier, respectively. C_1 and C_2 are feedback capacitors which define the gain of the active electrode. f_c is the operating frequency of the chopper modulators. f_{in} is the frequency of the EEG input signal. C_p is the input parasitic capacitance of the core amplifier.

The first component in (6) refers to the $1/f^2$ voltage noise of the non-inverting chopper amplifier due to its parasitic switched-capacitor resistance [7]. Although chopper modulation mitigates $1/f$ noise of the core amplifier ($OP1$), this parasitic resistance reduces the input impedance of the amplifier and increases its equivalent current noise. This results in $1/f^2$ voltage noise in the presence of external capacitive feedback. The second component in (6) refers to another equivalent $1/f^2$ voltage noise source associated with the current noise $I_{ni,OP1}$, which is due to the charge injection and clock feed-through of the input chopper MOSFETs [23]. The current noise PSD linearly increases with the chopping frequency [24] and induces significant $1/f^2$ voltage noise when chopping is performed at a high-impedance node [23].

The proposed IA employs several approaches to minimize the total noise in (6). In order to reduce the thermal noise of $V_{ni,OP1}$, the core amplifier employs a two-stage amplifier (Fig.

7), whose input pair consists of NMOS and PMOS differential pairs connected in parallel [25]. This approach doubles the input transconductance of the core amplifier without consuming extra bias current, while still achieving an input DC range from 0.7 V to 1.2 V. In order to reduce $I_{ni, OPI}$, a relatively low chopping frequency ($f_c = 2$ kHz) and transistors of the chopper modulators are implemented minimum size [23]. Besides, the use of a non-inverting topology means its input impedance is not dominant by the feedback capacitors. As a result, very large feedback capacitors C_1 (5 nF) and C_2 (50 pF to 500 pF) were used to reduce the impedance at the chopping node, thus leading to less $1/f^2$ voltage noise in (6) without compromising IA's input impedance. This solves the tradeoff between noise and input impedance in previous AC-coupled inverting chopper IAs [7][16], where large coupling capacitors significantly reduced the IA's AC input impedance. In this work, both C_1 and C_2 were implemented with $2 \text{ fF}/\mu\text{m}^2$ metal-metal capacitor with common-centroid layout and dummies to improve their matching, since the AE's gain mismatch limits their CMRR.

The RRL's noise contribution is negligible, since it is located between the two choppers of the core amplifier (*OPI*). The $1/f$ noise from *GM2* and current buffer (*CB*) are effectively chopped out, while their thermal noises are suppressed by the input stage of *OPI*. The DSL does not induce significant noise in the EEG bandwidth either, as its low-pass corner frequency is well below 0.5 Hz.

B. Current Source for ETI Measurement

The current source employs a self-biased triple-cascode architecture to boost its output impedance ($>3.2\text{G}\Omega@20\text{Hz}$) (Fig. 8). The magnitude of the reference current (I_{dc}) is configurable from 10 nA to 2 μA . This current is mirrored either to a NMOS or PMOS

triple-cascode stage, enabling either current injection or current sink. An output chopper then generates a square-wave current and sets the ETI measurement frequency ($f_I=1$ kHz).

IV. BACK-END SIGNAL PROCESSING ASIC

A. Instrumentation Amplifiers (IA)

The EEG channel and two ETI channels use the same IA architecture, but with different chopping schemes to separate EEG and ETI from each other. The IA of the EEG channel utilizes both input and output choppers to reduce its $1/f$ noise. Two ETI channels share the same TC stage to reduce power dissipation, and only implement output choppers in their TI stages to demodulate the ETI signal back to baseband.

The IA is based on a current-balancing instrumentation amplifier [26] (Fig. 9). The TC stage employs input voltage followers, so the differential input voltage applies across the input resistor R_i and creates a signal dependent current. This current is mirrored (P_8 and P_6) to the TI stage and converted back to a voltage via resistor R_o . The voltage gain of the IA is given by

$$G_{IA} = \frac{R_o}{R_i} \left(\frac{W_6 / L_6}{W_2 / L_2} \right) \quad (7)$$

The level shifters (P_3 and P_4) help to keep the voltages V_{on} and V_{op} at reasonable values for a wide range of input common-mode voltages. The maximum input swing of the IA is determined by $R_i * I_b$.

B. Low-Pass Filter and ADC

The anti-aliasing LPFs separate the EEG signal and the residual ETI signal (at 1 kHz), and reject chopping spikes. The LPF is a 4th-order unity-gain Bessel filter realized with a Sallen-Key topology [27], which provides tunable bandwidth (100 Hz to 300 Hz), as well as sufficient attenuation (>60 dB at 1 kHz) of residual ETI signal. The use of a Bessel filter ensures that the EEG and ETI channels all have a constant group delay of about 1 ms. The sample and hold circuit samples all channels at the same time. Both constant group delay and synchronized sampling improve the accuracy of temporal correlation across channels. This is important for brain-computer-interface applications, such as ETI-based motion artifact reduction [14].

Two time-multiplexed 12 bit SAR ADCs, conceptually similar to the ones used in [28], digitize all analog outputs (EEG, ETI-I and ETI-Q from 8 channels), at 1 kSps per channel.

V. MEASUREMENT SUMMARY

A. Measurement of Performance

The system is implemented in a standard TSMC 0.18 μm CMOS process. Fig. 10 shows the photographs of both chips and the packaged AE placed on an 11 mm diameter electrode. The 8-channel system, including nine AEs and one BE, consumes less than 700 μW from 1.8 V. Table II shows the power breakdown of the 8-channel system.

Fig. 11 shows the original PWM data sent from the BE, and the demodulated serial data received by the AE. It can be seen that the PWM demodulation scheme works properly.

Fig. 12 shows the measured voltage gain of one EEG channel, with various PGA gain settings (3, 9, 12 and 18). The measured bandwidth of 200 Hz is determined by the LPF.

Fig. 13 shows the measured input impedance of an AE, which is about 1.2 G Ω at 20 Hz and above 300 M Ω at 50 Hz.

Fig. 14 shows the input-referred noise density of one EEG channel (including two AEs and one BE) versus frequency. When chopping is disabled, $1/f$ noise is clearly visible; when chopping is enabled at 2 kHz, $1/f^2$ noise dominates below 20 Hz. Above this frequency, the input noise-density is about 75 nV/sqrt(Hz). The integrated input-referred noise is 1.75 μ Vrms from 0.5 Hz to 100 Hz.

Fig. 15 shows the CMRR of one EEG channel (including two AEs and one BE). Enabling the CMFF improves the CMRR by 25 dB at 50 Hz. Fig. 16 shows that the measured CMRR of 7 pairs of AEs is always above 84 dB.

Fig. 17 shows the AE's output voltage as a function of time. When a transient electrode offset of 200 mV is applied to the input of AE, its output first saturates and then recovers in about 20 seconds.

Fig. 18 and Fig. 19 show the measured ETI resistance and capacitance, respectively. Test resistors and capacitors were connected to the inputs of two AEs. The gain of the AE and BE were set to 101 and 9, so that both the EEG and ETI channels have the same gain (≈ 900). In this default setting, the maximum differential ETI that the system can linearly measure is approximately 60 k Ω or 2 nF (at $f_I = 1$ kHz). This is limited by the output swing of the PGA in the BE (0.35 V-1.45 V), and the amplitude of the injected current (10 nA). By lowering the gains of the AE and BE to 11 and 9, respectively, ETIs of up to 550 k Ω can be measured, at the expense of less gain (≈ 100) in the EEG channel. In principle, even larger ETIs can be measured by lowering the amplitude of the injected current.

Table III summarizes the performance of the proposed AE system and compares it with

state-of-the-art AE-based implementations. Compared to these, the proposed 8-channel AE system is able to measure EEG and ETI signals simultaneously, while still achieving very competitive performance, in terms of input impedance, input referred noise, electrode offset rejection and CMRR. This system also achieves the lowest power dissipation per channel.

VI. 4-CHANNEL WIRELESS EEG HEADSET

The low-power highly-integrated ASICs (AE and BE) enable their use in battery-powered wearable devices. A 4-channel wireless EEG headset utilizing these ASICs is shown in Fig. 20. The headset consists of four signal AEs, one reference AE, and one bias electrode. Two mechanical bridges cover all the electrode positions and have compartments for sensor node electronics and battery. The signal AEs are positioned at predefined positions: C_3 , C_4 , C_z and P_z according to the 10-20 electrode EEG system. The reference AE and bias electrode are positioned behind the ears at the mastoid bone. All these electronics are connected via flat cables and embedded in the headset.

The digital outputs of BE ASIC are streamed out to a low-power microcontroller [32] via a SPI protocol and stored in local memory. Then the data is transmitted wirelessly to PC through a low-power radio [33]. The data transmission of microcontroller and radio occupies more than 80% of the system power, while AEs and BE consume 5%.

Fig. 21 shows the spectrogram of the measured 4-channel EEG signals from a subject whose eyes were alternately opened and closed. There is no alpha wave during the eyes-open period for all channels, except some artifacts due to blinking. During the eyes-closed period, the alpha waves at 10 Hz are clearly visible on all four channels.

VII. CONCLUSION

This paper describes an 8-channel active-electrode (AE) system for EEG/ETI measurement with dry electrodes. The whole system consists of nine AE ASICs for high-quality pre-amplification, and a low-power highly-configurable BE ASIC for analog signal processing and digitization. Several circuit techniques were implemented to improve the system performance. Electrode offset is rejected by employing a DC-servo loop around a non-inverting chopper amplifier, whose input stage employs both PMOS and NMOS devices in parallel for greater noise efficiency. At the system level, a CMFF technique improves the CMRR of an AE pair by 25 dB; a PWM modulation scheme enables a single-wire data communication link between AE and BE; and a continuous-time ETI measurement scheme can sense impedances up to 550 k Ω . To demonstrate its functionality, the AE system was used to realize a light-weight, wireless 4-channel EEG headset based on dry electrodes.

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TABLE I
SUMMARY OF MAJOR GOALS AND SPECIFICATIONS TO FACILITATE AMBULATORY USAGE

Goals	Solutions	Specifications	
Patient Comfort			
Minimal intervention	Dry electrode, Continuous-time ETI monitoring	ETI range	500 kΩ@1kHz
Long battery-life	Low-power AE and BE ASICs, AE with voltage gain	Power AE gain BE gain	<1 mW@1.8V 20 dB-40 dB 0 dB-20 dB
System volume reduction	Few connecting wires between AE and BE via PWM interface, Fully-integrated ADC	Number of wires ADC	6 12-bit
Signal Quality			
Less 50/60 Hz interferences	Active electrode	Output impedance	<100kΩ
Low noise	Chopper amplifier	Input noise	<100 nV/sqrt(Hz)
Electrode offset rejection	AC-coupled amplifier	DC rejection	± 300 mV
High CMRR	CMFF architecture, High input-impedance amplifier	CMRR Input impedance	>80 dB >500 MΩ@20Hz

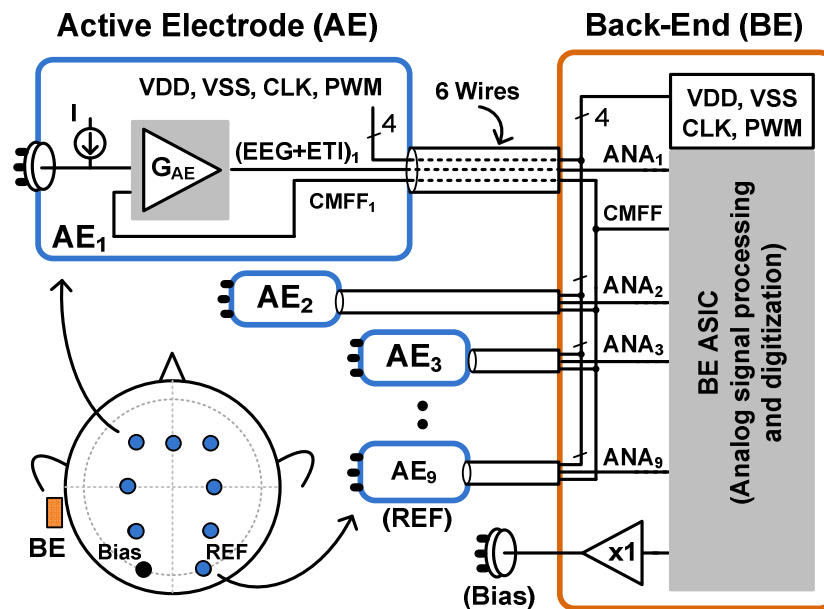


Fig. 1. Block diagram of the 8-channel active-electrode based EEG/ETI system

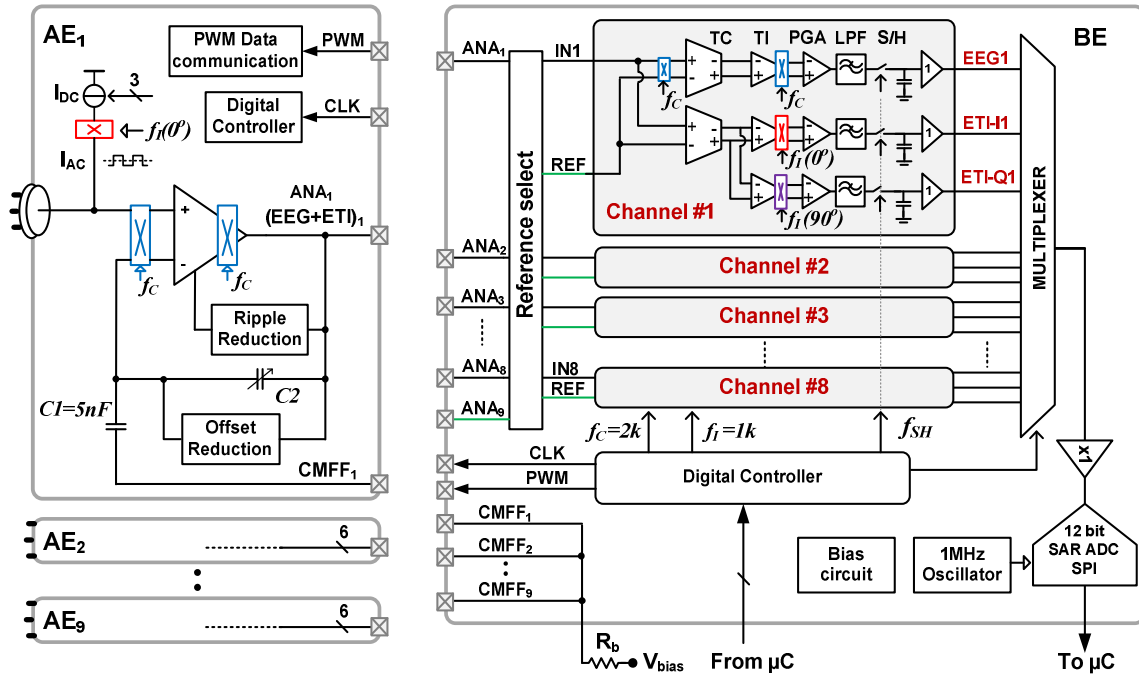


Fig. 2. Complete Architecture of the 8-channel EEG acquisition system. (TC and TI represent transconductance and transimpedance amplifiers, respectively).

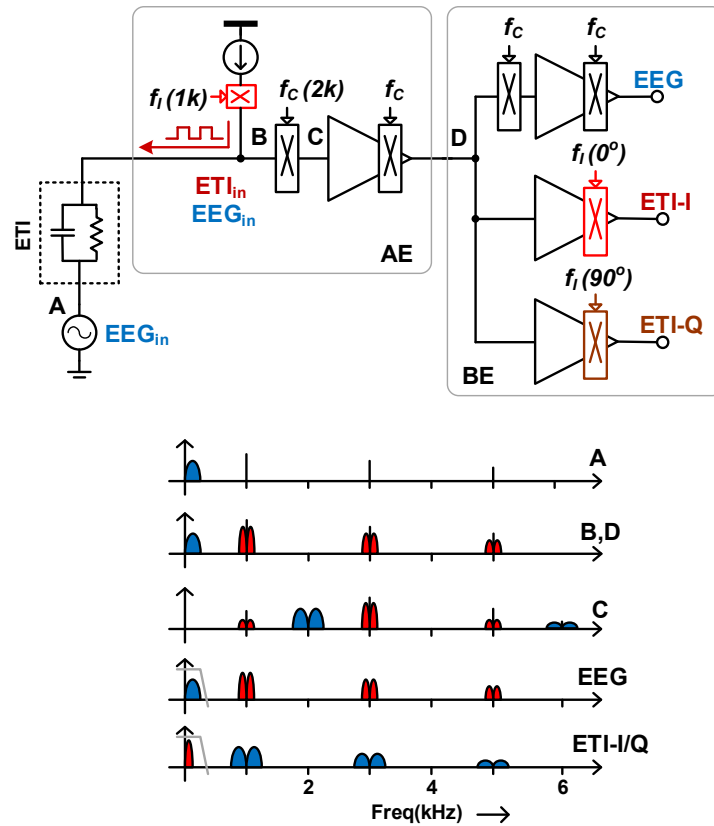


Fig. 3. Block diagram and spectrum illustration of the EEG/ETI measurement principle

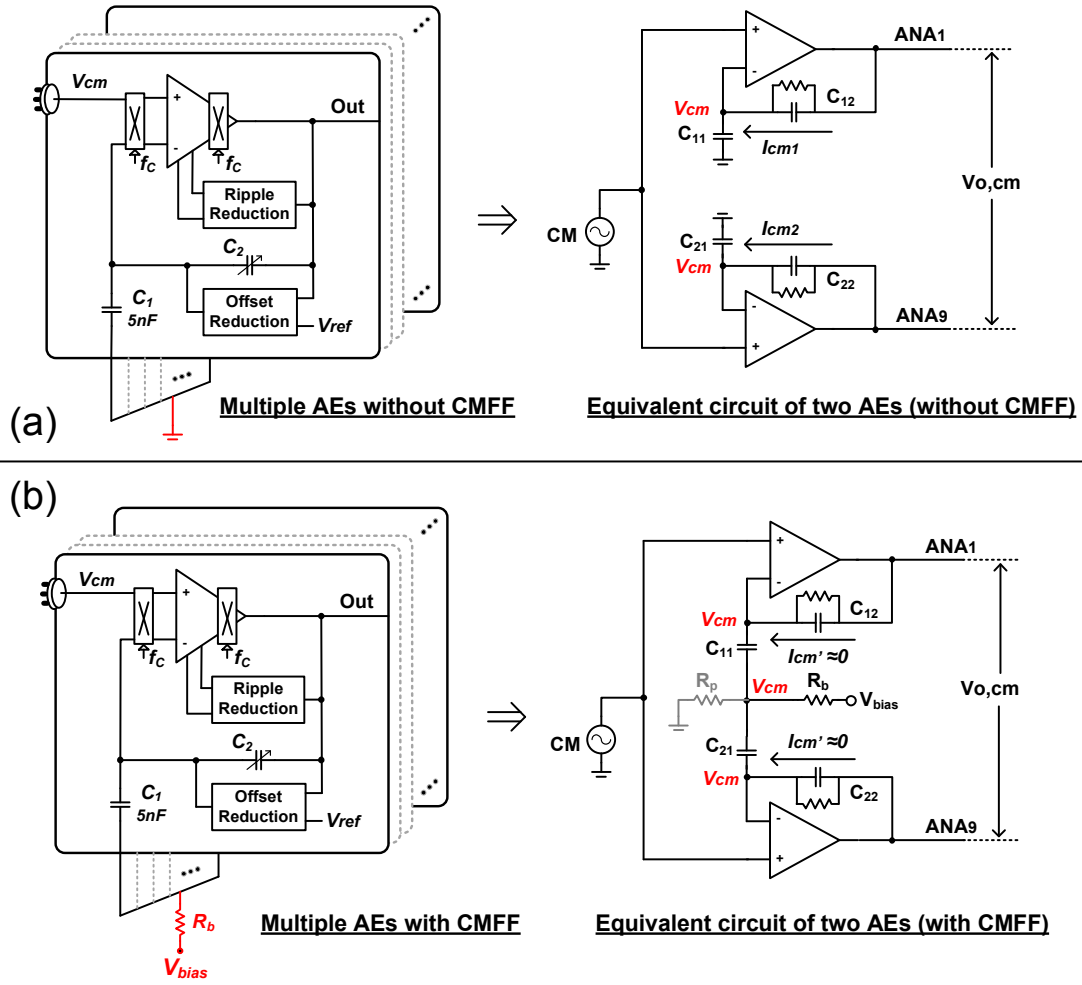


Fig. 4. (a) Conventional AEs without CMFF, and the equivalent circuit diagram of one-channel AEs; (b) AEs with CMFF for CMRR enhancement, and the equivalent circuit of one-channel AEs

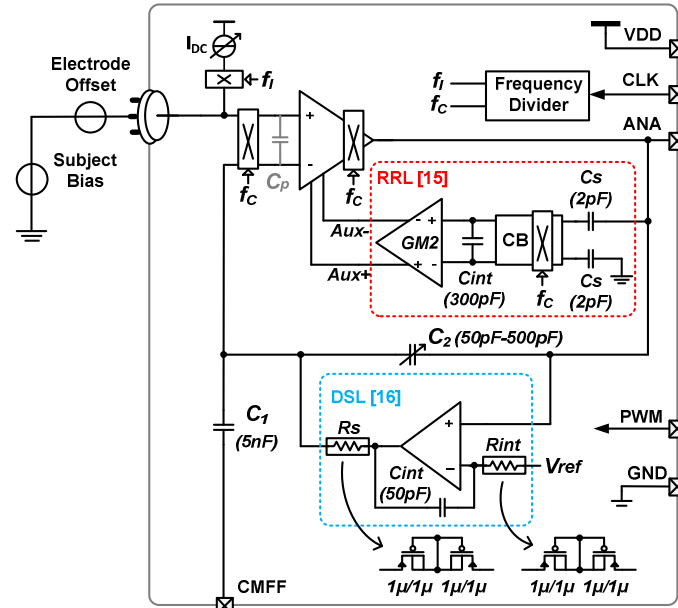


Fig. 5. Block diagram of the instrumentation amplifier in AE

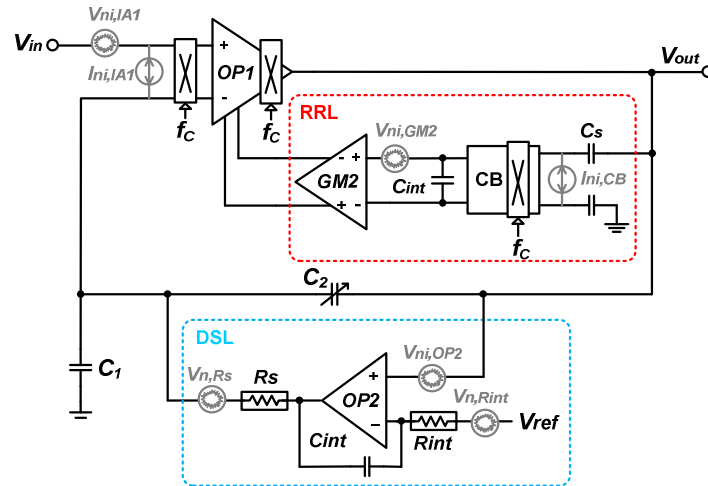


Fig. 6. Noise model of the instrumentation amplifier in AE

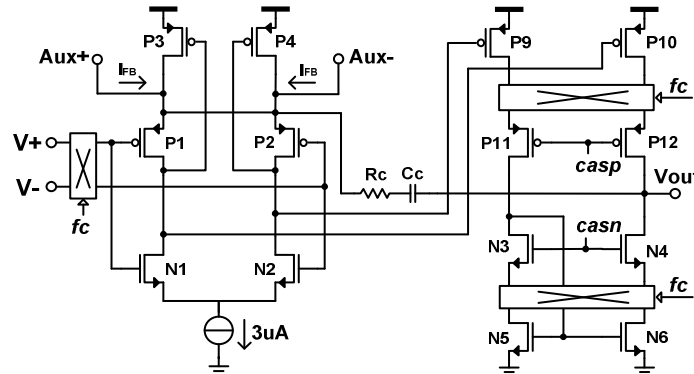


Fig. 7. Schematic of the core amplifier in AE

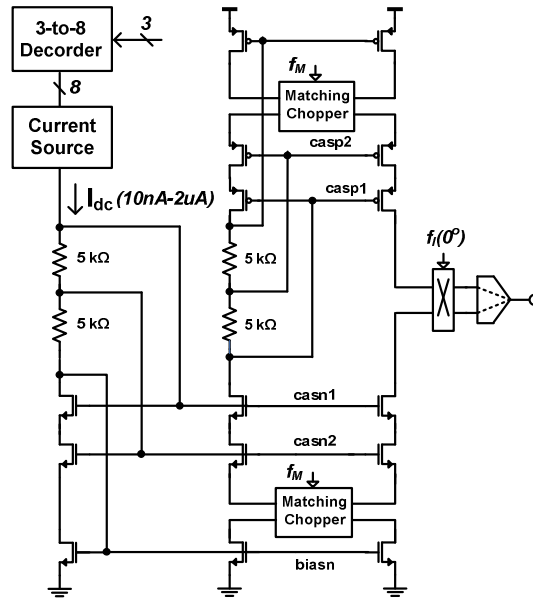


Fig. 8. A triple-cascode, self-biased, square-wave output current source

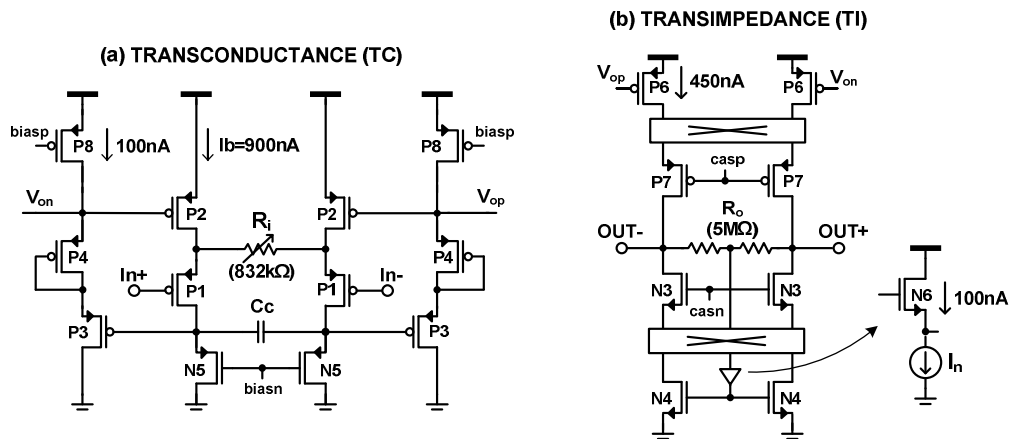


Fig. 9. Schematic of TC and TI stages of instrumentation amplifier

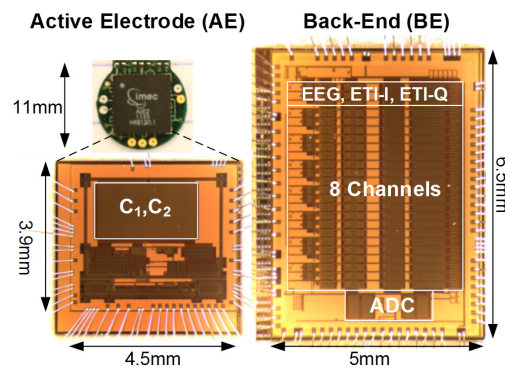


Fig. 10. Chip photograph (AE and BE).

TABLE II
POWER BREAKDOWN OF THE 8-CHANNEL AE SYSTEM BUILDING BLOCKS

Active Electrode (AE)	11.1 μ A *9=100 μ A
Core Pre-amplifier	5 μ A
DSL	1.5 μ A
RRL	0.7 μ A
Bias	1.9 μ A
Current Source	2 μ A
Back-End (BE) Readout	265 μ A
Bias	10 μ A
8-channel EEG	56 μ A
16-channel ETI	83.2 μ A
ADC+SPI	115.2 μ A
Total Power of the System	365 μ A@1.8V=657 μ W

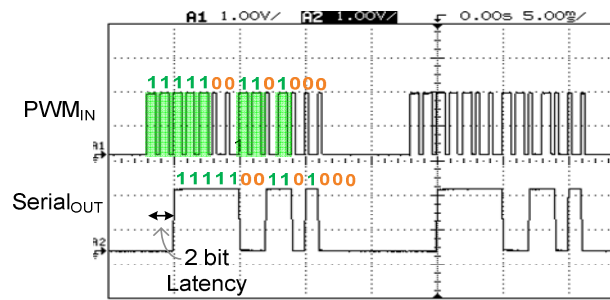


Fig. 11. Measured PWM input data and demodulated serial output

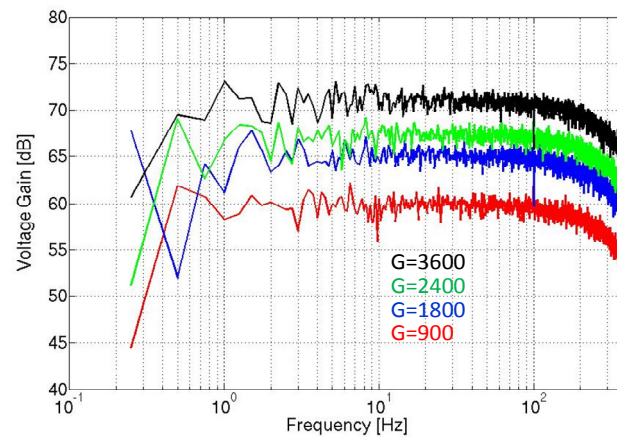


Fig. 12. Measured EEG channel gain of the system (G=900, 1800, 2400, 3600)

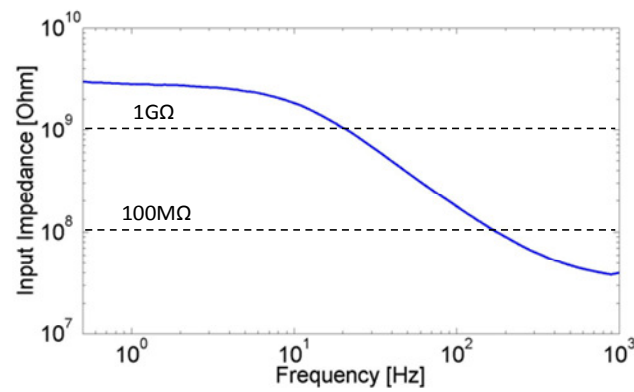


Fig. 13. Measured input-impedance of an AE

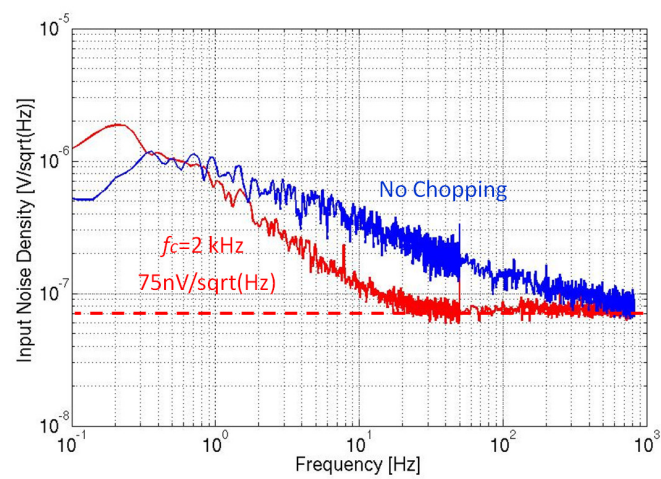


Fig. 14. Measured input referred noise density per channel (two AEs and one BE)

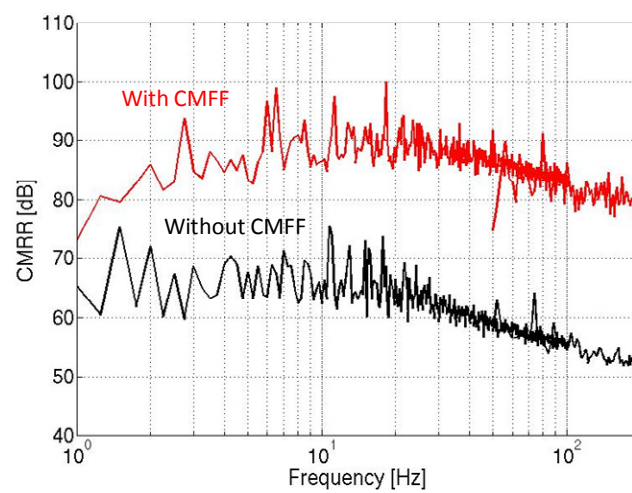


Fig. 15. Measured CMRR (with and without CMFF)

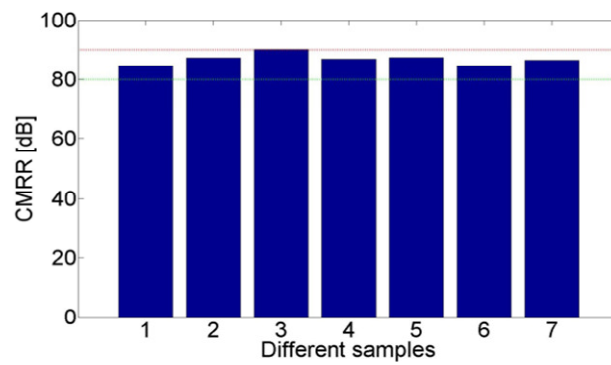


Fig. 16. Measured CMRR @50 Hz from different samples

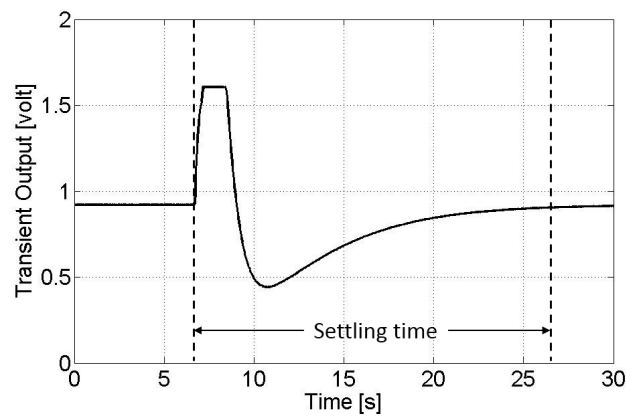


Fig. 17. Measured Settling time of the DC servo loop (DSL)

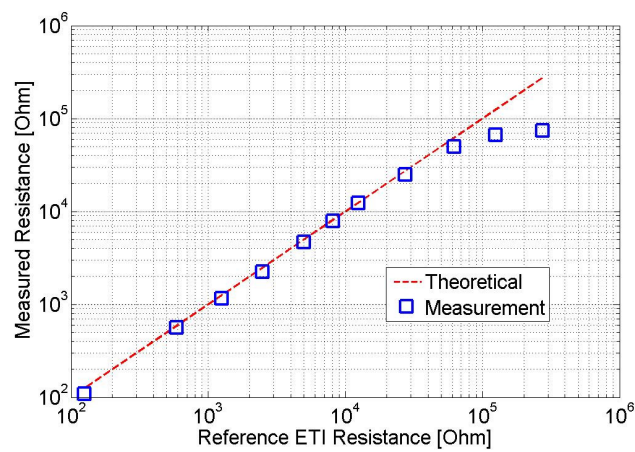


Fig. 18. Measured differential ETI resistance

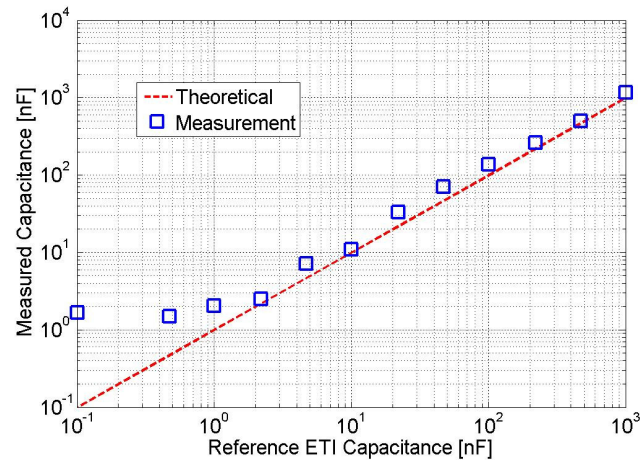


Fig. 19. Measured differential ETI capacitance

TABLE III
COMPARISON TABLE WITH THE STATE-OF-THE-ART ACTIVE ELECTRODE SYSTEM FOR BIOPOTENTIAL SIGNALS ACQUISITION

Parameters	[7]+[29]	[30]	[8]	[31]	This work
Technology	0.18 μm	N/A	0.35 μm	N/A	0.18 μm
Supply	1.8 V	5 V	3 V	3.3 V	1.8 V
AE Gain	3-100	100	N/A	11	11-101
Input Impedance	0.6G Ω @10Hz	1T Ω @DC	N/A	N/A	1.2G Ω @20Hz
Noise/Channel	1.2 μV_{rms} (0.5-100Hz)	7.49 μV_{rms} (1-1kHz)	0.9 μV_{rms} (0.5-100Hz)	2.4 μV_{rms} (0.5-100Hz)	1.75 μV_{rms} (0.5-100Hz)
Electrode Offset Rejection	Rail-to-rail	± 250 mV	N/A	Rail-to-rail	± 250 mV
CMRR	82 dB	78 dB	105 dB	90 dB	84 dB
ETI Measurement	No	No	Yes	No	Yes
Power/Channel (including ADC)	20 μW + N/A	7.5mW	1mW	600 μW	82 μW (EEG + ETI)

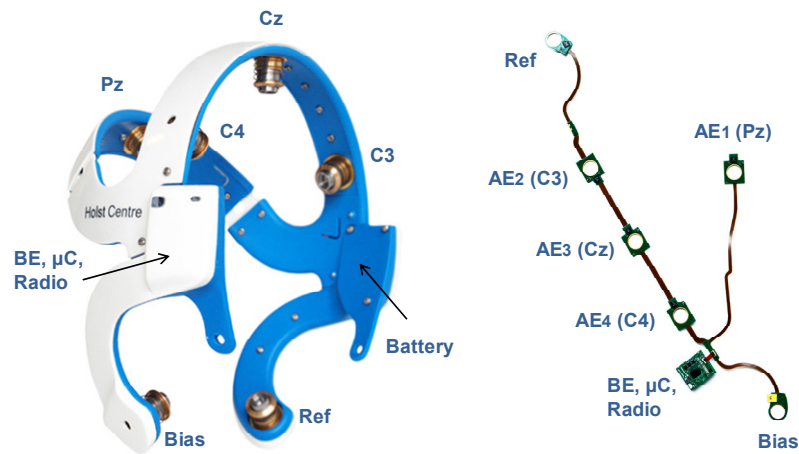


Fig. 20. Wireless EEG headset and its internal electronics

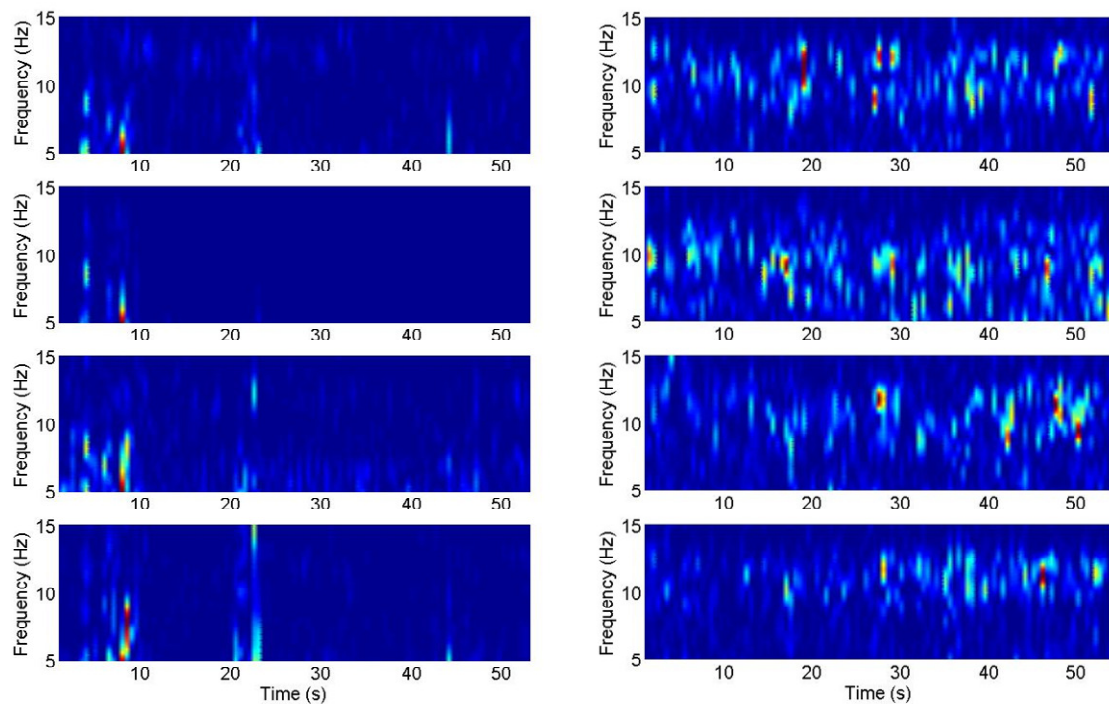
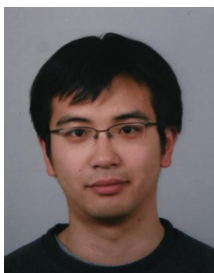


Fig. 21. 4-channel real-time EEG recording using dry-electrode wireless headset, during eyes open (left) and eyes closed (right); output channels from top to bottom: C₃, C₄, C_z, P_z.



Jiawei Xu received the M.Sc. degree in Microelectronics from Delft University of Technology, The Netherlands, in 2006. Since then, he started as a researcher on analog IC design at imec/Holst Centre in Eindhoven, The Netherlands, where he worked on low-power readout circuits for smart sensors. In 2010, he joined Delft University of Technology as a PhD candidate in collaboration with imec, where he is currently working on low-power biopotential readout circuits.



Srinjoy Mitra received his bachelor degree from Calcutta, India, and the M.Tech, degree from the Indian Institute of Technology, Bombay, India. After briefly working in microelectronic industry he completed his PhD from Institute of Neuroinformatics (UNI-ETH Zurich, Switzerland) in 2008. He spent two years as a post-doctoral researcher at The Johns Hopkins University, Baltimore USA and joined the medical electronics team at imec, Belgium, in 2010. His interests are in low-power analog circuits for biomedical interfaces.



Akinori Matsumoto was born in Hyogo, Japan. He received the M.Sc. degree in physical electronics from Osaka Prefecture University, Osaka, Japan, in 2003. He joined Panasonic Corporation in 2003 and was engaged in the developments of power management technology and analog-to-digital converters for system LSIs.

From June 2010 to January 2012, he worked at imec in Leuven, Belgium as an industrial engineer, where he developed low-power analog integrated circuits for EEG sensors. During the residence in Belgium, he was also involved in the system integration of the EEG sensors at Holst Centre in Eindhoven, The Netherlands. He is currently engaged in the research of biopotential sensors at Panasonic Advanced Technology Research Laboratories in Kyoto, Japan.



Shrishail Patki received his bachelor degree in Instrumentation Engineering from University of Mumbai and MS degree from University of Miami in Biomedical Engineering. He spent one and half years working as an assistant electronics engineer at Bio-Signal Group Corp where he worked on EEG system development. In 2010, he joined imec-nl/Holst Centre as a researcher, where he is currently working on system development of different generations of miniaturized, low noise and low power wireless EEG systems.



Chris Van Hoof (M'87) is Director Wearable Healthcare at imec, responsible for the R&D direction and business strategy of a multi-site R&D team across 3 imec locations (Eindhoven, Leuven and Gent). He has a track record of 20+ years of initiating, executing and leading national and international contract R&D with worldwide customers. His R&D has resulted in 3 imec startups and he has delivered space-qualified flight hardware to 2 cornerstone European Space Agency missions.

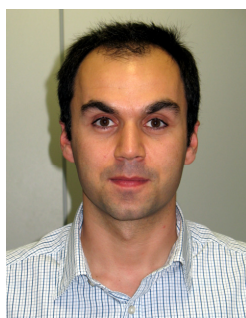
After a PhD in Electrical Engineering (University of Leuven, 1992), Chris Van Hoof has held positions at imec at manager and director level in diverse technical fields (sensors and imagers, MEMS and autonomous microsystems, wireless sensors, body-area networks). He has published over 500 publications and given more than 50 keynote and invited talks. Chris Van Hoof is an imec Fellow and also full professor at the University of Leuven (KU Leuven).



Kofi A. A. Makinwa (M'97–SM'05–F'11) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Nigeria in 1985 and 1988 respectively. In 1989, he received the M.E.E. degree from the Philips International Institute, The Netherlands and in 2004, the Ph.D. degree from Delft University of Technology, The Netherlands.

He is currently an Antoni van Leeuwenhoek Professor with the Faculty of Electrical Engineering, Computer Science and Mathematics, Delft University of Technology, which he joined in 1999. From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on interactive displays and on front-ends for optical and magnetic recording systems. His main research interests are in the design of precision analog circuitry, sigma-delta modulators, smart sensors and sensor interfaces. This has resulted in 7 books, 19 patents and over 180 technical papers.

Kofi Makinwa is on the program committees of the European Solid-State Circuits Conference (ESSCIRC) and the Advances in Analog Circuit Design (AACD) workshop. From 2006 to 2012, he was on the Program Committee of the International Solid-State Circuits Conference (ISSCC). He has been a guest editor of various issues of the Journal of Solid-State Circuits (JSSC) and a distinguished lecturer of the IEEE Solid-State Circuits Society (2008 to 2011). For his doctoral research, he was awarded the 2005 Simon Stevin Gezel Award from the Dutch Technology Foundation. He is a co-recipient of several best paper awards: from the JSSC, ISSCC, Transducers and ESSCIRC, among others. He is an alumnus of the Young Academy of the Royal Netherlands Academy of Arts and Sciences and an elected member of the IEEE Solid-State Circuits Society AdCom, the society's governing board.



R. Firat Yazicioglu has received the Ph.D. degree in Electronics Eng. from Katholieke Universiteit Leuven in 2008 in collaboration with imec, Belgium. He is currently working at imec, Belgium as R&D Team Leader and Principal Scientist, where he is leading the “Biomedical Integrated Circuits” team focusing on Analog and Mixed Signal Integrated Circuit design for wearable and implantable biomedical applications.

During his career, Dr. Yazicioglu has (co)authored over 70 publications, 3 book chapters, and a book on ultra-low-power circuit and system design for biomedical applications, and authored several patents in this field. He has developed several generations of integrated circuits for wearable and implantable healthcare applications.

Dr. Yazicioglu is the co-receipient of best (student) paper award in Int. Symp. on Circuits and Systems (ISCAS) 2013, Biomedical Circuits and System Conf. (BioCAS) 2011, Smart Systems Integration Conf. (SSI), 2008, and Sensors&Transducers Journal 2008. Dr. Yazicioglu is member of IEEE and serves in the technical program committees of European Solid State Circuits (ESSCIRC) and International Solid State Circuit Conference (ISSCC). He was the co-chair of Biomedical Circuits and Systems Conference (BioCAS) 2013 in Rotterdam.