Comments and Corrections

Correction to "Reconfigurable Processor for Energy-Efficient Computational Photography"

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In the above paper [1], an error was made in reporting the operating voltage for the SRAMs. Section VI of the paper states: "The test chip, shown in Fig. 19, is implemented in 40 nm CMOS technology and

Manuscript received August 17, 2014; accepted August 23, 2014. Date of publication September 16, 2014; date of current version October 24, 2014.

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Digital Object Identifier 10.1109/JSSC.2014.2353797

verified to be operational from 25 MHz at 0.5 V to 98 MHz at 0.9 V with SRAMs operating at 0.9 V." The processor and the SRAMs were connected together and operated from the same supply voltage on chip. As a result, this statement should be modified as: "The test chip, shown in Fig. 19, is implemented in 40 nm CMOS technology and verified to be operational from 25 MHz at 0.5 V to 98 MHz at 0.9 V." The reference to the SRAM supply being at 0.9 V should be ignored in the table in Fig. 19.

We would like to thank our colleagues Arun Paidimarri and Mehul Tikekar for bringing this error to our attention.

REFERENCES

 R. Rithe, P. Raina, N. Ickes, S. Tenneti, and A. P. Chandrakasan, "Reconfigurable processor for energy-efficient computational photography," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2908–2919, Nov. 2013.