An Interleaved Full Nyquist High-Speed DAC Technique

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Abstract—A 9 bit 11 GS/s DAC is presented that achieves an SFDR of more than 50 dB across Nyquist and IM3 below −50 dBc across Nyquist. The DAC uses a two-times interleaved architecture to suppress spurs that typically limit DAC performance. Despite requiring two current-steering DACs for the interleaved architecture, the relative low demands on performance of these sub-DACs imply that they can be implemented in an area and power efficient way. Together with a quad-switching architecture to decrease demands on the power supply and bias generation and employing the multiplexer switches in triode, the total core area is only 0.04 mm² while consuming 110 mW from a single 1.0 V supply.

Index Terms—CMOS, current-steering, digital-to-analog converter (DAC), full Nyquist, high speed, quad-switching, time-interleaving (TI).

I. INTRODUCTION

CURRENT-STEERING (CS) digital-to-analog converters (DACs) are commonly used to generate high-frequency signals. These converters consist of an array of current-sources and current-switches as depicted in Fig. 1. Depending on the digital code, current is switched either to the positive or the negative output. Distortion components in the output current are due to both static and dynamic error mechanisms. Static errors include those due to mismatch between current-sources and those due to the finite output resistance of the current-sources. Dynamic errors are due to, e.g., timing errors at the switching moment, glitches of the switches and output capacitance of the current-sources. High-speed DACs are typically limited in their linearity by dynamic errors; static errors can generally be sufficiently suppressed to not limit the high-frequency performance [1].

A. Dynamic Errors

Many significant dynamic error mechanisms are present in CS DACs. One of the major dynamic error mechanisms is non-exact timing in the data switches. Timing errors can be variable, due to, e.g., data-dependent clock loading, or they can be static,

due to, e.g., random component mismatch or layout issues. For high-speed DACs timing errors are required to be in the sub-picosecond range, which is tough to achieve. Return-to-zero (RZ) output waveforms can reduce the impact of timing errors, either using RZ as a method to retime the output [1], [2], by randomizing the required switching actions [3] or as a periodical reset method to suppress signal-dependent phenomena. However, RZ waveforms also introduce their own drawbacks.

Other timing related errors are due to, e.g., break-before-make behavior of switches that have periodically both switches in their off-state during switching, leaving the current source disabled and forcing some kind of recovery behavior after switching. Further significant timing related error mechanisms are due to differences in rise and fall times of the switches and effects such as clock feedthrough that all create spurs in the DAC's output signal.

In conventional CS DACs, the data switches switch only if the new code is different from the previous code: the amount of switching is hence code dependent. Switching introduces code-dependent load on the power supply, and induces disturbances to, e.g., the bias lines. Both of these effects yield unwanted modulation of the output signal. Current-mode logic may be used to reduce the impact of this, but for complete suppression the switching fundamentally needs to be data-independent, which can for example be achieved with RZ-switching or quad-switching [4].

A last significant source of dynamic errors is the output capacitance of the current sources. While this capacitance usually is very linear, these capacitances are data-dependently switched to either the positive or the negative output. Together with the load impedance they form a code-dependent RC filter, which results in spurs. In [5] this effect is reduced by adding cascodes and bleeding current sources, at the cost of more power consumption.

All these dynamic error mechanisms start at the switching time instance and last for a fraction of the sample period. The timing and switching related errors can have a large impact despite occurring only for a picosecond or even less.

B. Interleaved Architecture

Dynamic errors in CS DACs are present at the switching time and during a short period after the switching time instances. During the remainder of a sampling period, the effect of these dynamic errors can be sufficiently small. Consequently, the linearity of a CS DAC can be improved if we make sure the DAC is not connected to the output during the time that the dynamic errors are significant; this is, for example, done in [1], [2] in the form of an RZ output signal. However, RZ results
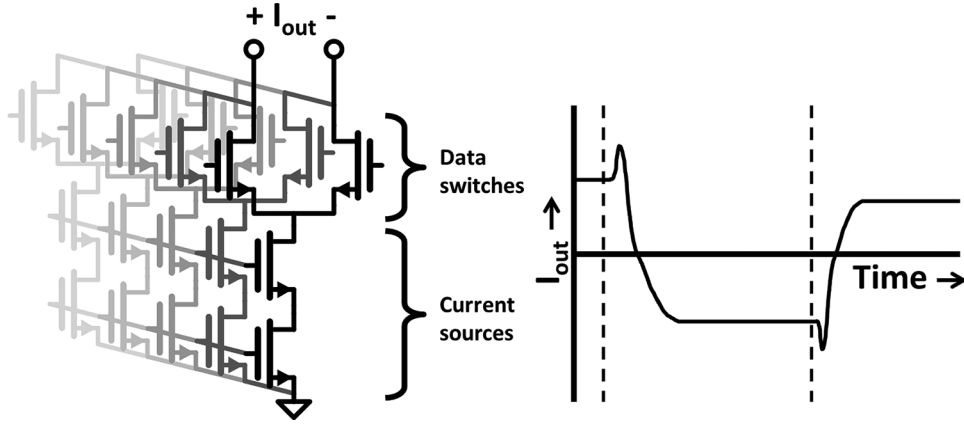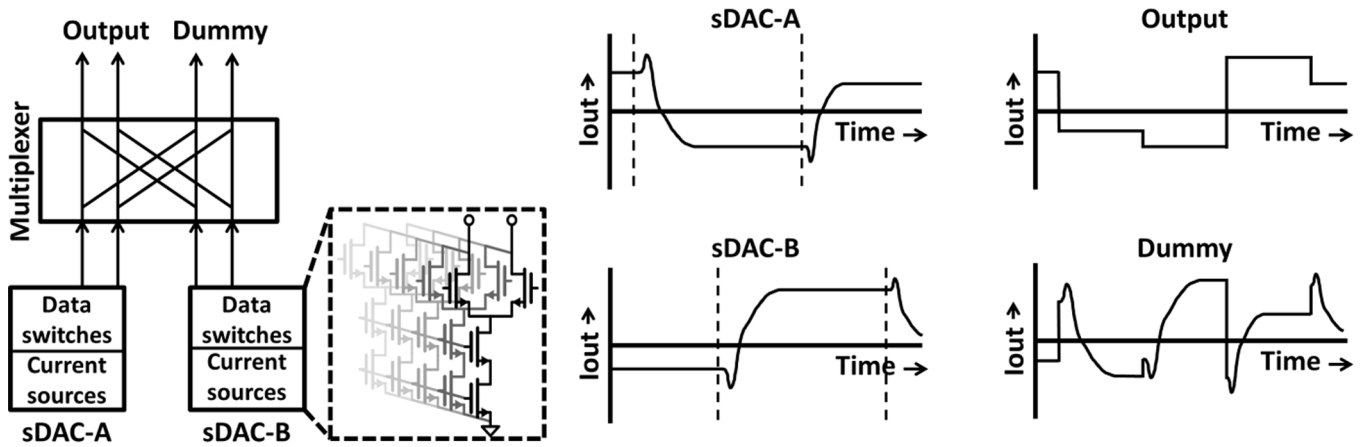
Fig. 1. Current-steering DAC structure.

Fig. 2. Interleaved architecture.

in much larger transients and increases demands on analog post-filtering while at the same time the delivered output power is decreased. This can be improved by using two sub-DACs (sDACs) that operate alternatingly by using opposite clock phases: then each sDAC can be connected to a dummy-output during the switching moment thereby placing the timing and settling related errors on only the dummy-output. Once settled, the sDAC's output can be routed to the actual output, and meanwhile the other sDAC can switch to and settle to its new code. The corresponding interleaved architecture for this is shown in Fig. 2. In this figure sDAC-A and sDAC-B are alternatingly switched to the actual output and to a dummy output by the multiplexer. In [6] a 10–20 dB improvement in IM3 versus frequency across Nyquist was achieved using this interleaving technique, demonstrating the merits of interleaving. Details of the sDAC implementation are described in Section V, while the demands on the implementation and the actual circuit implementation of the multiplexer is described in Sections II-C, III, and V, respectively. Note that while this interleaved approach doubles the required area and power compared to the RZ variant, it also doubles the sampling rate without requiring higher switching frequencies and outputs a regular, non-return-to-zero, waveform.

Several other interleaving architectures are known from literature; a brief discussion is given below. Placing multiple sDACs in parallel and shorting their outputs is sometimes classified as interleaving [7]. However, while this is easy to implement and does double the sampling rate, it does not solve issues such as timing mismatch and code-dependent settling speed. Since it sums the currents it does not output the converted digital input word, but the sum of the last two, modifying the frequency response. This last issue can be solved by implementing RZ switching in each sDAC cell [8] which makes sure that only the current code is converted to the output, and at the same time it adds some of the advantages of an RZ DAC. However, it does not remove all of the timing and settling issues associated with conventional RZ DACs.

In this paper, the focus is on two-times-interleaved CS DAC architectures with a central multiplexer to combine the outputs; see Fig. 2. Higher interleaving counts can be used, but two-times interleaving will already suppress all timing errors sufficiently by giving enough time for settling of nodes.

Using an interleaved architecture as low-power, area-efficient solution might seem counter-intuitive at first; placing two sDACs in parallel doubles both area and power consumption, and additionally also an analog multiplexer is required to toggle between the two. However, since both sDACs only run at half the overall DACs speed with significantly reduced demands on dynamic errors for each sDAC due to the interleaving setup, each individual sDAC can actually be small and

low-power, while maintaining a good overall interleaved DAC performance.

Interleaved DACs employing an analog multiplexer have been reported before. The work in [9] contains the first reference to this method of removing switching transients from the output of a DAC; using an opamp with a built-in multiplexer to switch between two sDACs. In [10] a method to limit the impact of gain mismatch between sDACs is presented and illustrated only using simulations on an idealized circuit. Our interleaved DAC in [6] uses triode switches without quad-switching to obtain 58 dB SFDR across Nyquist at 1.7 GS/s. In [11] saturation switches are used; large bleeder currents are added to improve their linearity. The design in [11] achieves 69 dB SFDR across less than a quarter Nyquist at 4.6 GS/s at a cost of more than one order higher power consumption and two orders in area compared to the work in this paper. This paper is based on [12], presenting more in-depth analyses of both error mechanisms and design considerations of interleaved DACs. Compared to our interleaved DAC from [6], this design achieves significantly higher speed with a decrease in linearity and a lot smaller core area. Instead of an active calibrated current source array, passive matching is used for the current sources and quad-switching is introduced which works in tandem with the interleaved architecture to suppress spurs.

II. Interleaving Errors Mechanisms

While the interleaved architecture suppresses most of the regular dynamic CS-DAC errors, it also introduces new errors that may limit performance if not dealt with correctly. The sDACs need to be matched well, both in their code-output signal transfer and in the time that they are connected to the output. Note that the first property is due to the matching of the two sDACs while the second property is determined by the analog multiplexer that toggles between the two sDACs.

In a regular CS-DAC, all data switches route the current of their associated current source to either output; hence the switches switch a static code-independent current. In the interleaved architecture, the switches in each individual sDAC also switch static code-independent currents, but the analog multiplexer that toggles between both sDACs switches the full, code-dependent, output current. This results in additional challenges to obtain good spectral performance compared to conventional CS DACs.

The following sections discuss the most important issues in interleaved DACs.

A. Static Matching of the sDACs

To simplify the analysis of the overall DAC performance limitation due to static sDAC mismatch, the output signal of the second sDAC is written as that of the first sDAC with a code-dependent mismatch term: $V_{\text{out,sDAC-B}}(\text{code}) = V_{\text{out,sDAC-A}}(\text{code}) + \epsilon(\text{code})$. Each of the sDACs in the interleaved DAC runs at half the sampling frequency, with their corresponding image frequencies. For perfectly matched sDACs, $\epsilon(\text{code}) \equiv 0$ and the image frequencies due to interleaving cancel each other. In that case,
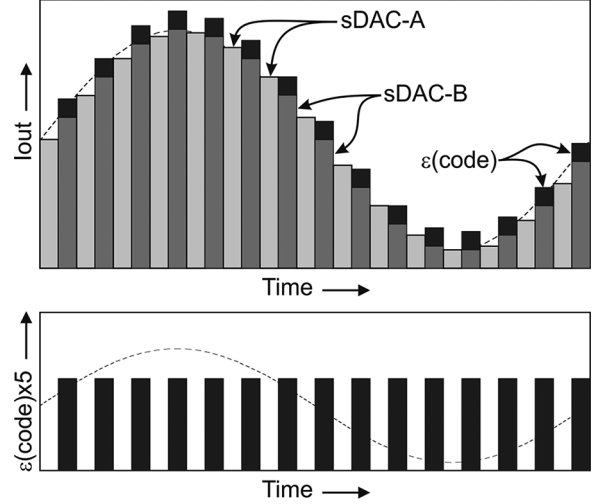

Fig. 3. Output of an interleaved DAC with an offset error between the sDACs.

the harmonics and images created by the interleaved DAC due to, e.g., any non-linearity in $V_{\text{out,sDAC-A}}(\text{code})$ are exactly the same as that of a non-interleaved DAC having the same $V_{\text{out,DAC}}(\text{code})$. Any mismatch $\epsilon(\text{code})$ between the sDACs, however, limits the cancellation of the image frequencies, while these images fall in-band for the complete interleaved DAC when assuming full Nyquist operation.

In a conventional non-interleaved DAC, a DC offset has no effect on its performance. In an interleaved DAC, a DC offset $\epsilon(\text{code}) = \Delta$ between the two sDACs results in a square wave shaped output signal running at half the sampling frequency, creating a spur at half-FS and at DC. An illustration of this error mechanism is shown Fig. 3; the output signals of both sDACs are shown in the top graph for a sinusoidal output, where the output signal of sDAC-B equals the sum of the output signal that sDAC-A would give for the same code and of a fixed offset. The lower graph in Fig. 3 shows only this error component, scaled up by a factor 5 for illustration purposes. The resulting spurs reside outside the Nyquist band.

Similarly, a gain error has no effect on the output spectrum in a conventional DAC. In the interleaved DAC, a gain error $\epsilon(\text{code}) = \varepsilon_{\text{gain}} * V_{\text{out,sDAC-A}}(\text{code})$ generates an RZ output signal proportional to the output signal, at half the sample frequency of the overall system. Fig. 4 shows an illustration of this error mechanism: the output signals of both sDACs are shown in the top graph for a sinusoidal output. The output of sDAC-B is subdivided into the response that sDAC-A would have given for the same code and into the error contribution $\epsilon(\text{code})$. The lower graph in Fig. 4 shows only this error component, scaled up by a factor 5, which is proportional to a 50% duty cycle RZ-version of the DAC's output signal.

Since $\epsilon(\text{code})$ has half the sampling frequency of the complete DAC, it generates signals at exactly the output frequency, adding to the main signal, and generating spurs mirrored around half Nyquist:

$$f_{\text{spur}} = \frac{f_{\text{sample}}}{2} - f_{\text{signal}} \qquad (1)$$
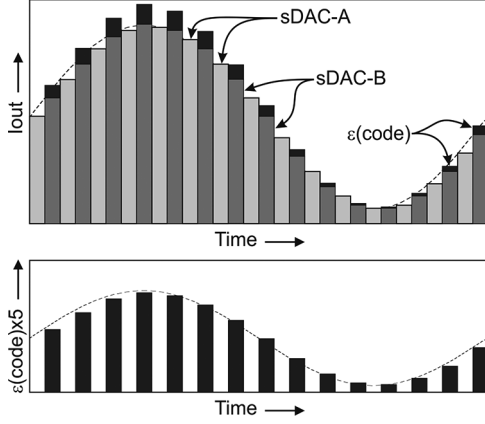
Fig. 4. Output of an interleaved DAC with a gain error between the sDACs.

Fig. 5. Output of an interleaved DAC with a duty-cycle error.

Ignoring the frequency roll-off due to zero-order hold behavior, the SFDR of the resulting return-to-zero signal is given by

$$\text{SFDR} = 20 \log_{10} \left(\frac{1}{\epsilon_{\text{gain}}} \right) + 6 \text{ dB} \qquad (2)$$

where the 6 dB is due to the 50% duty cycle of the RZ signal. When the zero-order hold behavior is taken into account the fundamental has a $\text{sinc}(x)$-shaped frequency response. The image is a return-to-zero signal at half the sampling frequency, yielding an equal sinc-shaped frequency response with 6 dB attenuation. Noting that the image frequency is mirrored around half Nyquist compared to the fundamental, the overall attenuation of the image compared to the fundamental is given by

$$\text{Image}_{\text{attenuation}} = 20 \log_{10} \left(\frac{\text{sinc}\left(\frac{f_{\text{signal}}}{f_{\text{sample}}} \right)}{\text{sinc}\left(\frac{\frac{f_{\text{sample}}}{2} - f_{\text{signal}}}{f_{\text{sample}}} \right)} \right). \qquad (3)$$

At (near) DC signal frequency, the relative attenuation of the image according to (3) is 4 dB, while at (near) Nyquist signal frequency this relative image attenuation is -4 dB. This yields

$$\text{SFDR}_{\text{DC}} = 20 \log_{10} \left(\frac{1}{\epsilon_{\text{gain}}} \right) + 10 \text{ dB} \qquad (4)$$

$$\text{SFDR}_{\text{Nyquist}} = 20 \log_{10} \left(\frac{1}{\epsilon_{\text{gain}}} \right) + 2 \text{ dB}. \qquad (5)$$

Higher order mismatch between the sDACs, where $\epsilon(\text{code}) = \varepsilon_n * V_{\text{out,sDAC1}}^n(\text{code})$, gives harmonics of the fundamental in the output current and due to the RZ behavior these are also folded around half-Nyquist. The effect of this higher order mismatch also result in spurs in a similar way as in CS DACs; so the required matching to suppress the spurs in interleaved DACs is also similar to the matching required for a regular CS DAC. It does not matter if this higher order mismatch is common for the sDACs or opposite to each other for the size of the resulting spur.
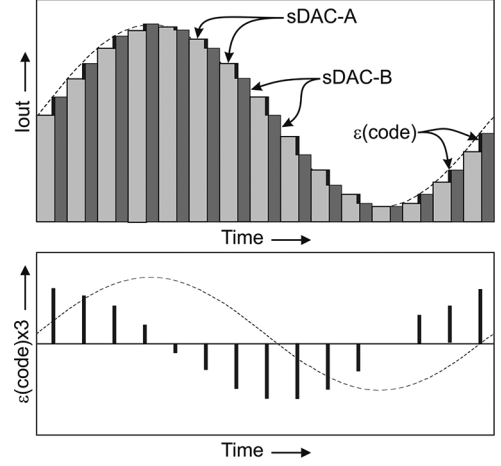
B. Dynamic Matching of the Multiplexer

Mismatch in the multiplexer and its driver result in a non-50% duty cycle for the connection of either sDAC to the overall output, which in turn yields spurs in the DAC output signal. With a non-50% duty cycle, one sDAC (e.g., the signal due to one code) is still at the output, while the next one should already have been placed on the output. Since this happens only at every second transition, an error is created which occurs at only half the sample rate of the complete DAC. This spur is located at the same frequency as an amplitude error (1).

Assuming a sinusoidal fundamental signal with unit amplitude and ignoring the sampled nature of the DACs output signal, the size of the error $\epsilon(\text{code})$ can easily be estimated. Under these assumptions, the error due to non-50% duty cycle switching between the two sDACs is a pulse train, at half the sample frequency. The amplitude of these pulses is the difference between two consecutive samples, which can be approximated by the derivative of the fundamental signal multiplied by the sample period, i.e., divided by its sample frequency. In this approximation, the sinc roll-off is ignored which effectively yields an overestimation of the error.

$$\epsilon_{\text{amp-pulse}} = \frac{2\pi f_{\text{signal}}}{f_{\text{sample}}} \cos(2\pi f_{\text{signal}} t). \qquad (6)$$

The duty cycle *of the error pulse train* is determined by the timing error, denoted as Δt, divided by two sample times, since it only occurs once every two samples:

$$\epsilon_{\text{duty-pulse}} = \frac{1}{2} \Delta t f_{\text{sample}}. \qquad (7)$$

An illustration of this error mechanism and of the resulting error signal is given in Fig. 5. The output signals of both sDACs are shown in the top graph for a sinusoidal output, for a 60% duty-cycle for sDAC-A; the output of sDAC-A is subdivided into the response for 50% duty-cycles and into an error contribution $\epsilon(\text{code})$. The lower graph in Fig. 5 shows only this error component, scaled up by a factor 3.

If the sDACs' duty cycle is almost 50%, the error pulse train has a small duty cycle $\epsilon_{\text{duty-pulse}}$, and the roll-off of its output spectrum is negligible for the first Nyquist zone. The magnitude

of the spurs in the signal band is simply the product of the error amplitude in (6) and the duty cycle in (7). The SFDR due to only the spurs originating from a non-50% duty cycle for the sDACs is the ratio between the fundamental signal and this error signal. The fundamental does suffer from a sinc roll-off as does the error signal amplitude, which was ignored in (6). Since these two sinc-roll-offs have an equal dependency on the fundamental frequency, they cancel each other when calculating the SFDR. This yields the following expression for SFDR due to duty cycle errors:

$$\text{SFDR} = 20 \log_{10} \left(\frac{1}{\pi f_{\text{signal}} \Delta t} \right). \qquad (8)$$

For the presented 11 GS/s full-Nyquist DAC this sets the maximum allowed timing error at less than 200 fs to be able to reach 50 dB SFDR, which is a stringent requirement.

C. Multiplexer Transistor Nonlinearities

Switches in regular CS DACs only have to switch a fixed (code-independent) current which is one of the reasons they are suitable for high-speed operation. In contrast, the multiplexer transistors in an interleaved DAC switch the output signal of the full sDACs, these signals are by definition code dependent and which hence may yield code-dependent spurs.

This code dependency results in for example a varying load impedance seen by the sDACs, which results in code-dependent settling speed, creating spurs in the output spectrum. Ideally in an interleaved DAC structure as presented in this paper this is irrelevant, since all signals in an sDAC should be fully settled before that sDAC is connected to the output by the multiplexer. However, for example charge injection from the fairly large multiplexer switches also has to settle, similar to transients caused by bondwire inductance and these are not suppressed in the interleaved structure. The multiplexer switches can be implemented with saturation or triode mosfets.

Saturation switches have as advantages that they provide reverse isolation and, if sufficiently wide, provide a low-ohmic load impedance for the sDACs. This low-ohmic loading of each sDAC decreases the signal swing at the source node of the multiplexers, improving sDAC linearity, and allowing for a larger output swing without the multiplexer transistors leaving their operating area. The downside is that the multiplexer's transistors behavior is highly dependent on drain current. At low drain current levels, their transconductance is low, providing a relatively high-ohmic load to the sDACs. Extra bias current or bleeders can reduce this problem, but relatively high levels of extra bias current would be required to get sufficiently low code-independent loading effects. Another issue with multiplexer transistors in saturation is that the DC voltage level of the output voltage of the DAC must be sufficiently high to ensure that these transistors stay in saturation which would increases power consumption and decreases the voltage headroom at the output of the DAC.

Triode switches operate largely independent of their drain current: their on-resistance is a relatively weak function of drain current compared to saturation switches. Since a triode switch in its on-state appears as a resistance in series with the load resistance, the sDACs see a relative constant load. Furthermore,

triode switches are bi-directional: both positive and negative currents (the latter due to, e.g., charge dump) are properly routed to the dummy-output. A last advantage of using triode switches over conventional saturation switches is that the drain-source voltage in triode is small which maximizes the voltage headroom. A drawback of using triode switches is that the source nodes of the multiplexer switches experience almost the full swing of the DAC output signal; this increases demands on the output impedance of the sDACs and requires operation of the triode switches in deep triode. Taking both the advantages and disadvantages of both options into account, our low-power interleaved DAC implements deep triode switches.

III. QUAD SWITCHING

Due to the switching of the data-switches, both the bias line(s) and power supply line(s) observe a code-dependent load which severely limits DAC linearity and may couple into the output signal.

The interleaving architecture inherently allows settling of all kinds of switching related issues, as long as sufficient settling is accomplished in an sDAC before placing it on the overall DAC output. For bias and power supply lines this translates in requiring low-ohmic (reference) voltages without decoupling capacitors as the latter are inherently slow.[1] Compared to the other nodes in high-speed DACs, these bias and supply power lines are, however, relatively slow, and a sufficiently low-ohmic reference over a wide bandwidth would require high power consumption. Hence, while interleaving suppresses artifacts from code-dependent switching, extra measures are required to decrease the code-dependent loading of bias and supply lines in an area and power efficient way.

A well-known method to decrease data-dependent behavior is using dummy structures that switch when the main structure does not switch. This fundamentally costs power and area. Using matched dummy structures to sufficiently suppress loading effects in high-speed DACs the increase in area and power is roughly a factor 2.

An alternative to using dummies is quad-switching [13], [14] which uses four switches per current source to direct the current to the positive or negative output; see, e.g., Fig. 6. Similar to dummy structures, quad-switches make sure every cycle the same amount of switching activity occurs: regardless of the (change in) code every clock cycle in each sDAC slice one switch will turn off and one switch will turn on. However, in contrast to a full dummy structure in parallel, quad switching re-uses the regular current sources, thereby only adding the extra switches and their drivers, with their corresponding increase in area and active power. Since quad switching structures can be closely grouped, timing matching can be better than with separate dummy structures.

However, quad-switching also has downsides compared to using dummy structures. The main problem is that the extra switches are directly in the signal path. The extra amount of

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[1]If there are no area requirements, an alternative may be to use very slow settling which effectively will make any bias and power supply line purely DC. This usually requires huge on-chip capacitances and many low-ohmic wiring which typically is not acceptable.
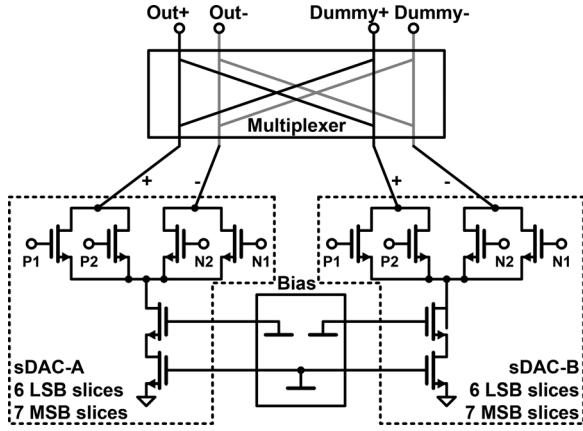
Fig. 6.   Schematic of the sDAC implementation and their connections.

switches increases the likelihood of timing errors, and differences between the two switches for one side result in spurs similar to interleaving spurs, which would require the high timing demands of interleaving switches. The usual way to solve these spurs is to run the quad-switches at twice the data rate [15]: in each sample period both switches for the active output are toggled. In interleaving DACs however, these quad-switching spurs mentioned above are *inherently suppressed* in the same way as all other data timing related errors. Static differences in output current between the different quad-switches, for example due to differences in threshold voltage, modulating the drain voltage of the current source, are suppressed by the output impedance of the current sources, and are generally not an issue. This makes quad-switching very suitable to be integrated in an interleaved architecture: the advantages of quad-switching are obtained, while its disadvantages are inherently suppressed.

IV. MEASURING AND TUNING THE MULTIPLEXER DUTY CYCLE

In our design, the multiplexer driver achieves good timing accuracy because in the (symmetrical) layout it is positioned in the symmetry plane while it is optimized for maximum passive matching. However, passive matching alone is not sufficient to reach the required timing accuracy required for a decent SFDR; see, e.g., (8). Duty cycle calibration is implemented to solve timing issues; this requires both a means to accurately measure timing and circuitry that can tune the timing in the sub-picosecond range.

Direct measurement of sub-picosecond timing requires high-end measurement equipment. However, for interleaved DACs only the timing error must be known and must be tuned to zero. This tuning error can easily be estimated using (1): a calibration signal at half the sampling frequency generates a timing spur at DC. This DC spur can be measured and tuned to zero using, e.g., an auxiliary ADC with low linearity and low signal bandwidth. Generating this calibration signal with an interleaved DAC is straightforward: both sDACs are placed at a constant, opposite, code. Assuming the amplitudes of the sDACs are equal, any error in the duty cycle will result in a non-zero DC differential output voltage level.

In practice, there will be offsets in the measurement, for example due to mismatch in the load resistors or in the ADC itself.

By swapping the sDAC codes these offsets can be cancelled, via the same principle as a chopper amplifier is based on. This also allows for doing the calibration single-endedly instead of differentially. Large variations in supply voltage or temperature can require new calibrations to keep the duty-cycle error sufficiently small. However, for small changes this is not necessary since the majority of the variation in delay due to these variations will be common mode for the positive and negative switch signals.

During calibration, the signal is at Nyquist while the calibration attempts to remove all spurs at DC. If amplitude mismatch is also present, this creates a spur at DC as well. The algorithm tries to cancel this spur by introducing a duty cycle error that creates a spur with equal size but opposite phase, cancelling out the amplitude spur.

For signals near DC, a duty cycle error has little effect while the amplitude error is attenuated by 10 dB; see (4). With just an amplitude error present this would decrease to 2 dB at Nyquist; see (5). However, with increasing signal frequency, the size of the duty cycle spur (with opposite phase compared to the amplitude spur) increases and increasingly cancels the amplitude spur. Then the combined spur magnitude decreases with increasing frequency; ideally at Nyquist the two spurs cancel out each other perfectly. From this, it follows that in a timing calibrated interleaved DAC the minimum attenuation of the amplitude error spur is 10 dB. This means that if a 50 dB SFDR is required, the amplitude difference between the two sDACs is allowed to be up to 1%, or slightly over 5 LSB for a 9 bit DAC.

Tuning of the duty cycle to get a sufficient SFDR can be done in multiple ways. For example [6] uses an array of capacitors followed by an SR latch to directly adjust the duty cycle of the clock signals. In our design, adjustable delay for the clocks is implemented via threshold voltage tuning of the multiplexer transistors. For this, the back gates of the FDSOI multiplexer transistors themselves are connected to a variable voltage; see Fig. 7: the wells for the transistors driven by SW+ are shared, as are those driven by SW−. Changing the back gate voltage modulates the threshold voltage of the multiplexer transistors which changes the turn-on and turn-off speed of the corresponding transistors which efficiently implements duty cycle tuning. Since there is no junction between the well and the source and drain areas, the back gates are allowed to be tuned between 0 V and 3 V, which implies a differential tuning range of −3 V to 3 V.

V. CIRCUIT IMPLEMENTATION DETAILS

The interleaving architecture significantly simplifies the sDAC design; since most of the dynamic errors are suppressed, the design is not as critical as that of regular DACs. Static errors are not suppressed by interleaving but do not have to limit performance at medium resolution and high speed.

Fig. 6 shows the implementation of the sDACs and their connections. Both of the 9 bit sDACs consist of six binary coded LSBs, and three thermometer coded MSBs, quad switches redirect their output current to either the positive or the negative output. The quadrature generation and switch drivers are implemented with standard core cells; together with the switches themselves and the requirement to have each cell as narrow as possible, this limits the maximum current that can properly be
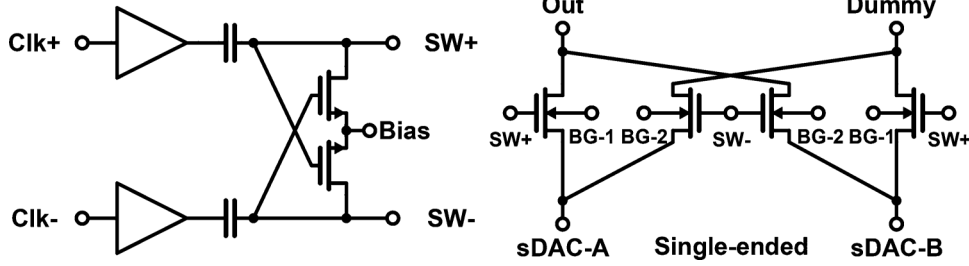
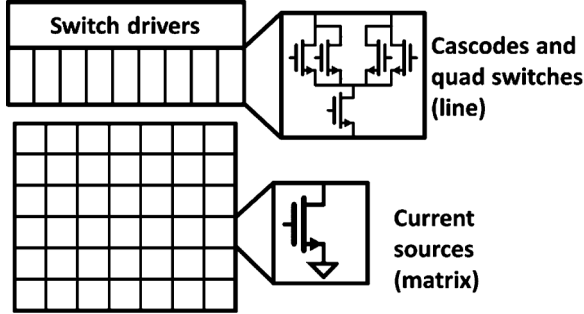Fig. 7.   Multiplexer level shifter and multiplexer (drawn single-ended).

Fig. 8.   sDAC layout.

Fig. 9.   Die photograph of the DAC core.

switched by each cell. This in turn determined the required segmentation of the DAC. The current source transistors of the two sDACs share a single bias to improve their matching, while their cascodes have split bias to improve isolation between the two halves.

In our design, the current sources are placed in a common centroid layout, with cascode transistors grouped together with the quad-switches and their drivers in a line-layout to minimize parasitics; see Fig. 8. This allows for relative large current sources, 1.5 μm/1 μm (W/L) for good matching and output resistance, with a small minimum length cascode transistor to obtain low parasitic capacitances.

The interleaving architecture suppresses the propagation of switching related errors to the DAC output which simplifies the generation of the switch signals. Both current mode logic (CML) and CMOS can be used to drive the current switches [5], [16]; both have specific advantages and disadvantages. Quad-switching combined with interleaving removes the need for most of the CML advantages, and using CML in combination with quad-switching is more complicated than using CMOS drivers. In our design, standard digital core cells are used to generate and buffer switch signals. These are area and power efficient, at the cost of a less than ideal switching waveform.

The multiplexer transistors need to be large enough to add only a small series resistance, while adding little parasitic capacitances. Each one of them is sized to be 65 μm wide and minimum length to obtain this. They are driven by an inverter chain that drives a capacitive level shifter; see Fig. 7. Since the level shifter directly drives the gate of the transistor, the bias voltage only needs to sink or source the leakage current of the capacitor and the gate leakage currents of the transistors. These currents are quite low, so the bias voltage can be generated by, e.g., a
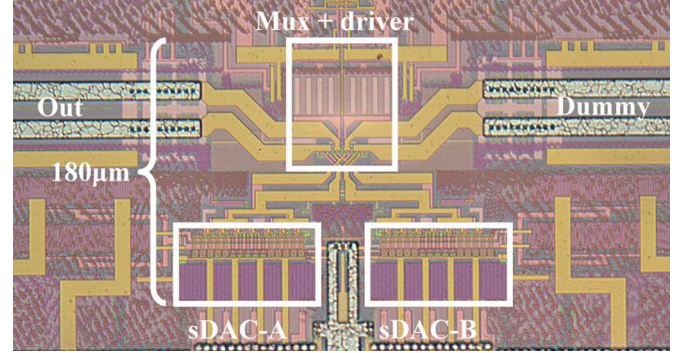
resistive voltage divider using high-ohmic resistors. Using this type of level shifter, the 'low' output voltage is within the nominal power supply, and no extra power supply is required.

VI. Test Chip

The 9 bit interleaved DAC was built in 28 nm FDSOI CMOS technology [12]. Compared to bulk CMOS, FDSOI can improve DAC performance due to mainly better matching and reduced source/drain to bulk capacitances. Fig. 9 shows the die photograph.

Both sDACs have a 63-word memory that provides a combined 126 word memory for test signals. Synchronization logic makes sure that after programming the memory, it will be read out in the correct order. Each sDAC occupies approximately 0.006 mm^2; the total DAC core area excluding memory is 0.04 mm^2. The DAC, excluding memory, consumes 110 mW from a single 1 V power supply source at its nominal speed of 11 GS/s. Both the regular output and the dummy output have a 50 Ω internal load in parallel to a 50 Ω external load. The bondwire inductances cause internal voltage peaks due to the high dI/dt of the DAC. While they cannot remove the peaks altogether, the internal 50 Ω resistors do limit their amplitude which improves performance. For measurement purposes the output is biased with a DC choke at 0.9 V. A signal swing of 425 mVpp-diff at DC was used during testing.

VII. Measurements

All measurements were performed at the nominal settings described in the previous section and after the timing was calibrated. Fig. 10 shows the measured output spectrum for a single tone full-scale signal at 4.6 GHz with an 11 GS/s sample rate.

TABLE I
COMPARISON TABLE

	This [12]	[17]	[14]	[6]	[16]	[18]	[11]
Tech	28nm FDSOI	28nm	180nm	65nm	65nm	65nm	180nm
Resolution [Bits]	9	13	14	12	9	6	14
Power [mW]	110	375	>600	70	60	750	2300
V_{supply} [V]	1.0	1.8	-1.5/1.8	1.2	1.2	1.1/2.5	1.8/3.3
Area [mm²]	0.04	1.16	4	0.4	0.04	0.24	5.2
Swing [$V_{pp-diff}$]	0.425	13.5dBm[b]	1.0	0.5	0.4	0.6	80mA[b]
Fs [GHz]	11	9	6	1.7	3	56	4.6
SFDR[a] [dB]	52	-	52	58	49	43	69[c]
IM3[a] [dBc]	-51	-44	-65	-62.5	-60	-	-74[c]

a) Worst-case reported SFDR/IM3 up to Nyquist/5.5GHz
b) No load impedance is reported: the voltage swing is unknown
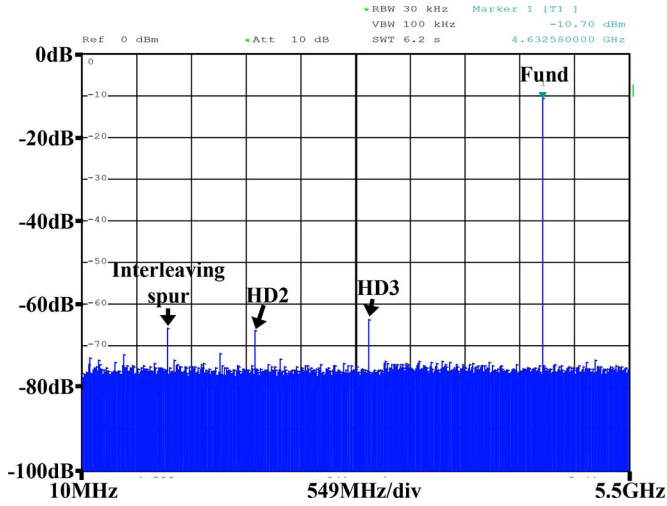c) SFDR is reported at 500MHz, IM3 up to 1GHz

Fig. 10. Measured output spectrum with 4.6 GHz full-scale sine output across Nyquist at 11 GS/s.
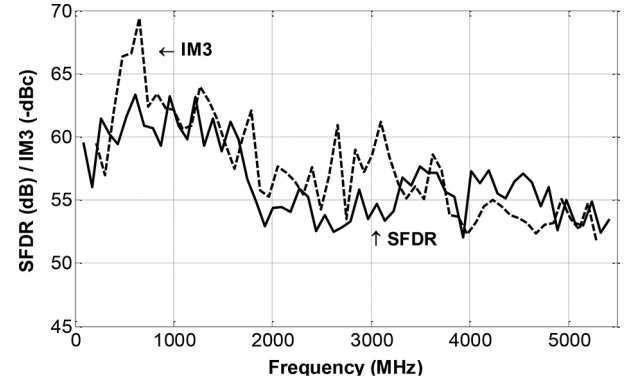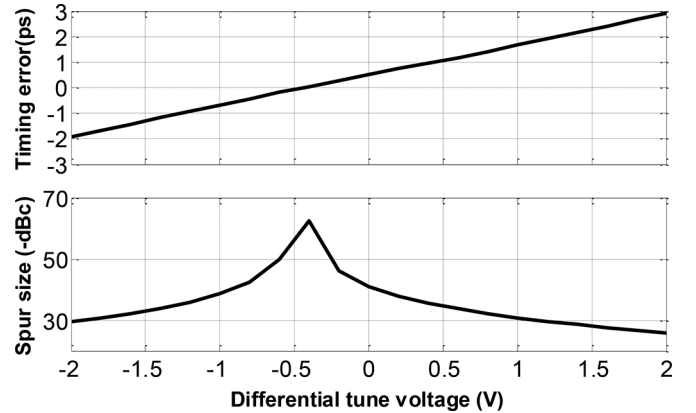

Fig. 11. SFDR and IM3 versus output frequency at 11 GS/s.

Fig. 12. Timing error and corresponding SFDR at Nyquist due to timing imbalance for different tune voltages.

Fig. 11 shows the measured SFDR and IM3 versus output frequency. Both the SFDR and IM3 stay respectively above 50 dB and below −50 dBc across Nyquist after timing calibration. At Nyquist, the fundamental is about 5 dB lower compared to its amplitude at DC, the majority of this drop is due to the sinc roll-off of the zeroth-order-hold.

Since the nonlinearities are largely due to the multiplexer transistors, the HD3 scales with 3 dB per dB increase in the fundamental and the HD2 tones with 2 dB. This limits the amplitude which can be obtained with an interleaved DAC with the multiplexer transistors residing in triode. Such a limitation does not exist for the output current, and by proper scaling it should be possible to increase the output power by delivering more current into a lower-ohmic output node, e.g., via a transformer.

The sensitivity of the timing adjustment was determined using the DC timing measurement discussed in Section IV. In FDSOI CMOS processes, the tuning range of back gates is much larger than that of transistors in bulk CMOS, and is much more linear. Fig. 12 shows the measured timing error and corresponding interleaving spur relative to the carrier at Nyquist for a (differential) tune voltage from −2 V to 2 V. This voltage is applied between the BG-1 and BG-2 connections shown in Fig. 7. While the process allows for a range of −3 V to 3 V, voltages above 2 V on the tune inputs result in a too low threshold voltage for proper operation. The sensitivity of the

timing adjustment is 1.2 ps/V, the (unselected) sample used for the measurement results in Fig. 12 has an uncalibrated error of 500 fs. The measured average and standard deviation of the timing error across all of our samples are respectively 0.65 ps and 0.75 ps which numbers include the errors due to amplitude imbalance. Similar to static timing errors, in the interleaved architecture also jitter on the data switches is isolated by the multiplexer, which will determine the overall jitter performance of the DAC. The jitter is related to the phase noise of the DAC output, which has been measured at −130 dBc/Hz for a 5 GHz carrier at 1 MHz offset. Noise generated by the current sources affect an interleaved DAC similar to a regular DAC.

The measured gain error between the two sDACs of the sample shown in the measurement plots was roughly 1.4 LSB on the full scale output. According to (4) this should result an image spur with a fundamental close to DC of 61 dB. The measured interleaving spur is at -63.5 dBc for a DC fundamental which is a little better than the theoretical value due to the extra suppression of the interleaving spur when the fundamental is close to DC due to bandwidth limitations. Over Nyquist the interleaving spur does not limit performance, with the worst case being -55 dBc; at Nyquist it is -60 dBc. Table I shows a summary of the performance and a comparison with state-of-the-art.

VIII. Conclusion

A 9 bit 11 GS/s DAC in 28 nm FDSOI CMOS technology is presented that uses two-times interleaving to obtain an SFDR above 50 dB across Nyquist and an IM3 below -50 dB across Nyquist, running on 110 mW from 1 V supply. This demonstrates that despite requiring two CS DACs in parallel and a multiplexer to combine those, the decrease in demands on the sDACs can result in an overall small and power-efficient DAC. Compared to state-of-the-art the measured SFDR is equivalent and the IM3 is a bit worse. However, the power consumption is a lot lower and also the core area is much smaller in this design. Triode switches and quad-switching yield additional reduction in demands on the power supply and bias generation, which allows a decrease in power and area while maintaining good linearity.

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