Compact Cascadable g_m-C All-Pass True Time Delay Cell With Reduced Delay Variation Over Frequency

Seyed Kasra Garakoui, Eric A. M. Klumperink, *Senior Member, IEEE*, Bram Nauta, *Fellow, IEEE*, and Frank E. van Vliet, *Senior Member, IEEE*

***Abstract*—At low-GHz frequencies, analog time-delay cells realized by LC delay lines or transmission lines are unpractical in CMOS, due to their large size. As an alternative, delays can be approximated by all-pass filters exploiting transconductors and capacitors (g_m-C filters). This paper presents an easily cascadable compact g_m-C all-pass filter cell for 1–2.5 GHz. Compared to previous g_m-RC and g_m-C filter cells, it achieves at least 5x larger frequency range for the same relative delay variation, while keeping gain variation within 1 dB. This paper derives design equations for the transfer function and several non-idealities. Circuit techniques to improve phase linearity and reduce delay variation over frequency, are also proposed. A 160 nm CMOS chip with maximum delay of 550 ps is demonstrated with monotonous delay steps of 13 ps (41 steps) and an RMS delay variation error of less than 10 ps over more than an octave in frequency (1–2.5 GHz). The delay per area is at least 50x more than for earlier chips. The all-pass cells are used to realize a four element timed-array receiver IC. Measurement results of the beam pattern demonstrate the wideband operation capability of the g_m-RC time delay cell and timed-array IC-architecture.**

***Index Terms*—All-pass filter, beam forming, beam squinting, CMOS, delay compensation, equalizer, phase shifter, phased array receiver, time delay, timed-array receiver, true time delay.**

I. Introduction

TIME DELAY circuits have broad applications in communication systems, e.g., for FIR and IIR filters [1], equalizers [2], and wide-band beam forming [3], [4]. This paper deals with the latter application, where a "timed array" is targeted instead of the more commonly used phased array. In a timed array, true time delays are used instead of the narrowband phase shifter approximation. In this way beam squinting can be minimized [4], [5]. In beam-forming receivers, the variable delay cells compensate the relative delay of signals of the antenna channels. The transfer function of an ideal delay cell is: $H(s) = e^{-s\tau}$ (Fig. 1). Its gain is 1 and its phase is linear versus frequency. The delay (τ) at frequency f_0 is: $\tau(f_0) = -\varphi(f_0)/2\pi f_0$, ideally independent of f_0 (linear phase). Note that we consider true time delay here, not group delay, which is defined as $-\partial\varphi/\partial\omega$. Achieving constant true time delay is tougher as it not only requires constant group delay independent of frequency but also a constant ratio between $-\varphi$ and ω independent of frequency [6]. There are different IC compatible circuits to approximate a time delay, e.g., transmission lines [7], [8], LC delay lines [9], switched capacitor delay circuits [10] and g_m-RC or g_m-C all-pass filters [10]. However, at low-GHz frequencies, transmission lines and LC delay lines in CMOS are unpractical due to the low quality factor of coils, loss of the transmission lines and their large sizes. Switched capacitor time-delay circuits on the other hand are not fast enough for low-GHz applications. One of the few remaining options is to exploit an all-pass filter approximation of a delay, e.g., a first-order all-pass filter:

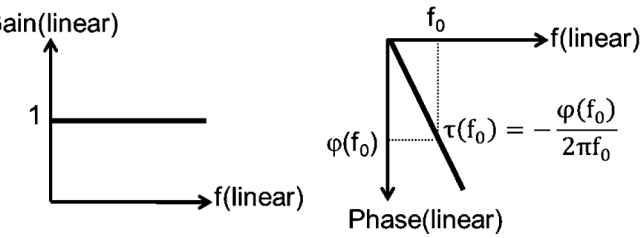

Fig. 1. The gain and phase transfer function of an ideal time delay cell.

$$H_{ap\_1}(s) = \frac{1 - s(\tau/2)}{1 + s(\tau/2)}. \tag{1}$$

The transfer function of this all-pass filter is plotted in Fig. 2. At low frequencies it approximates the ideal delay cell but at higher frequencies the delay is reduced and delay variations occur. This delay variation is quantified via the criterion $f_{\varphi=0}$ [6] which is the crossing point of the frequency axis and the tangent to the phase curve at operating frequency f_0 (Fig. 2). The delay variation in $\pm\Delta f$ around f_0 is approximately

$$\frac{\tau(f_0 \pm \Delta f) - \tau(f_0)}{\tau(f_0)} \approx \frac{\frac{f_{\varphi=0}}{f_0}}{1 - \frac{f_{\varphi=0}}{f_0}} \cdot \frac{\pm\Delta f}{f_0}. \tag{2}$$

The first-order all-pass transfer function can be realized both with g_m-RC filters [2], [11] (see Fig. 3) and the g_m-C filter presented in this paper and in [12]. In [13], a benchmarking method has been proposed to compare delay cells based on $f_{\varphi=0}$. This method is re-used here to show that the g_m-C delay cell of [12] has better performance than other published designs. Moreover, the feasibility of a compact broadband beam-forming IC with g_m-C delay cells is demonstrated. Apart from bandwidth, other important properties of the delay cell are: 1) cascadability; 2) compactness; 3) wide delay tuning range; 4) high

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The authors are with the University of Twente, CTIT Institute, IC Design Group, 7500AE, Enschede, The Netherlands (e-mail: kasra.garakoui@teledynedalsa.com).

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delay tuning resolution and precision; 5) gain controllability; 6) noise figure and 7) linearity. In [12] it has been shown that the g_m-RC all-pass filters of [2] and [11] (shown in Fig. 3) do not work adequately up to several GHz in UMC 180 nm CMOS because of their high parasitic capacitors. Besides, they need DC blocking capacitors or source-follower buffer circuits to realize cascadability, which limits the bandwidth and/or results in high current consumption. It will be proven that the g_m-C topology of [12] has better performance: 1) low delay variation over a 5x wider frequency band compared to other reported g_m-RC delay circuits, while maintain similar noise and nonlinearity performance; 2) compactness compared to LC or transmission lines; 3) high resolution of delay and gain tuning; 4) direct cascadability. Compared to [12], this paper adds circuit analysis and circuit optimization techniques, e.g., for phase linearization and bandwidth extension.

The structure of this paper is as follows. In Section II, the all-pass filter as an approximation of a delay cell is reviewed and the all-pass filter of [12] is explained. Section III assesses non-idealities of the delay cell. Section IV discusses improvements of its characteristics. Section V establishes a relation between requirements of the beam forming system and the delay cell. Section VI presents the sub-circuits of the timed-array IC and Section VII presents chip implementation and measurement results, while Section VIII draws conclusions.

II. First-Order All-Pass Delay Cell

The transfer function of the first-order all-pass filter of (1) can be rewritten as a combination of a low-pass part with DC-gain of two and a unity-gain part [14] as

$$H_{ap\_1}(s) = \frac{1 - s(\tau/2)}{1 + s(\tau/2)} = \frac{2}{1 + s(\tau/2)} - 1. \quad (3)$$

It is realizable without floating capacitors and hence with good bandwidth potential, because the low-pass part can be implemented by a capacitor to ground and the unity gain part does not require capacitors. Fig. 4 shows the block level and g_m-RC implementation of this all-pass filter. Aiming for direct cascadability, the g_m-C topology of Fig. 5 [12] with equal input and output DC voltages was proposed. Transistors M_1, M_4, M_5 and M_3 realize the low-pass signal path with a DC-gain of 2. Transistors M_2 and M_3 realize the inverting unity gain path. Using PMOS transistors in the "slow low-pass path" and faster NMOS transistor in the unity gain path, the useful frequency range of the delay cell is maximized. Also, current re-use for NMOS and PMOS transistors reduces power consumption. The DC input voltage $V_{in,DC}$ results in equal drain currents I_{DC} in M_1, M_2, M_3 and M_4, and $2I_{DC}$ for M_5. Therefore, $V_{out,DC} = V_{in,DC}$. Modelling M_4 by its small-signal g_{m4} and C as the total capacitance, the transfer function and its low frequency delay can be written as:

$$H(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{1 - \frac{sC}{g_{m4}}}{1 + \frac{sC}{g_{m4}}} \quad (4)$$

$$\tau_{LF} \approx 2C/g_{m4}. \quad (5)$$

The low-frequency delay is made controllable by splitting C in switchable binary weighted capacitors. Fig. 6 shows the bias

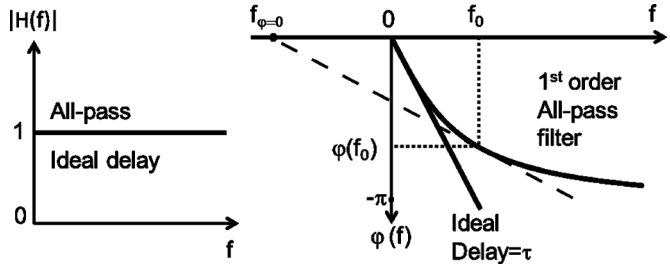

Fig. 2. First-order all-pass filter with extrapolation point $f_{\varphi=0}$ versus ideal delay (linear scales).

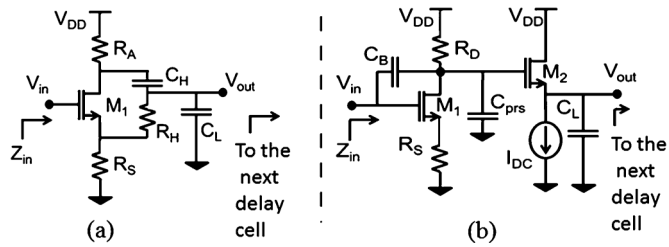

Fig. 3. Two known g_m-RC delay circuits: (a) of [11] and (b) of [2].

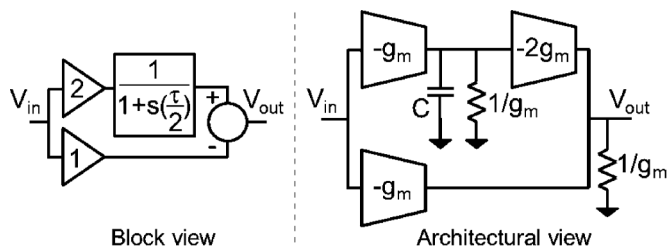

Fig. 4. The block view and architectural view of the first-order all-pass filter implementable with no floating caps.

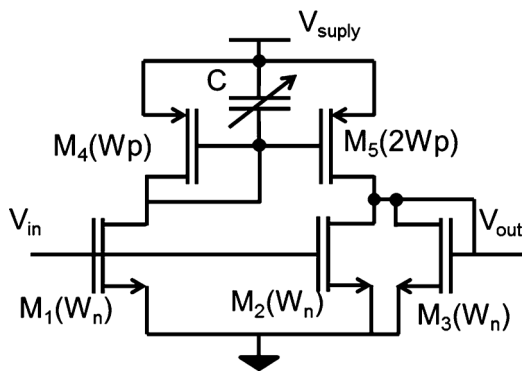

Fig. 5. The proposed first-order g_m-C all-pass filter in [12].

circuit of the first delay cell of a delay line. It is the only cell with an AC-coupling capacitor to the input RF signal, $V_{in,RF}$. As each signal path has this, no difference in gain and delay results. The DC voltage of V_{out} is equal to $V_{DC,bias}$. R_b is made more than 10 times larger than the source impedance of $V_{in,RF}$, for insignificant attenuation.

III. The Non-Idealities of the Delay Cell

As the aim is to cascade cells, the non-idealities of a delay cell will now be analyzed with a capacitive load equal to the input capacitance of the next delay cell: $C_{gs,M1} + C_{gs,M2}$. In the

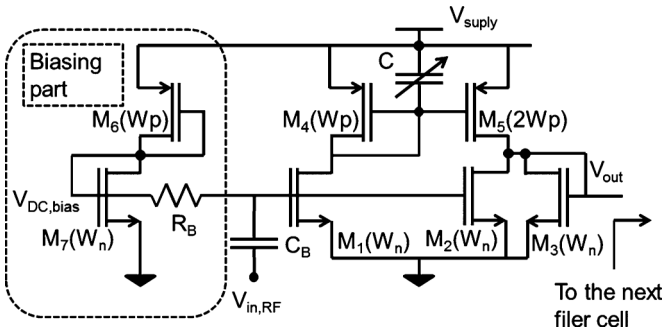

Fig. 6. The biasing circuitry of the first filter cell in a cascade line.

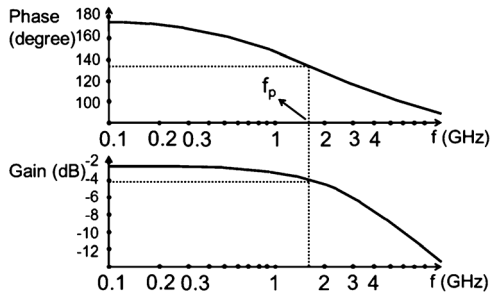

Fig. 7. The phase at the gate of M_5, and the output of the delay cell in a delay line.

analysis the effect of C_{gd} will be neglected as the voltage gain is low (unity gain all-pass behavior), while the right half-plane zero introduced by at g_m/C_{gd} is in the range of 50 GHz for the transistors used. This is well beyond the targeting low-GHz operating frequency, and therefore for the sake of simplicity we neglected its effect. This assumption was validated by checking hand calculation versus simulation results.

A. Finite Output Impedance and Parasitic Capacitances

Considering finite output impedances of the transistors and the parasitic capacitors which affect the pole/zero frequency and DC gain, the transfer function of the filter becomes:

$$H(s) = \frac{1}{1+\frac{2}{g_{mn}}(g_{dsn}+g_{dsp})} \cdot \frac{1-\frac{1}{g_{mp}}(g_{dsn}+g_{dsp})}{1+\frac{1}{g_{mp}}(g_{dsn}+g_{dsp})} \cdot \frac{1-\frac{sC}{[g_{mp}-(g_{dsn}+g_{dsp})]}}{1+\frac{sC}{[g_{mp}-(g_{dsn}+g_{dsp})]}} \cdot \frac{1}{1+\frac{sC_L}{[g_{mn}+2(g_{dsn}+g_{dsp})]}} \quad (6)$$

where g_{mn} and g_{dsn} are the transconductance and output conductance of M_1, M_2 and M_3 in saturation, g_{mp} and g_{dsp} those of M_4 and $2g_{mp}$ and $2g_{dsp}$ of M_5. The parasitic capacitances $C_{gs,M4}$, $C_{gs,M5}$, $C_{db,M4}$ and $C_{db,M3}$ are absorbed in C. Also C_L absorbs the parasitic capacitors $C_{gs,M3}$, $C_{db,M5}$, $C_{db,M2}$, $C_{db,M3}$ plus the input capacitance of the next delay cell $(C_{gs,M1}+C_{gs,M2})$. The transfer function (6) deviates from the ideal one (4) in two aspects: 1) the DC-gain is less than unity, and 2) an extra high frequency pole causes both an extra phase shift and a high frequency gain roll-off. If the following conditions are satisfied:

$$g_{mn} \gg 2(g_{dsn}+g_{dsp}) \quad (7a)$$

$$g_{mp} \gg 2(g_{dsn}+g_{dsp}) \quad (7b)$$

then the transfer function can be rewritten as

$$H(s) = \frac{1-\frac{2}{g_{mp}}(g_{dsn}+g_{dsp})}{1+\frac{2}{g_{mn}}(g_{dsn}+g_{dsp})} \cdot \frac{1-\frac{sC}{g_{mp}}}{1+\frac{sC}{g_{mp}}} \cdot \frac{1}{1+\frac{sC_L}{g_{mn}}}. \quad (8)$$

Using the analysis in [13], the maximum usable pole frequency f_p is defined as the frequency where the gain roll-off with respect to DC is less than ΔH_p, resulting in

$$f_p \le \frac{g_{mn}}{2\pi C_L}\sqrt{\frac{1}{(1-\Delta H_p)^2}-1}. \quad (9)$$

For frequencies larger than f_p, the roll-off is more than ΔH_p. Substituting $C_L \approx C_{gs,M1}+C_{gs,M2}+C_{gs,M3} = 3C_{gs,M1}$ and $f_{t,M1} \approx g_{mn}/2\pi C_{gs,M1}$ (unity current gain) in (9) results in

$$f_p \le \frac{f_{t,M1}}{3}\sqrt{\frac{1}{(1-\Delta H_p)^2}-1}. \quad (10)$$

To estimate f_p and compare it with the delay cells reported in [2] and [11] (benchmarked in [13]), the same technology (UMC 180 nm CMOS), same $\Delta H_p = 1$ dB and same $f_{t,M1} = 12.4$ GHz for the NMOS transistors have been used. The choice $\Delta H_p = 1$ dB is only for comparison to [13], and it will be reduced in Section IV where several delay cells will be cascaded. Substituting the values in (10), the result is $f_p \le 2$ GHz, which is a 4x improvement compared to other circuits in [13]. Fig. 7 shows the simulation results of the delay cell. Reading f_p as the frequency where 45° phase shift occurs w.r.t. DC, we find $f_p \approx 1.7$ GHz and a gain roll-off of ≈ 1.5 dB at f_p which is due to the parasitic capacitor effects at the output of the cell. Also the DC gain is not 0 dB due to the finite output impedances of transistors. In Section IV, the DC-gain will be calibrated to 0 dB and the useful frequency range is increased further to 5x (up to 2.5 GHz) that of other reported g_m-RC all-pass delay cells.

The operating bandwidth is limited to f_p, to keep the gain roll-off less than ΔHp. Within the operating bandwidth, the value of the true time delay and group delay mainly depends on f_p, but may also be affected by the -3 dB gain-roll-off frequency f_{-3dB} due to the parasitic pole at the output. Because f_{-3dB} $(\approx f_{t,M1}/3)$ is much larger than f_p, a linear phase approximation can be made. This causes both a constant time delay shift and group delay shift equal to $1/2\pi f_{-3db}$. Equation (11) shows expressions for both the total true time delay (τ) and group delay (τ_g) of the delay cell:

$$\tau \approx \frac{2\tan^{-1}\frac{f}{f_p}}{2\pi f}+\frac{1}{2\pi f_{-3dB}} \quad (11a)$$

$$\tau_g \approx \frac{f_p}{\pi\left(f^2+f_p^2\right)}+\frac{1}{2\pi f_{-3dB}}. \quad (11b)$$

In both equations, the second term is much smaller than the first term.

B. Nonlinearity

The nonlinear V-to-I conversions in M_1 and M_2 can be compensated by the I-to-V function of M_3, which are inverse functions. Also, the mirror M_4 and M_5 with gain 2 ideally renders an

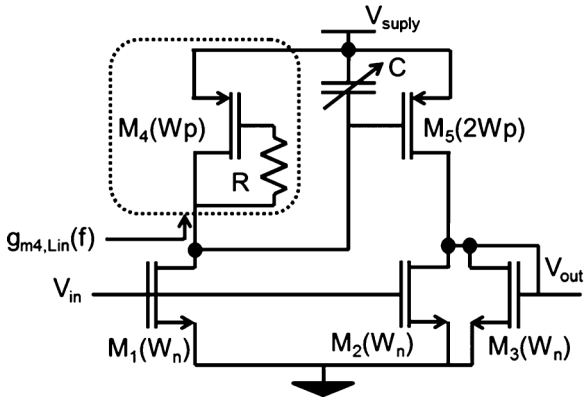

Fig. 8. The phase linearization technique.

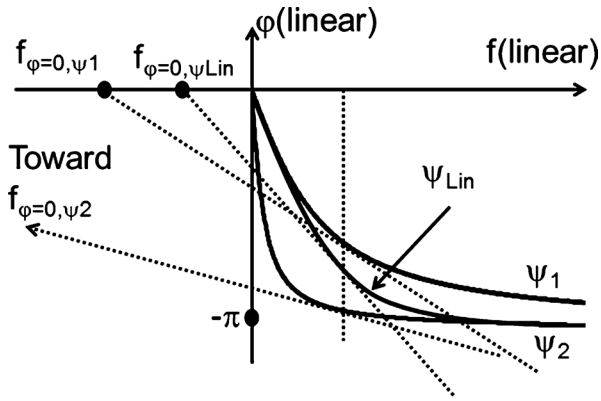

Fig. 9. Low-frequency linearization technique of the phase transfer curve of the filter (conceptually depicted).

inverse function nonlinearity compensation. However, reactive harmonic distortion [15] occurs at frequencies well below the pole frequency. The I–V conversion by $\mathrm{M_4}$ becomes more linear for higher frequencies, as the (linear) capacitor starts to dominate the I–V conversion instead of the square-root I–V function due to diode connected transistor $\mathrm{M_4}$. As the V–I conversion of $\mathrm{M_5}$ remains nonlinear (quadratic for long transistors), the overall function is nonlinear. Due to the phase shifts caused by capacitor C, the nonlinearity compensation between $\mathrm{M_1}$, $\mathrm{M_2}$ and $\mathrm{M_3}$ is degraded. Therefore, the nonlinearity of the filters cell increases by increasing the frequency.

C. Thermal Noise

The input-referred thermal noise of the delay cell can be written as

$$\overline{v_{\mathrm{in}}^2} = 8\ \mathrm{kT}\gamma\left(\frac{\mathrm{g_{mn}}+\mathrm{g_{mp}}}{\mathrm{g_{mn}^2}}\right)\left[\frac{3\mathrm{g_{mp}^2}+(\mathrm{C}\omega)^2}{\mathrm{g_{mp}^2}+(\mathrm{C}\omega)^2}\right] = 8\mathrm{kT}\gamma\left(\frac{\mathrm{g_{mn}}+\mathrm{g_{mp}}}{\mathrm{g_{mn}^2}}\right)\left[\frac{3\left(\frac{\mathrm{f_p}}{\mathrm{f}}\right)^2+1}{\left(\frac{\mathrm{f_p}}{\mathrm{f}}\right)^2+1}\right] \quad (12)$$

where γ is the noise excess factor of a MOSFET. As (12) shows, the input-referred noise is frequency-dependent. In a delay line of *n* cascaded delay cells with unity gain, the total input-referred noise power is *n* times the noise of each individual delay cell. Therefore, in systems with variable numbers of cascaded delay cells, the total noise figure will be delay-dependent.

D. PVT Sensitivity

Process, voltage and temperature (PVT) variations may affect the gain and amount of the delay of each delay cell. Due to mismatch and the finite output impedance of the transistors, the DC gain of the delay cell is not exactly one. In cascaded cells, these errors add up. A tuning mechanism for DC gains is addressed in Section IV. Moreover, just as for any $\mathrm{g_m}$-C filters, there will be spread in the filter time-constant and hence delay due to PVT. Using master-slave techniques [16], these variations can be cancelled largely, e.g., by using replicas of the delay cell in an oscillator loop, and tuning its frequency equal to a well-known reference frequency.

IV. Delay Cell Enhancements

We will now describe some techniques to reduce true time delay variation (make the delay more constant over the frequency band), extend bandwidth, and (fine-) tune the delay and gain.

A. Phase Linearization (Small Delay Variations)

It is shown below that adding a resistor R between the gate and drain of $\mathrm{M_4}$ (Fig. 8) improves the linearity of the phase transfer function in a limited frequency band. This can be considered as "inductive peaking" that is often used in wideband amplifiers for equalization of the gain [17]. Here, its purpose and optimization targets phase linearity and low $\mathrm{f}_{\varphi=0}$, to minimize delay variation. The conductance $g_{m4,\mathrm{Lin}}$ of the linearized-phase circuit inside the dashed rectangle in Fig. 8 is

$$\mathrm{g_{m4,Lin}(S)} = \mathrm{g_{m4}}\cdot\frac{\frac{\mathrm{sC_{gsM4}}}{\mathrm{gm4}}+1}{\mathrm{sRC_{gsM4}}+1}. \quad (13)$$

Its value for very low and very high frequencies is $\mathrm{g_{m,LF}} \approx \mathrm{g_{m4}}$ and $\mathrm{g_{m,HF}} \approx 1/\mathrm{R}$, respectively. As is shown conceptually in Fig. 9, the phase transfer function of the linearized delay cell ψ_{lin} shows a smaller value of $\mathrm{f}_{\varphi=0}$ compared to two other phase transfer functions ψ_1 and ψ_2. Hence, not only is the variation in group delay reduced, but also the variation in true time delay (low $\mathrm{f}_{\varphi=0}$). This happens for a certain optimum value of R. For low frequencies, the phase curve is similar to that of an all-pass cell with its pole/zero at $\pm\mathrm{g_{m4}}/2\pi\mathrm{C}$ (curve ψ_1), while for high frequencies it follows the phase curve of a cell with pole/zero at $\pm 1/2\pi\mathrm{RC}$ (curve ψ_2). For intermediate frequencies the phase curve is an interpolation between the two lines ψ_1 and ψ_2. A proper value of R found through parametric simulations results in a curve (ψ_{Lin}) with a minimum amount of the delay variations in a band $\pm\Delta\mathrm{f}$ around $\mathrm{f_0}$, i.e., a minimum value of the criterion $\mathrm{f}_{\varphi=0}$ (see (2)) [5], [6]. Note that closer proximity of $\mathrm{f}_{\varphi=0}$ to zero corresponds to less delay variation versus frequency. Fig. 10 shows simulated phase curves with R as a parameter. The process technology used is now 160 nm CMOS, and Table I lists the circuit parameters. $\mathrm{f}_{\varphi=0}$ is evaluated at operation frequency of 1.75 GHz (in the middle of the band 1–2.5 GHz). $\mathrm{f}_{\varphi=0}$ varies improves from -0.52 GHz for $\mathrm{R} = 0\ \Omega$ to -0.06 GHz for $\mathrm{R} = 1.5\ \mathrm{k}\Omega$ (optimum). In terms of

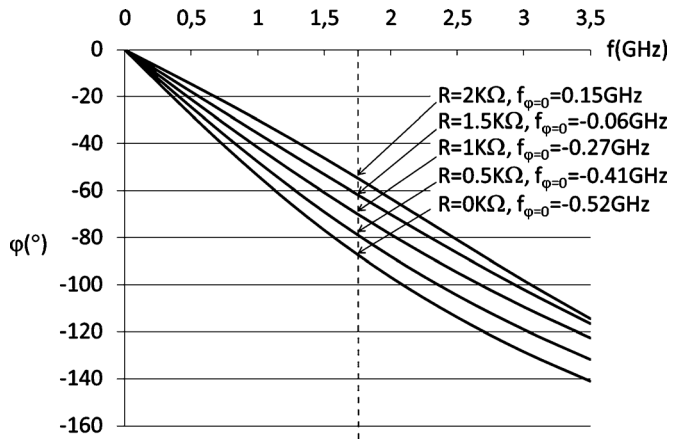

Fig. 10. Simulation results of the phase linearization technique for the parameters shown in Table I.

delay variation over 1–2.5 GHz, using (2), a delay variation reduction from 9.8% for $R = 0$, to 1.4% for $R = 1.5$ kΩ is found. The phase linearization resistor increases the noise figure of the delay cell by about 1.7 dB.

B. Bandwidth Extension

The load capacitor plus the parasitic capacitors at the output of the delay cell ($\approx C_L + C_{gs3}$) cause an unwanted pole and, consequently, gain roll-off plus an extra amount of delay. In a cascade of identical delay cells, the total load plus parasitic capacitance at the output node is $3C_{gs,M1}$. Therefore, the parasitic pole at output is: $f_{p,out} \approx g_{m3}/(6\pi C_{gs,M1})$. An active inductive peaking technique [18] is used for bandwidth extension by adding resistor R_{BWE} to convert the diode-connected transistor M_3 to an "active inductor" (Fig. 11). The impedance of the active inductor (the part inside the dotted box) is

$$Z_{A-ind}(s) = \frac{1}{g_{m3}} \frac{sR_{BWE} \cdot C_{gs,m3} + 1}{s\frac{C_{gs,M3}}{g_{m3}} + 1}. \qquad (14)$$

Choosing $R_{BWE} = 1/g_{m3}$ results in $Z_{A-ind} = 1/g_{m3}$. Therefore, the pole at the output becomes $f_{BWE} = g_{m3}/(4\pi C_{gs,M1})$ which means 50% bandwidth extension. Fig. 12 shows the gain curve with R_{BWE} as a parameter. The transistor parameters are the same as in Table I. Theoretically, 50% bandwidth extension happens at R_{BWE} $(= 1/g_{m,M3}) = 298$ Ω; however, because of extra parasitic capacitance due to $C_{db,M2}, C_{db,M5}, C_{db,M3}$, $C_{gd,M2}, C_{gd,M3}$ and $C_{gd,M5}$ and also finite output impedances of M3, M2 and M5, simulation shows a 33% bandwidth extension. The DC gain drop of -2 dB is caused by the finite output impedance of the transistors. The bandwidth extension resistor (R_{BWE}) increases the noise figure of the delay cell by about 0.6 dB. In the following subsections, a technique is introduced to compensate the DC gain drop.

C. Binary Tuning of the Delay

Referring to (5), delay can be fine-tuned by varying C, which is designed as a 3 bit switchable binary weighted capacitor bank (see Fig. 13). Because all capacitors of the bank are AC-grounded, referred to V_{supply}, they are easily switchable with PMOS transistors.

TABLE I
THE TRANSISTOR PARAMETERS OF THE SIMULATED DELAY CELL

	W/L(μm/μm)	V_{th}(V)	I_D(μA)	V_{GS}(V)	V_{DS}(V)
M_1	13.76/0.25	0.465	488	0.714	0.714
M_2	13.76/0.25	0.465	488	0.714	0.714
M_3	13.76/0.25	0.465	488	0.714	0.714
M_4	10.64/0.25	0.449	488	1.086	1.086
M_5	21.28/0.25	0.449	976	1.086	1.086

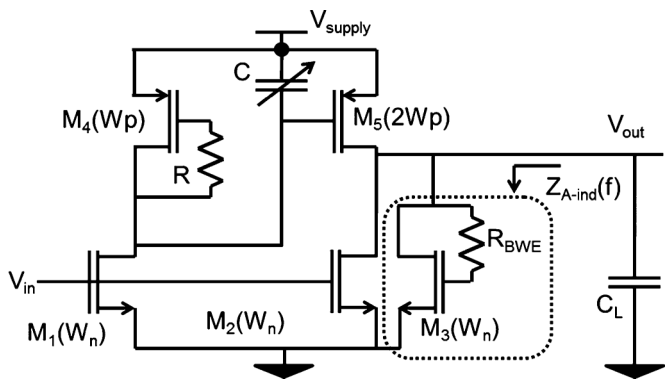

Fig. 11. Bandwidth extension of the filter.

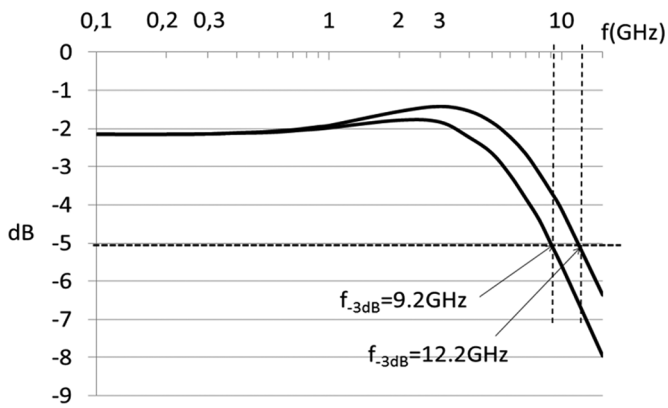

Fig. 12. Simulation of bandwidth extension technique (R_{WBE} as a parameter).

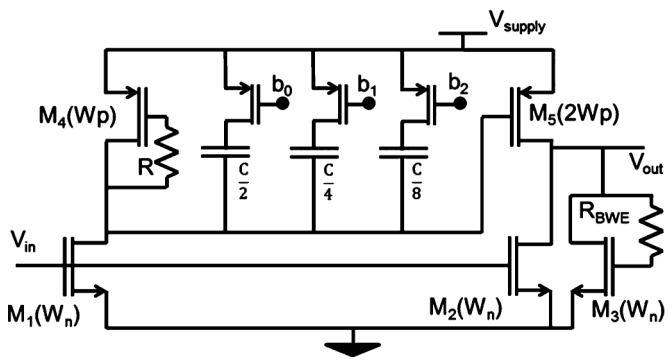

Fig. 13. The delay cell with 3 bit delay selection.

D. Gain Adjustment

The practically achieved DC-gain of the filter is less than one because of the finite output impedance of the transistors (refer to (6)). In a delay line gain errors add up and there may be a need to calibrate the gains to unity. For this purpose, a switchable

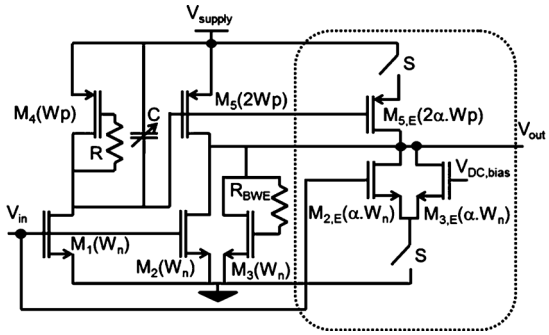

Fig. 14. Adding gain tuner to the delay cell.

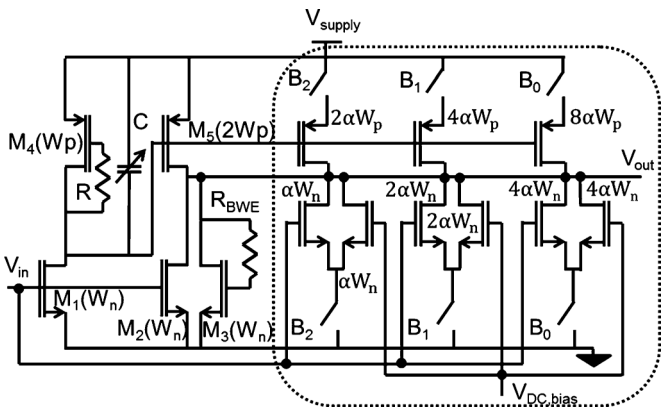

Fig. 15. Adding 3 bit gain calibration to the filter.

structure consisting of $M_{2,E}$ and $M_{3,E}$ and $M_{5,E}$ has been added (Fig. 14). $M_{2,E}$ and $M_{5,E}$ work in parallel with M_2 and M_5 to increase their effective width by an amount equal to αW, so that the DC gain is multiplied by $1+\alpha$. Transistor $M_{3,E}$ sinks the excess DC current at the output point to keep the DC output bias voltage unchanged. $V_{DC,bias}$ is re-used from the biasing circuit (refer to Fig. 6).

A set of binary weighted switchable gain tuning stages makes the tuning more precise (Fig. 15). Three bits have been used for the DC-gain tuning in a gain-range of 3 dB (LSB $\approx$ 0.4 dB). Table II shows a comparison between the simulated results of this work and the simulated results of other reported g_m-RC delay cells (refer to Fig. 3). The technology used in every case is UMC 180 nm to compare to [13]. The V_{GS} of NMOS transistors for all circuits are the same to maintain equal $f_{t,n} = 12.4$ GHz for fair comparison. As the table shows, the pole frequency of this work is much higher (more than $5\times$) than other works. The NSNR [15] (defined as SNR/P@IM3 = 1%) criterion of the cells at 0.1 GHz bandwidth was used to compare dynamic range. The NSNR of this work is 1 dB better than [11] and 6 dB less than [2], partly due to IIP_3, but mainly due to the number of noise contributing devices of the new delay cell [12]. Clearly, the strongest point of this work is its frequency range, which is much better than for other circuits in the same technology.

V. Beam-Forming System Design

In this section, the timed-array system specifications are related to the delay cell requirements. The formulas of this section are used in Section VII to find the specifications of the sub-blocks in timed-array antenna systems. Suppose we aim at N antenna elements, a frequency band from f_{min} to f_{max}, a maximum steering angle $\pm\theta_{max}$ w.r.t. the bore-sight and b bits of spatial steering resolution, while the required noise figure is less than NF_{max}. No grating lobes should exist and < -40 dB null depth is targeted. From these specifications, system design parameters are extractable using [3] and [4], like the distance between antenna elements, maximum required delay, number of delay steps, and the noise figure of each channel.

To avoid grating lobes, the distance between antenna elements (d) must be less than half the wave length at the maximum operating frequency (f_{max}):

$$d \le \frac{\lambda_{fmax}}{2}. \tag{15}$$

The noise figure for N antennas improves with 10log(N) [dB] w.r.t. the noise figure for a single antenna channel. The maximum required delay per channel (τ_{max}) depends on: 1) the number of antenna elements (N), 2) the distance between antenna elements (d), and 3) the maximum steering angle (θ_{max}). It can be expressed as [4]:

$$\tau_{max} = (N-1)\frac{d\cdot\sin(\theta_{max})}{c} \tag{16}$$

(c is the speed of the waves in the space.) The minimum delay steps (τ_{min}) depend on: 1) distance between antenna elements (d), 2) maximum steering angle (θ_{max}) and 3) spatial resolution in bits (b):

$$\tau_{min} = \frac{d\cdot\cos(\theta_{max})}{C}\cdot\frac{\theta_{max}}{2^{b-1}}. \tag{17}$$

The null depths are ideally equal to $-\infty$, but gain mismatch will decrease the null depths. Timed-array system simulations shows that for a four-antenna array and null depths less than -40 dB, less than 0.06 dB gain difference between the channels is required.

TABLE II
Comparison Between Simulated Delay Cells

	Fig.3a [11]	Fig.3b [2]	This work
$V_{GS,nmos}$ (V)	0.714	0.714	0.714
$V_{GS,pmos}$ (V)	-	-	1.086
$V_{th,nmos}$(V)	0.427	0.427	0.427
$V_{th,pmos}$(V)	-	-	0.449
I_{DC} (mA)	0.2	3.4	0.6
Pole f_p (GHz)	0.36	0.48	2.63
Input referred noise @f_p (nV/sqrt(Hz)	12.8	2.4	6.2
IIP_3 (dBm@50Ω) @f_p	3	5	3
$V_{IM3=1\%}$ (mV)	48	84	45
SNR @ IM3=1% in BW=0.1GHz	52	71	57
Normalized SNR/P (1%IM_3,1Hz,1mW [20])	138	145	139

VI. Four-Channel Wide-Band Beam-Forming IC

The designed delay cell is the basic building block of the time-delay-based timed-array antenna IC. The IC has four antenna channels (Fig. 16) [12]. Each channel applies adjustable

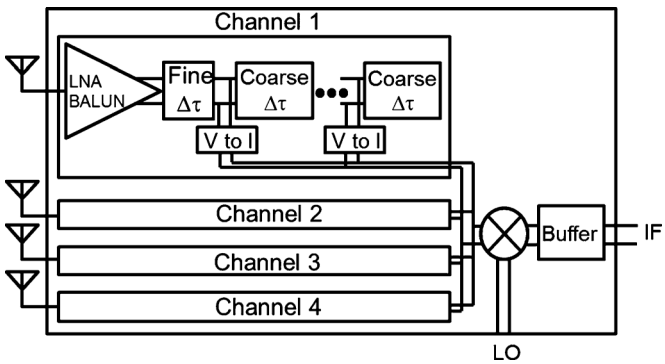

Fig. 16. The timed-array IC: block level [12].

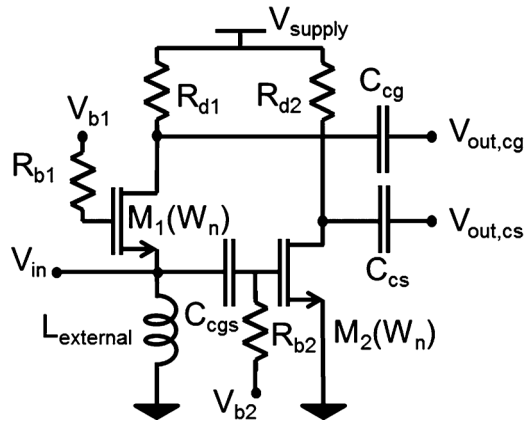

Fig. 17. LNA/BALUN.

delay and gain on the input signal. As shown in Fig. 16, the adjustable delay is a combination of "Fine $\Delta\tau$" cells cascaded with "Coarse $\Delta\tau$" delay cells. The "Fine $\Delta\tau$" is realized by a cascade of three delay cells with small delay steps (refer to Fig. 13). Each "Coarse $\Delta\tau$" is a cell with large delay steps (refer to Fig. 15). In Section VII, it will be shown that 550 ps total delay has been realized in a 5 bit delay resolution via "Fine $\Delta\tau$" and six cascaded "Coarse $\Delta\tau$" cells. The last "Coarse $\Delta\tau$" cell acts as a termination. An LNA/BALUN precedes the delay chain to reduce the noise figure. The output signals of the lines are added to each other to complete the beam-forming function. Then the signal is down-converted to IF via a mixer and external LO. The total noise of the chip depends on the beam direction because the amount of the delay at each channel (number of cascaded coarse $\Delta\tau$ cells) changes with the beam direction. The maximum noise figure occurs when the beam directs toward the maximum steering angle $\theta_{\max}$. In this case, the average delay of the channels is at maximum.

Analysis based on a Taylor series expansion shows that distortion has only minor impact on the phase of the fundamental frequency. Therefore, the position of the null and its depth do not change much. However, strong signals may also generate higher harmonics with different phases than the fundamental signal in each antenna channel. After summation, the amplitude of the harmonics can add up and cause high-frequency interference even if a signal comes from a null direction. Whether this is a problem depends on specific requirements and boundary conditions which are outside the scope of this paper. Next, the functionality and circuit structure of the sub-blocks are explained.

A. LNA/BALUN

The LNA/BALUN has four main functions: 1) antenna impedance matching, 2) low noise amplification, 3) single-to-differential conversion (BALUN), and 4) gain tuning. The single-to-differential conversion makes the signals less sensitive to interference from other channels. It exploits a noise-cancelling common-gate (CG)–common-source (CS) structure (Fig. 17) [19]. The DC blocking capacitors C_{cg}, C_{cs} and C_{csg} are the only series capacitors in each channel. Due to a design error, their parasitic capacitance to the substrate is the main cause of the bandwidth limitation. $V_{out,cg}$ and $V_{out,cs}$ are DC fed to the "Fine $\Delta\tau$" block. The AC gain in CG, CS stages of the LNA/BALUN can be trimmed by controlling bias voltages V_{b1} and V_{b2} to provide gain equalization and calibration. A 4 bit DAC is used to cover 1 dB gain variation with 0.06 dB as LSB step. This small range hardly degrades S_{11} (it remains less than -10 dB) but provides the required gain resolution to provide < -40 dB null depths.

B. Fine Delay Control

The Fine $\Delta\tau$block realizes small delay steps. It consists of three cascaded delay adjustable cells (Fig. 13), to cover one coarse delay step with extra margin for PVT, to prevent "missing bits". The gain of the fine $\Delta\tau$ blocks are the same for all antenna channels, therefore, it does not affect the beam pattern and consequently they do not require gain calibration.

C. Coarse Delay Control

The Coarse $\Delta\tau$ delay line consists of six cascaded delay cells, each with a fixed delay and an adjustable amount of gain. At each (voltage) output of a coarse delay cell, there is a V–I converter (see Fig. 16) which can be activated or not. This acts as a selectable tap to effectively change the length (and the delay amount) of the delay line. The gain adjustability of the stages is to calibrate the gain of the coarse delay line to unity, independent of the number of cascaded blocks.

D. Selectable V–I Converters

The selectable V–I converters fulfill two tasks: They select the desired output of the delay chain and they convert the signal from voltage to current. The input capacitance of the V–I converter has an effect on the delay of the channel, but because this delay shift is equal for all channels, it does not affect the beam pattern. However, they limit the bandwidth. Because the signals are converted to current, the summation function required for beam forming can be implemented by simply connecting all outputs together.

E. LO, Mixer and Output Buffer

An external differential LO is used to down-convert the beam-formed signal to IF. The circuit and its outputs are differential and an active Gilbert-cell mixer is used with load resistors. The output voltage is buffered via source followers to match the output impedance to 50 Ω.

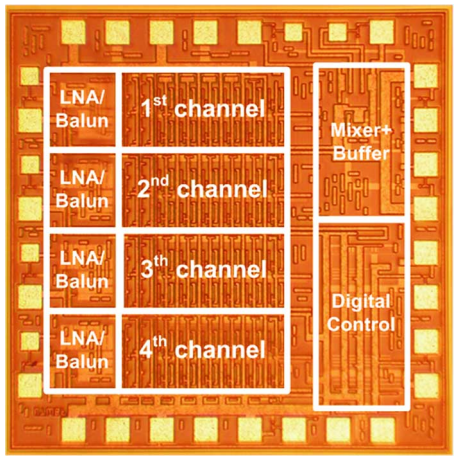

Fig. 18. Chip photograph.

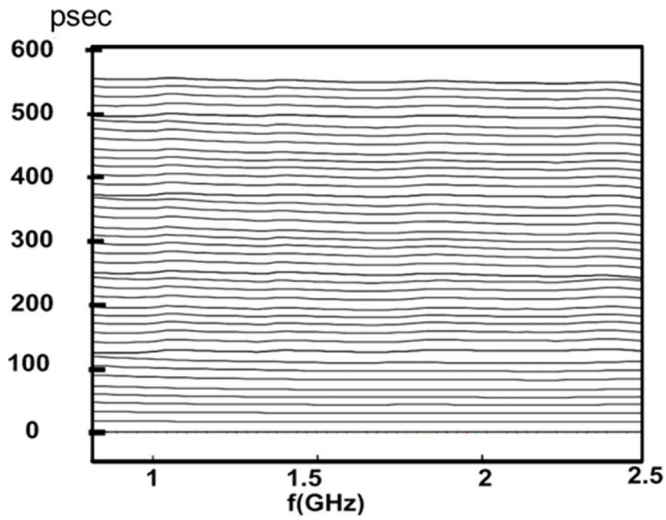

Fig. 19. Delay versus frequency for all delay settings.

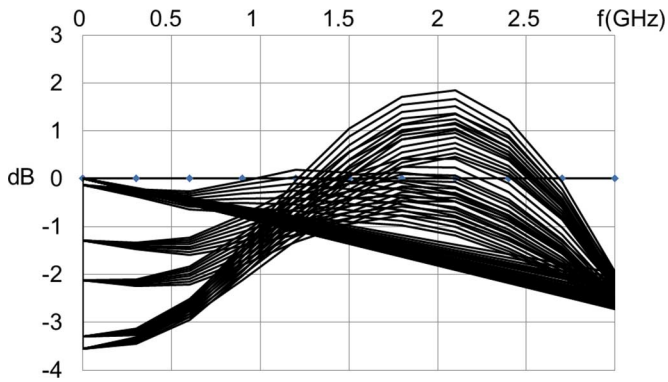

Fig. 20. Gain of the delay line (fine tune and coarse tune) versus f for all delay settings.

VII. Chip Implementation and Measurements

To demonstrate wideband beam-forming, a four-channel beam-forming chip was designed in 160 nm CMOS, covering more than one octave of bandwidth from 1 GHz to 2.5 GHz. The beam can be steered from -60° to 60° related to bore-sight in 4 bits resolution. To avoid grating lobe conditions, the required inter-element antenna distance is $0.5\lambda_{2.5\,\mathrm{GHz}} \approx 6$ cm (refer to (15)). The maximum required delay in each channel is found from (16) and is $\tau_{\max} = 510$ ps. The delay step size is derived from the 4 bit beam-steering resolution (refer to (17)): $\tau_{\min} \approx 13$ ps. The $\tau_{\max}$ to $\tau_{\min}$ ratio shows that for 4 bit steering angle resolution, 5 bit delay resolution is needed per channel. The targeted average noise figure of the channels when the beam steers towards $\theta_{\max} = \pm 60^\circ$ is 8 dB at the mid of the frequency range ($f_0 = 1.75$ GHz), i.e., the noise figure of each channel at 255 ps delay must be 8 dB. The 255 ps delay consists of three cascaded coarse $\Delta\tau$ cells besides fine $\Delta\tau$. A single-ended-to-differential voltage gain of 13 dB for each channel and 3.5 dB noise figure for the LNA/BALUN theoretically results in 8.9 dB noise figure for every individual delay cell. Keeping the overdrive voltage of the transistors similar to Table I results in 3.6 mA current for each individual delay cell. In this test chip, the simple bias circuit of Fig. 6 consisting of a diode connected N- and PMOS was used. Reduction of the supply directly decreases the current and consequently affects the g_m, noise and time-delay of the delay cell. To stabilize performance, either a voltage regulator will be needed, or a bias current source should be used to bias M6 and M7 in Fig. 6. Fig. 18 shows the chip photograph. For each channel, the delay versus frequency over the whole frequency band and for all settings was measured. An effective number of bits for the delay setting equal to ENOB $= 4.7$ (NOB $= 5$) was found (Fig. 19). The delays are approximately constant within <10 ps variation in the operating frequency band of 1–2.5 GHz. The flatness of the delay curves in Fig. 19 is an immediate result of applying the technique in Figs. 9 and 10 to linearize the phase versus frequency and demonstrates that the optimization approach is highly effective. Substituting the maximum delay variations (10 ps) and the maximum amount of delay ($\tau(f_0) = 550$ ps) in (2), we find $f_{\varphi=0} \approx 0.06$ GHz at the mid of the frequency band ($f_0 = 1.75$ GHz) which is close to the circuit simulations shown in Fig. 10.

Fig. 20 shows the gain versus frequency variations for all delay and gain settings (without the effect of the LNA/BALUN gain trimming). For all delay settings the gain varies less than ± 1.8 dB at each individual frequency point from 1 GHz to 2.5 GHz band. For each delay setting (a fixed delay) the gain versus frequency variations from 1 GHz to 2.5 GHz remains less than 2.8 dB (or ± 1.4 dB with respect to its average). The gain adjustability in the BALUN provides another opportunity to trim the gain of the individual frequency points with 0.03 dB resolution. The gain variations versus all delay amount settings with the help of BALUN gain trimming is ± 0.03 dB over 1–2.5 GHz band (non-simultaneous). This gain equality resolution results in deep null depths of the beam pattern which will be shown later (Fig. 22). The gain, noise figure and input matching (S_{11}) versus frequency of a single receiver channel set at 255 ps delay is shown in Fig. 21. The 255 ps is the average delay of the four channels when the beam steers towards its maximum angle ($\theta_{\max}$) which results in the maximum noise figure for the timed array (worst case scenario). For other steering angles, the average delay of the channels is less and

TABLE III
BENCHMARKING AND COMPARISON BETWEEN DIFFERENT REPORTED DELAY CELLS

	[21]	[22]	[23]	[9]	[24]	[25]	[26]		[26]		This work
Technology	0.18 µm SiGe	0.13 µm SiGe	0.13 µm SiGe	0.13 µm CMOS	0.8 µm SiGe	0.09 µm CMOS	0.25 µm SiGe		0.25 µm SiGe		0.14 µm CMOS
Supply Voltage(V)	2.5	2.5	2.5	1.5	2.5	N/A	2.7		1.5		1.5
Gain variation(dB)	±1	N/A	N/A	±3	±0.7	±3	±0.9		±1.4		±1.4
Max. delay(ps)	64	16	54	225	25	26	12		12.5		550
Frequency[GHz]	1-15	55-65	31-41	1-15	3-10	0-8	20-40	25-35	20-40	25-35	1-2.5
Delay variation	~16 %	N/A	N/A	~14%	40%	10%	6.4 %	3%	6.6 %	3.2%	1.8%
P_{DC}/channel(mW)	87.5	-	104	78	38.5	-	146		33		90
Resolution(ps)	4	1.2	18	15	Cont.	13	Cont.		Cont.		13
Size(mm^2)	0.82	0.35	1.44	1.5	0.23	N/A	0.1		0.1		0.07
Delay/Size (ps/mm^2)	78	45	37.5	150	109	N/A	120		125		7857

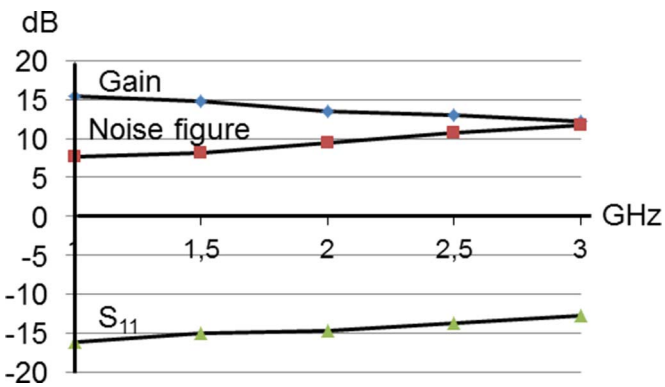

Fig. 21. Gain, input matching and noise figure when delay of the channel is 255 ps.

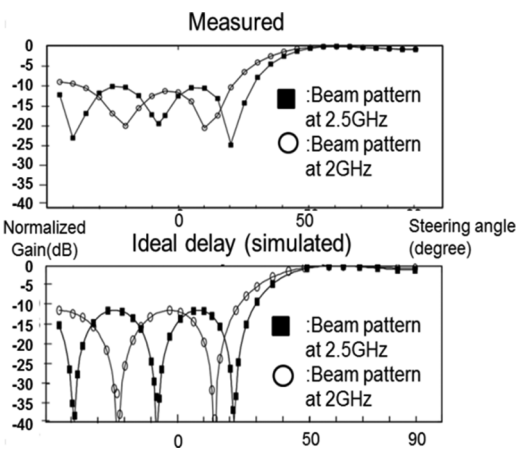

Fig. 22. The measured beam pattern compared to a simulated ideal beam pattern.

therefore the noise figure is better. The measured gain and noise figure is in agreement with the simulations within 0.9 dB.

The measured beam pattern was compared with a simulated ideal time-delay-based beam-forming system as shown in Fig. 22. For the frequency range from 2 to 2.5 GHz, the −3 dB beam width varies from 63° to 51° and the null-to-null distance from 37° to 29°. Also, a new null appears at −38° in the pattern both in measurement and simulation.

The method used for beam pattern measurement is as follows. Four RF signals representing the antenna signals are generated via four external RF generators. Experiments were done at 2 GHz and 2.5 GHz, while an external 3 GHz signal was applied to the LO input. The beam-formed signal is down-converted to 500 MHz to 1 GHz. Going through all delay settings, the beam patterns for 2 GHz and 2.5 GHz are synthesized. Comparing to the simulated beam pattern, it can be seen (Fig. 22) that spatial directions for the beam and nulls in the measured pattern closely follow the ideal pattern. The null depths of the beam pattern were limited to −24 dB which was caused by the cross talk between the off-chip transmission lines of the antenna channels.

Table III [24] compares several reported delay circuits implemented via different technologies and topologies. Compared to other methods, the proposed circuit provides the lowest amount of delay versus frequency variation (1.8% over more than an octave of bandwidth). Also, it is the most compact delay circuit which provides between 1 and 2 orders of magnitude more delay per area. Therefore this circuit is one of the best candidates for low-GHz RF-band applications requiring large amounts of delay. Table IV shows a comparison between our g_m-RC timed-array chip and two other reported time-delay-based chips designed for beam-forming, which exploit LC delay lines and transmission lines. The compactness of the delay cells allows us to implement the chip in a much smaller area at comparable power consumption conditions. The reported noise figure of this circuit is higher, but it is for the worst case scenario (maximum steering angle: $\theta = \pm 60°$). Steering to smaller angles (referred to the bore-sight) requires less delay and produces less noise. The reported amplitude versus frequency variations (± 1.4 dB) are instantaneous for the 1–2.5 GHz frequency band at each delay settings. The gain-trimming property of the LNA plus gain calibration of the delay cells provide 0.03 dB resolution for individual frequencies.

TABLE IV
COMPARISON BETWEEN THIS WORK AND TWO OTHER TIME-DELAY-BASED TIMED-ARRAY SYSTEMS

	This work	Chu, ISSCC 2007 [9]	Van Vliet, GAAS 2003 [8]
Technology	CMOS, 140nm	CMOS, 130nm	PHEMT, 250nm
Technique	Gm-C	LC delay	Transmission line
Features Per Antenna Channel			
Gain	12-15dB (f-dependent)	10dB	6-9dB
Noise Figure	8-10dB	2.9-4.8dB	4.3dB
IIP3	-13 to -20dBm (min to max delay length)	Not mentioned	Not mentioned
-1dB compression point	-21 to -28 dBm (min to max delay length)	Not mentioned	5dBm
Amplitude variation vs. f	±1.4dB	±1dB	±2.5dB
Delay resolution	14psec	15psec	2.5psec
Delay variation vs. f	<10psec	<40psec	<20psec
Maximum delay	550psec	225psec	150psec
Current consumption	50mA	40mA	Not mentioned
Complete 4 channel beamformer			
Beam direction resolution	3.5Bit	3.5Bit	6Bit
Bandwidth	1-2.5GHz	18GHz	3-16GHz
Power consumption	250mA@1.8V	370mA@1.5V	Not mentioned
Die area	1mm^2	10mm^2	10mm^2

VIII. CONCLUSION

This paper has presented a compact all-pass g_m-C cell that was compared to other reported g_m-RC delay cells, showing 5× higher operating frequency range. A chip implementation of the delay cell in 160 nm CMOS results in a flat gain up to 2.5 GHz for the delay cell, with the help of a bandwidth-extension technique. The delay cells are directly cascadable to realize a delay line without AC-coupling or buffering. This avoids parasitic capacitances to ground from DC blocking capacitors which limit frequency range or require extra current consumption. The circuit exploits current re-use with a slow PMOS low-pass path in parallel to a fast NMOS unity gain path to maximize the useful frequency range. Bandwidth and phase linearity are further enhanced by adding carefully dimensioned resistors to the diode-connected transistors. Gain fine control in the delay cells allows for precise gain calibration, independent of delay. Using simulation, a direct comparison of the new delay cell with existing g_m-C and g_m-RC delay cells has been made in terms of frequency range, dynamic range and power consumption. The SNR/P at 1% IM3 of the designed delay cell is 1 dB better than [11] and 6 dB worse than [2], while the frequency range is at least 5× larger (compared to [2] and [11]). To validate performance, a four-antenna beam-forming receiver chip with a maximum steering angle $\theta_{\max}$ of $\pm 60^\circ$ was designed in 160 nm CMOS technology with a total delay per channel of 550 ps in an area of 0.15 mm^2. Compared to other chips with LC delay lines and transmission lines, this is about 2 orders of magnitude more delay per area. The 550 ps delay is digitally controllable in 13 ps steps. Delay variation over a bandwidth from 1 to 2.5 GHz is less than 10 ps, which is only 1.8% of the realized delay. In other words, the selectable delays are monotonous, with low RMS error in the frequency band, and therefore are easy to use in calibration schemes. The delay/size of the circuit, which is 7857 ps/mm^2, is at least 50× more than other delay circuits reported in the literature, which makes it quite suitable for low-GHz operations that need large amounts of delays. An effective delay resolution of 4.7 bits is demonstrated, which corresponds to an effective spatial beam steering resolution of 3.5 bits for full scale steering range of $\pm 60^\circ$, i.e., 10.6° spatial angle resolution. The average noise figure of each antenna channel in the worst case scenario (when the average delay in four channels is maximum, i.e., a beam direction is at $\pm 60^\circ$), is 10 dB.

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Seyed Kasra Garakoui was born in Rasht, Iran, in 1974. He received the B.Sc. degree in electrical engineering from Guilan University, Iran, in 1997, and the M.Sc. degree in analog/RF circuit design from Sharif University of Technology, Tehran, Iran, in 2000. He will defend his Ph.D. thesis in 2015.

Subsequently, he joined NRI (research institute for the electric power industry in Iran) in 2001, where he was working on the design and implementation of radio modems for monitoring the electric power network. In 2007, he joined the Integrated Circuit Design group (ICD) of the University of Twente, The Netherlands, where he worked on RF beam-forming techniques in CMOS technology. In 2011, he joined Axiom-IC in Enschede, The Netherlands (in 2013, this company was acquired by Teledyne Dalsa). He works on mixed-mode circuits with focus on data converters.

Eric A. M. Klumperink (M'98–SM'06) received the B.Sc. degree from HTS, Enschede, The Netherlands, in 1982. After a short period in industry, he joined the University of Twente in 1984, participating in analog CMOS circuit research resulting in several publications and his Ph.D. thesis, "Transconductance Based CMOS Circuits" (1997).

In 1998, he became an Assistant Professor at the IC-Design Laboratory, University of Twente, and his research focus changed to RF CMOS circuits. In April–August 2001, he extended his RF expertise during a sabbatical at the Ruhr Universitaet in Bochum, Germany. Since 2006, he has been an Associate Professor, teaching Analog and RF IC Electronics courses. He participates in the CTIT Research Institute, guiding Ph.D. and M.Sc. projects related to RF CMOS circuit design with focus on software defined radio, cognitive radio, and beam-forming.

Prof. Klumperink was an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II (2006–2007), IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I (2008–2009), and IEEE JOURNAL OF SOLID-STATE CIRCUITS (2011–2013). He is a member of the technical program committees of the IEEE International Solid-State Circuits Conference (ISSCC) and the IEEE RFIC Symposium. He holds several patents, has authored and co-authored more than 150 internationally refereed journal and conference papers, and was a co-recipient of the ISSCC 2002 and ISSCC 2009 Van Vessem Outstanding Paper Award.

Bram Nauta (M'91–SM'03–F'08) was born in 1964 in Hengelo, The Netherlands. In 1987, he received the M.Sc. degree (*cum laude*) in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1987. In 1991, he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies.

In 1991, he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands. In 1998, he returned to the University of Twente, as a full Professor heading the IC Design group. His current research interest is high-speed analog CMOS circuits, software-defined radio, cognitive radio, and beam-forming. In 2014, he was appointed as a Distinguished Professor at the University of Twente.

Prof. Nauta has served as the Editor-in-Chief of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) (2007–2010), and was the 2013 program chair of the IEEE International Solid-State Circuits Conference (ISSCC). He has also served as an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II (1997–1999), and of JSSC (2001–2006). He was on the Technical Program Committee of the Symposium on VLSI Circuits (2009–2013), is on the steering committee and program committee of the European Solid-State Circuits Conference, and is a member of the ISSCC Executive Committee. He has served as a Distinguished Lecturer of the IEEE, and is an elected member of IEEE SSCS AdCom. He was a co-recipient of the ISSCC 2002 and 2009 Van Vessem Outstanding Paper Award, and in 2014 he received the Simon Stevin Meester award, the largest Dutch national prize for achievements in technical sciences.

Frank E. van Vliet (M'96–SM'06) was born in Dubbeldam, The Netherlands, in 1969. He received the M.Sc. degree, with honors, in electrical engineering in 1992 from Delft University of Technology, The Netherlands. He later received the Ph.D. from the same university on MMIC filters.

He joined TNO (Netherlands Organisation for Applied Scientific Research) in 1997, where he is currently a Principal Scientist responsible for MMIC, antenna and transmit/receive module research. In 2007, he was appointed a Professor in microwave integration in the Integrated Circuit Design group at the University of Twente, where he founded the Centre for Array Technology. He also founded the Doctoral School of Microwaves. His research interests include MMICs in all their aspects, advanced measurement techniques and phased-array technology. He has authored and co-authored more than 100 peer-reviewed publications.

Dr. van Vliet is a member of the European Space Agencies Component Technology Board for microwave components, a member of the European Defence Agencies CapTech IAP-01, and chair of the 2012 European Microwave Integrated Circuit Conference (EuMIC 2012). He serves on the TPCs of EuMIC, the IEEE International Symposium on Phased Array Systems and Technology, the IEEE Compound Semiconductor IC Symposium, and the IEEE Conference on Microwaves, Communications, Antennas and Electronic Systems. He was a guest editor of IEEE MTT 2013 Special Issue on Phased-Array Technology.