A thermistor-based temperature sensor for a real-time clock with ±2 ppm frequency stability

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A Thermistor-Based Temperature Sensor for a Real-Time Clock With ±2 ppm Frequency Stability

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***Abstract*—This paper describes the design of a temperature sensor based on integrated poly-silicon thermistors. The thermistors are incorporated in a Wien-bridge *RC* filter, which, in turn, is embedded in a frequency-locked loop. The loop's output frequency is then determined by the filter's temperature-dependent phase shift, thus realizing an energy-efficient and high resolution temperature sensor. After a 3-point calibration, the sensor achieves an inaccuracy of less than ±0.12 °C (min-max) from −40 °C to 85 °C. This translates into a frequency stability of better than ±2 ppm from −40 °C to 85 °C when the sensor is used to temperature compensate the quartz-crystal oscillator of a 32 kHz real-time clock. The 0.09 mm² sensor also achieves 2.8 mK (rms) resolution in a 32 ms conversion time while dissipating only 31 μW.**

***Index Terms*—Real-time clock, TCXO, temperature compensation, temperature sensor, Wien-bridge.**

I. Introduction

INTEGRATING a MEMS or XTAL resonator together with silicon-based sustaining amplifiers and temperature compensation circuitry has become a mainstream approach for the realization of real-time clocks (RTCs), since it results in compact size, low power consumption, and high-frequency stability [1], [2]. The temperature compensation scheme usually consists of a fractional-*N* division or multiplication that scales the output frequency of a MEMS or XTAL oscillator in a temperature-dependent manner [1]–[4]. The temperature sensor used in such schemes must therefore achieve high accuracy and resolution so as not to compromise the frequency stability and jitter of the temperature-compensated output frequency.

Recent publications [1], [3]–[7] have shown that thermistor-based temperature sensors can achieve higher resolution than conventional BJT-based sensors [8]–[10]. In CMOS processes, the required thermistors can be readily realized as integrated polysilicon or diffusion resistors, but the nonlinearity and spread of their temperature dependencies requires time-consuming and, thus, expensive multitemperature calibration. In the context of RTCs, however, this is not a major issue, since such calibration is also required to compensate for the nonlinear temperature dependence of XTAL and MEMS oscillators [1], [3], [4], [6]. Another important feature of thermistor-based temperature sensors is their high energy efficiency, which facilitates the realization of low-power RTCs [1], [3] [4], as in this work. Like other data-converters, the energy efficiency of temperature sensors can be benchmarked with the help of a figure of merit, the resolution FOM, which is the product of their energy/conversion (Joules) and the square of their resolution (°C) [14], [15]. A recent thermistor-based sensor [5], achieves a FOM of 0.5 pJK^2, which exceeds that of recent BJT-based sensors: 13 pJK^2 [8] and 3.6 pJK^2 [10].

Since temperature-stable resistors are not available in standard CMOS processes, another important consideration in the design of a thermistor-based temperature sensor is the choice of a reference. In order not to add extra nonlinearity to the sensor's characteristic, and thus increase the required calibration effort, this should either be temperature stable or have a linear temperature dependence. In [3], the reference consists of a switched-capacitor network based on metal-insulator-metal capacitors, whose effective resistance is thus nearly temperature independent. A feedback loop dynamically balances the resistances of the thermistor and the switched-capacitor network by adjusting the latter's switching frequency with the help of a sigma-delta ($\Sigma\Delta$) modulator, a 480 MHz reference frequency and a fractional-*N* divider. Due to the nonlinearity of the chosen thermistor, the resulting RTC requires a 6-point calibration to achieve ±0.5 ppm frequency stability from −40 °C to 85 °C. In [1] and [4], a temperature-dependent current derived from an n-well thermistor controls the frequency of a ring oscillator, which is then digitized with respect to a reference clock. Due to the nonlinear temperature dependence of the thermistor and the ring oscillator, the resulting RTC requires a 5-point calibration to achieve ±10 ppm frequency stability from −40 °C to 85 °C. In [5], instead of using a reference clock, the resistance of two different polysilicon thermistors (with opposite temperature dependencies) is compared with the help of a continuous-time sigma-delta modulator (CTDSM). Despite the use of an on-chip lookup table (LUT) to compensate for the systematic nonlinearity in the temperature dependence of the two thermistors, process tolerances mean that the sensor's characteristic is still quite nonlinear: it achieves an inaccuracy of ±0.4 °C from 0 to 100 ° C after a 2-point trim.

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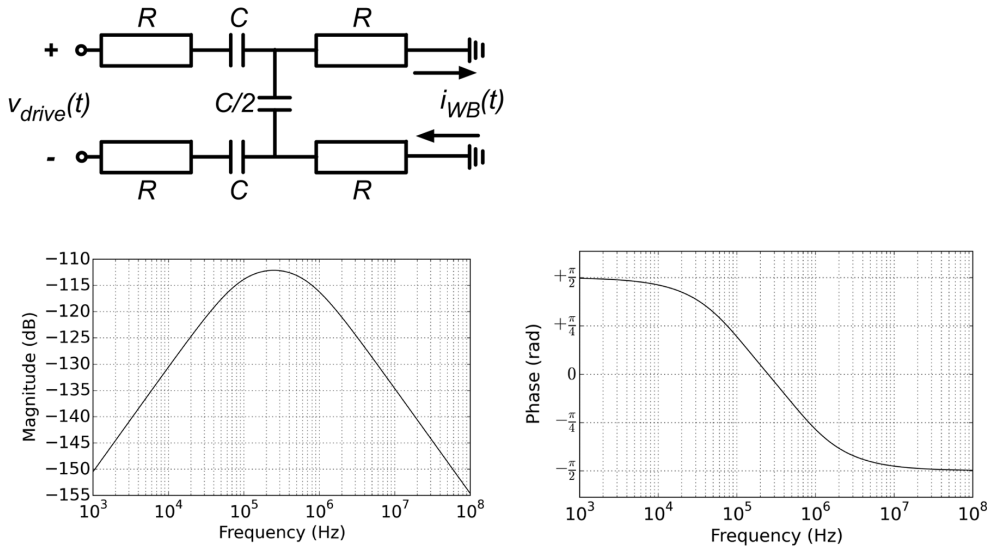

Fig. 1. Schematic and Bode plot of the WB (R = 135 kΩ and C = 4.7 pF).

An alternative time-based approach involves incorporating thermistors into an *RC* Wien-bridge (WB) filter, which is then driven by a reference frequency [6]. The filter's phase shift will then be mainly determined by the thermistors, since on-chip metal–insulator–metal are comparatively stable. In [6], this filter's phase-shift was digitized by a phase-domain sigma-delta modulator, using phase references derived from a reference frequency. By exploiting the relatively linear temperature dependence of polysilicon thermistors, the sensor only requires a 3-point calibration to achieve an inaccuracy of ±0.15 °C (3σ) from −40 °C to 85 °C. In order to generate the modulator's phase references, however, the reference clock frequency (4 MHz) was significantly higher than the filter's drive frequency (250 kHz). As a result, this approach is not well suited for use in low-power RTCs.

In this work, this drawback is overcome by embedding a WB sensor in a frequency-locked loop (FLL) [7], whose output frequency can then be readily digitized with the help of the RTC's 32 kHz output. The resulting sensor achieves ± 0.12 °C inaccuracy (min-max) from −40 °C to 85 °C after a 3-point calibration. Over the same range, and using data collected at the same calibration points, the resulting RTC achieves a frequency stability of ±2 ppm.

The remainder of this paper is organized as follows. In Section II, the characteristics of the WB sensor are briefly explained and the performance of the FLL-based readout methodology is investigated. In Section III, the circuit design is discussed and the measurement results are shown in Section IV. The paper concludes in Section V.

II. Wien-Bridge (WB)-Based Temperature Sensor

A. WB Filter and its FLL-Based Readout

The schematic of a WB filter is shown in Fig. 1 together with its Bode plot. The relationship between the input voltage $v_{\mathrm{drive}}(t)$ and output current $i_{\mathrm{WB}}(t)$ is given by

$$\frac{I_{\mathrm{WB}}(s)}{V_{\mathrm{drive}}(s)} = \frac{C \cdot s}{R^2C^2s^2 + 3RCs + 1} \tag{1}$$

and the phase shift of the WB $\phi_{\mathrm{WB}}(\omega)$ can be expressed as follows:

$$\phi_{\mathrm{WB}} = \tan^{-1}\frac{1 - R^2C^2\omega^2}{3RC\omega}. \tag{2}$$

The transfer function $I_{\mathrm{WB}}(\mathrm{s})/V_{\mathrm{drive}}(\mathrm{s})$ has a bandpass characteristic whose phase shift varies from $\pi/2$ to $-\pi/2$ and which is zero at the filter's center frequency $\omega_0 = 1/RC$. Around this frequency, $\phi_{\mathrm{WB}}(\omega)$ is quite linear and so may be regarded as an error signal that indicates the difference between f_0 and the frequency of $v_{\mathrm{drive}}(t)$. This insight motivates the use of a WB in a frequency-locked loop (FLL) which attempts to drive this error signal to zero by tuning a voltage-controlled oscillator, whose output frequency will then be locked to a (multiple of) $\omega_0 = 1/RC$ [11].

A simplified block diagram of the FLL is shown in Fig. 2. The output of a voltage-controlled oscillator (VCO) is divided by N and used to generate in-phase and quadrature-phase signals. The in-phase signals drive the WB, generating a filtered and phase-shifted output current that is demodulated by the quadrature-phase signals. The resulting dc output current $i_{\mathrm{DC}}(t)$is (approximately) proportional to the cosine of $\phi_{\mathrm{WB}}(\omega)$. This current is then integrated on capacitor, C_{int}, and the resulting voltage is used to adjust the VCO's output frequency f_{VCO}. At steady state, the phase shift of the WB will be zero, which means that $f_{\mathrm{VCO}} = N \cdot f_0$.

B. Resolution of the FLL-Based Readout Circuit

The temperature-sensing resolution of the FLL-based readout circuit will be limited by the thermal noise of the thermistors in the WB and the input-referred current noise of the current buffer. In order to estimate their effects, a small-signal model of the FLL will be derived. Since the WB is a bandpass filter, useful insights can be obtained by considering only the first harmonic of the square-wave drive signal, which simplifies the analysis

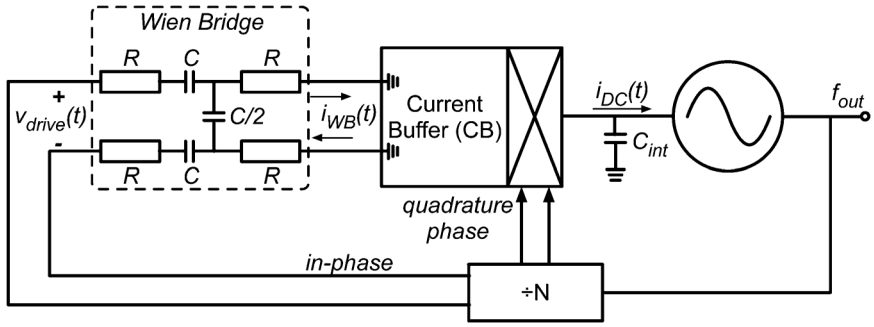

Fig. 2. FLL-based readout method for the WB-based temperature sensor.

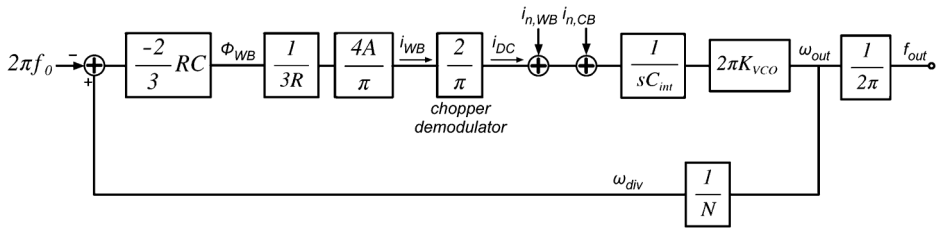

Fig. 3. Small-signal model of the WB-based temperature sensor with FLL-based readout method at steady-state ($\omega_{\rm out} \sim 1/{\rm RC}$).

considerably. The first harmonic of the drive signal can be expressed as follows:

$$v_{\rm drive}(t) = \frac{4}{\pi} A \sin(\omega_{\rm drive} t). \tag{3}$$

Noting that, at $\omega = 1/RC$, the magnitude of the transfer function in (1) is $1/3R$, the output current of the WB, $i_{\rm WB}(t)$, can then be approximated as

$$i_{\rm WB}(t) \approx \frac{4}{\pi}\frac{A}{3R}\sin(\omega_{\rm drive} t + \phi_{\rm WB}) \tag{4}$$

where A is the amplitude of the drive signal and R is the temperature-dependent resistance of the thermistors used in the WB. The current $i_{\rm WB}(t)$ is then demodulated (chopped) by the quadrature signal resulting in components at even harmonics of $\omega_{\rm drive}$ and a dc component $i_{\rm DC}(t)$ as

$$\begin{aligned} i_{\rm DC}(t) &= \frac{4}{\pi}\frac{A}{3R}\sin(\omega_{\rm drive} t + \phi_{\rm WB}) \\ &\quad \cdot \frac{4}{\pi}\sin\left(\omega_{\rm drive} t + \frac{\pi}{2}\right) @{\rm DC} \\ &= \frac{16}{\pi^2}\frac{A}{6R}\cos\left(\phi_{\rm WB} - \frac{\pi}{2}\right) \approx \frac{16}{\pi^2}\frac{A}{6R}\phi_{\rm WB}. \end{aligned} \tag{5}$$

At steady state, the sensitivity of the FLL's error signal $\phi_{\rm WB}$to small variations in ω can then be determined by evaluating $d\phi_{\rm WB}/d\omega$ from (2) at $\omega_0 = 1/RC$ as follows:

$$\frac{d\phi_{\rm WB}}{d\omega} = -\frac{2}{3}RC \tag{6}$$

The resulting linear model of the proposed temperature sensor is shown in Fig. 3. $K_{\rm VCO}$ (Hz/V) and N are the gains of the VCO and the division ratio of the feedback divider, respectively. The current noise of the WB and CB is modeled by current sources at the output of the chopper demodulator, since the contribution of down-converted noise at the odd harmonics of the square-wave chopping signal only results in a small increase (∼10%) in the total output noise near dc [12].

The power spectral density (PSD) of the output current noise of the WB, $i_{n,{\rm wb}}$, can be estimated by adding the contribution of each resistor's noise at $\omega \sim 1/RC$. The resulting PSD is given by

$$S_{in,WB} = \frac{8kT}{3R}\cdot\frac{1}{2} = \frac{4kT}{3R} \tag{7}$$

where k is the Boltzmann constant and T is the absolute temperature. This noise current will cause fluctuations $\Delta f_{\rm out}$ in the FLL's output frequency. The noise transfer function (NTF) from $i_{n,{\rm wb}}$ to $f_{\rm out}$ can be derived from Fig. 3 as follows (assuming that the loop gain ≫1 near dc):

$$\frac{F_{\rm OUT}(s)}{I_{n,wb}(s)} = \frac{\frac{1}{sC_{\rm int}}\cdot 2\pi K_{\rm VCO}}{1 + \frac{2C}{9N}\cdot\frac{8A}{\pi^2}\cdot\frac{1}{sC_{int}}\cdot 2\pi K_{\rm VCO}}\cdot\frac{1}{2\pi} \approx \frac{9\pi N}{32AC}. \tag{8}$$

By combining this with (7), the PSD of the FLL's output frequency's deviation $S_{f\rm out}$can be calculated as

$$S_{f\rm out}(f) = S_{\rm in,wb}(f)\cdot\left|\frac{F_{\rm OUT}(f)}{I_{n,\rm wb}(f)}\right|^2 = \frac{4kT}{3R}\cdot\left|\frac{9\pi N}{32AC}\right|^2. \tag{9}$$

The output frequency of the FLL is digitized by an on-chip counter, which counts the number of VCO clock edges that arrive during the conversion time $T_{\rm conv}$. As shown in Fig. 4, after scaling by $T_{\rm conv}$, the final counter output is a digital representation of the output frequency $\widehat{f}_{\rm out}$. This process is equivalent to filtering $\Delta f_{\rm out}$ with a sinc^1 filter of length $T_{\rm conv}$ and a noise bandwidth of $1/2T_{\rm conv}$. As a result, the rms variation in $\widehat{f}_{\rm out}$ is given by

$$\Delta\hat{f}_{\rm out}({\rm rms}) \approx \sqrt{S_{f\rm out}(f)\cdot\frac{1}{2\cdot T_{\rm conv}}}. \tag{10}$$

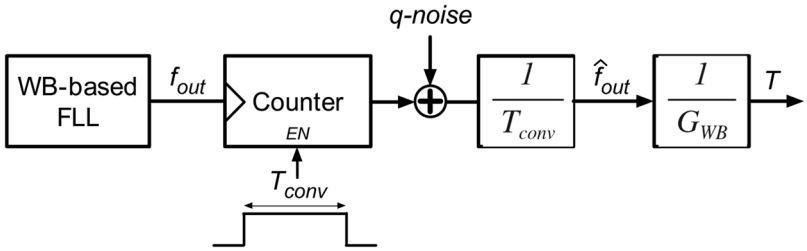

Fig. 4. Block diagram showing how the FLL's output frequency, $f_{\rm out}$ is digitized.

The sensor's resolution ΔTcan then be obtained by dividing $\Delta\widehat{f}_{\rm out}$(rms) by its sensitivity $G_{\rm WB}$. The latter is simply the derivative of the output frequency $f_{\rm out} = N/(2\pi RC)$ with respect to the absolute temperature T. Assuming that $R = R_0(1+\alpha(T - T0))$, the sensitivity $G_{\rm WB}$is

$$G_{\rm WB} = \frac{df}{dT} = \frac{df}{dR}\cdot\frac{dR}{dT} = \frac{-N}{2\pi R_0^2 C}\cdot\alpha R_0 = \frac{-\alpha N}{2\pi R_0 C}. \quad (11)$$

From (7)–(11), the resolution ΔT at temperature T_0, can now be calculated as follows:

$$\Delta T = \frac{\Delta\hat{f}_{\rm out}}{G_{\rm WB}} = \sqrt{\frac{2kT_0}{3}\frac{1}{T_{conv}}}\cdot\frac{\sqrt{R_0}}{(-\alpha)}\cdot\frac{9\pi^2}{16A}. \quad (12)$$

In the actual design, the WB is implemented with $R_0 = 135$ kΩ, $C = 4.7$ pF and $A = 1.8$ V. For various $T_{\rm conv}$, the estimated temperature resolution at $T_0 \sim 300$ K is plotted in Fig. 5. For $T_{\rm conv} = 32$ ms, the resolution is ~ 221.5 μK (rms), and drops to ~ 122.5 μK (rms) for $T_{\rm conv} = 125$ ms, showing that with a noiseless readout circuit the sensor should be able to achieve sub-mK resolution.

In practice, the current buffer's input-referred noise current $i_{n,CB}$ will be non-negligible. However, it will be filtered by the same NTF as the WB filter's noise $i_{n,WB}$, and so its effect on the sensor's resolution can be obtained by following a similar procedure. In the actual implementation, the buffer is also chopped, and so its main contribution is thermal noise. In this design, simulations show that $i_{n,CB} = 0.9$ pA$/\sqrt{Hz}$. As shown in Fig. 5, the current buffer's noise degrades the sensor's resolution to $\sim$1 mK (rms) and ~ 513 μK (rms) for $T_{\rm conv} = 32$ ms and $T_{\rm conv} = 125$ ms, respectively.

Using an on-chip counter to digitize the FLL's output frequency adds quantization noise and thus limits the achievable temperature resolution. Assuming that the output of the counter is M, then $\widehat{f}_{\rm out}$ is

$$\hat{f}_{\rm out} = \frac{M}{T_{\rm conv}} + \frac{q}{T_{\rm conv}} \quad (13)$$

where q is the quantization noise added during digitization whose variance, $\sigma_q^2$is 2/12, since quantization noise is added both at the beginning and at the end of the measurement. By taking into account both CB noise and the quantization noise, the rms deviation in $\widehat{f}_{\rm out}$ can be represented as follows:

$$\Delta\hat{f}_{\rm out} \approx \sqrt{S_{f\rm out}(f)\cdot\frac{1}{2\cdot T_{\rm conv}} + \frac{\sigma_q^2}{(T_{\rm conv})^2}} \quad (14)$$

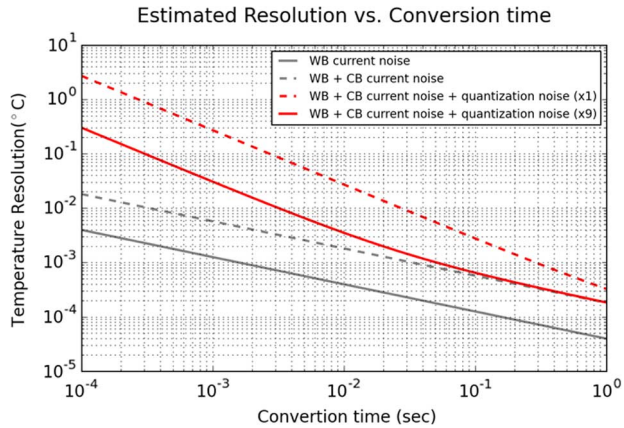

Fig. 5. Estimated temperature resolution of the WB-based temperature sensor with FLL-based readout method.

The temperature resolution is derived by dividing (14) by the $G_{\rm WB}$ and is also plotted in Fig. 5. The contribution of the quantization noise is inversely proportional to $T_{\rm conv}$, and degrades the temperature resolution for $T_{\rm conv} = 32$ ms from 1 mK (rms) to 8.5 mK (rms). This can be mitigated by multiplying the FLL's output frequency before it is digitized. Since the actual VCO is based on a 9-stage ring-oscillator, a multiplication by $K = 9$ can be readily obtained with an edge-combining circuit [1]. The scaled output frequency, $\widehat{fh}_{\rm out}$ can then be written as

$$\hat{fh}_{\rm out} = \frac{M'}{T_{\rm conv}} + \frac{q}{T_{\rm conv}} \quad (15)$$

where M' is the output of the counter with scaled output frequency. Then, the rms frequency deviation of the scaled output frequency is

$$\Delta\hat{fh}_{\rm out} \approx \sqrt{S_{f\rm out}(f)\cdot\frac{K^2}{2\cdot T_{\rm conv}} + \frac{\sigma_q^2}{(T_{\rm conv})^2}}. \quad (16)$$

The sensor's resolution can then be obtained by dividing (16) by $K \times G_{\rm WB}$, in order words, the quantization noise is attenuated by a factor of K. The improved resolution with $K = 9$ is also plotted in Fig. 5. For $T_{conv} > 30$ ms, the contribution of quantization noise becomes less than that of thermal noise, and a resolution of $\sim$1.4 mK (rms)can be achieved in a 32 ms conversion time.

In practice, there will be other sources of noise, e.g. the jitter of the reference clock, the phase noise of the VCO, the noise present in the power supplies from which the driving square-wave is derived, and last, but certainly not least, fluctuations in

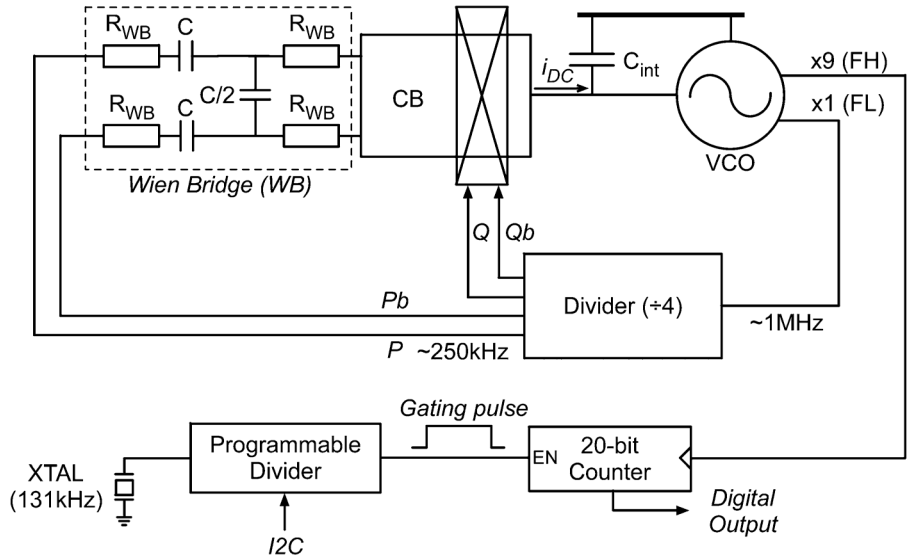

Fig. 6. Overall block diagram of the proposed temperature sensor.

ambient temperature. Like the quantization noise added during digitization, the jitter of the reference clock will be mitigated by increasing $T_{\rm conv}$. The VCO's phase noise is injected after the FLL's integrator, and so it will be effectively high-pass filtered by the loop. In the actual implementation, the loop bandwidth is designed to be ~5 kHz so that the effect of VCO noise should be well suppressed for conversion times of a few tens of milliseconds. Due to the band-pass characteristic of the WB itself and the use of a synchronous phase detector, the sensor is only sensitive to power supply noise in a narrow band around f_0. This is further suppressed by the use of on-chip decoupling capacitors and an on-chip LDO.

III. Architecture and Circuit Implementation

The overall architecture of the proposed temperature sensor is shown in Fig. 6. The WB is driven by complementary square-waves, P and Pb, at a frequency, $f_{\rm drv} \sim 250$ kHz, which are derived from the VCO's output (FL) by a divide-by-4 circuit. The divider also generates the quadrature signals Q and Qb that drive the chopper demodulator, used here as a synchronous phase detector. The output frequency is digitized by a 20-bit on-chip counter, which is gated by a reference pulse derived from the RTC's 131 kHz quartz-crystal oscillator. The counter is driven by a 9× scaled output frequency (FH) to reduce the quantization noise. The conversion time is an integer number of periods of the 131 kHz oscillator and can be programmed from 0.5 ms to 1 s via an I2C interface. The loop bandwidth of the FLL is designed to be 5 kHz to reduce the phase noise of VCO. This ensures that the effect of VCO's noise is negligible when the conversion time is longer than few tens of milliseconds. The WB consists of poly-silicon resistors and fringe capacitors with nominal values of 135 kΩ and 4.7 pF respectively. Despite their lower temperature coefficient, polysilicon (0.15%/°C) rather than nwell (0.3%/°C) resistors were used, because their more linear temperature dependence requires less calibration. To reduce substrate-noise coupling, a grounded n-well shield was placed under the WB.

A. Current Buffer (CB)

The detailed schematic of the current buffer (CB) is shown in Fig. 7. The WB's output current is injected into the CB, where it is demodulated by a chopper, CH1 and then integrated on C_{int} (80 pF). CH1 also up-modulates the $1/f$ noise of PMOS current sources, which were degenerated to reduce their $1/f$ noise corner, thus mitigating this source of noise. Similarly, another chopper at NMOS side, CH2, mitigates the $1/f$ noise contribution of the NMOS current sources. Cascode transistors $\rm M_{3-6}$ are gain boosted to ensure that the CB's input impedance at f_0 is much less than that of $R_{\rm WB}$, and that the FLL's loop gain is large enough to suppress the VCO's own drift and phase noise. As a result, the FLL's resolution is mainly limited by the thermal noise of $R_{\rm WB}$ and the current sources. The use of gain boosting also minimizes the error current associated with the switching action of CH1 and CH2 and the parasitic drain capacitances of M1,2 and M7,8 [13]. The bias current of each branch of the CB is about 3 μA, which is designed to be larger than the output current from the WB to ensure the linear operation. The simulated current noise of the CB ranges from 0.7 pA/$\sqrt{Hz}$ to 1.25 pA/$\sqrt{Hz}$ over PVT variations. The current noise is mainly determined by the resistor of degenerated current source whose maximum value is also limited by the required voltage headroom. The FLL is powered by an on-chip LDO, while its bias currents are derived from a constant-g_m bias circuit with a nominal value of 1 μA. In combination with the gain boosters' tail and load resistors, this approach ensures that the various node voltages are well defined over temperature and process.

B. Voltage-Controlled Oscillator (VCO)

The schematic of the VCO is shown in Fig. 8. MVCO converts the CB's output into a current that drives a 9-stage current-controlled oscillator (CCO) with a nominal output frequency of 1 MHz. To ensure that the FLL starts up properly, a pulse-generator drives an initial current $i_{\rm initial}$ into the CCO via the switch Mi. The relatively small switch is then turned off, so that it's $1/f$ noise does not degrade the CCO's phase noise. The size of

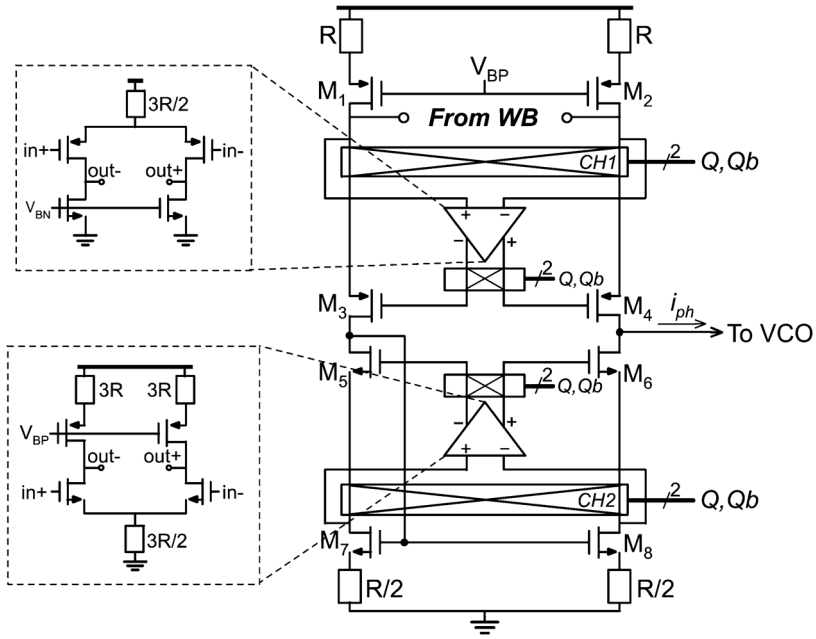

Fig. 7. Schematic of the CB.

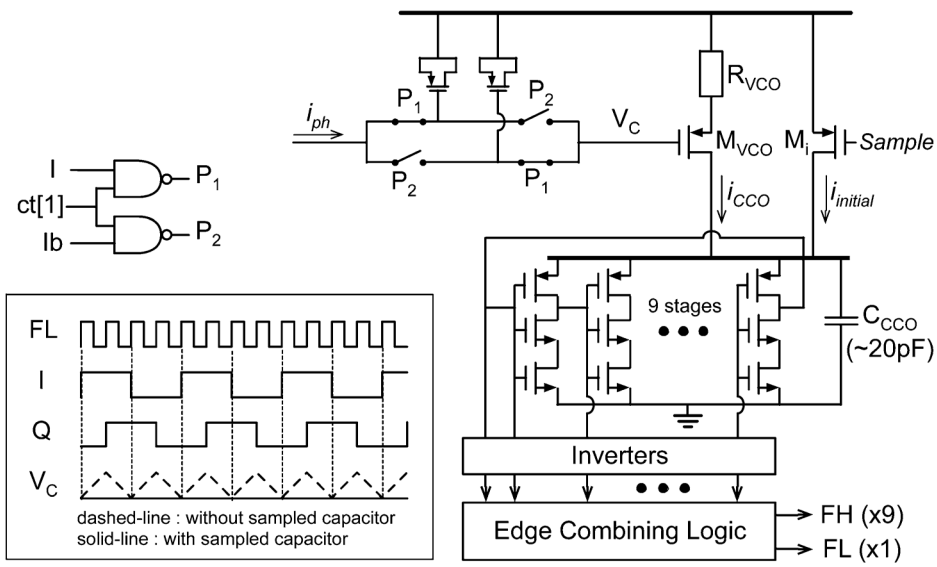

Fig. 8. Schematic of the VCO with SC integrator.

MVCO is carefully chosen so that its $1/f$ noise does not dominate the CCO's phase noise. A decoupling capacitor CCCO (20 pF) is used to stabilize the voltage swing across the CCO. The associated pole (150 kHz) is high enough not to cause stability problems. For increased resolution, an edge-combining circuit generates a 9 MHz output (FH) from the CCO's output, which is then decimated by a 20-bit counter. The edge-combining circuit consists of several NAND gates as shown in Fig. 9. The NAND gate generates narrow pulses from two consecutive outputs of the CCO and then the pulses are combined generating higher output frequency.

Besides the dc component $i_{\rm DC}$, chopping the WB's output current also results in a second-harmonic component. After integration on $C_{\rm int}$, the resulting ripple on VC reduces the CB's effective output range and causes a resolution-limiting spur in FL. Although this ripple can be minimized by increasing $C_{\rm int}$, this is not area-efficient. As shown in Fig. 8, the ripple can be more effectively suppressed by a switched capacitor (SC) notch filter, which samples the ripple at $2f_{\rm drv}$. It should be noted that $C_{\rm int}$ is realized by PMOS capacitors that are referenced to the supply voltage, thus making the output of the voltage-to-current converter MVCO insensitive to supply-voltage variations.

IV. Measurement Results

A prototype RTC, consisting of a 131 kHz oscillator, an on-chip state machine, a fractional-N divider, the temperature sensor and an I2C interface, was implemented in a standard 0.18 μm CMOS technology. The prototype chip was mounted together with a miniature 131 kHz crystal in a 44-pin QFP ceramic package [1]. The temperature sensor occupies 0.09 mm^2

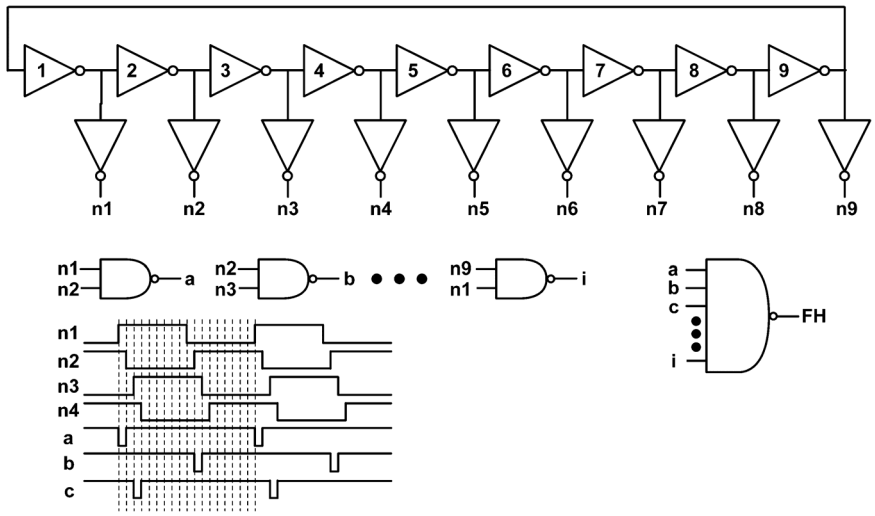

Fig. 9. Schematic of the edge-combining circuit that generates ×9 higher output frequency.

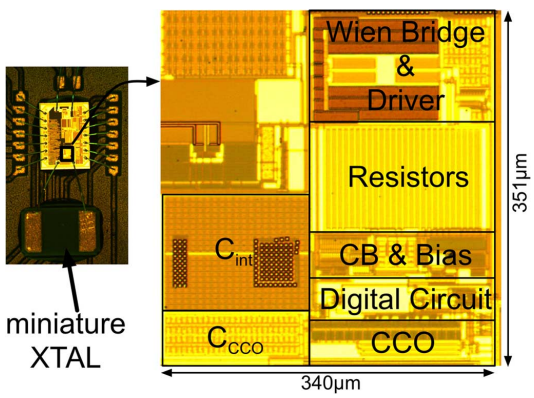

Fig. 10. Micrographs of the packaged chip and the temperature sensor.

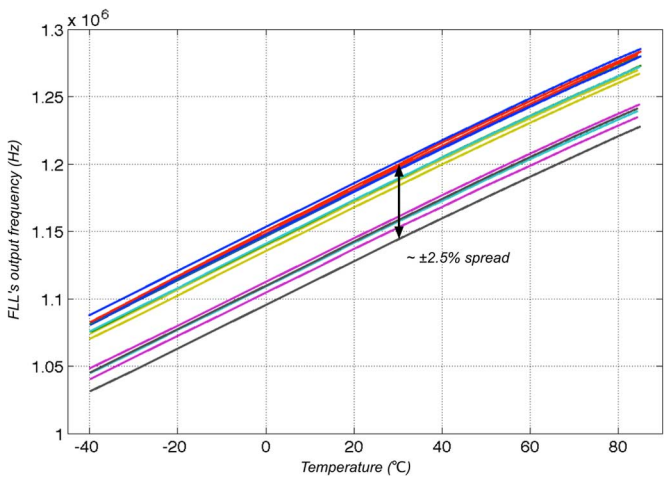

Fig. 11. Measured output frequency of FLL over temperature.

of the 1.92 mm^2 chip (Fig. 10). The chip is powered from a 3.3 V supply, from which the FLL draws 17.5 μA via a 1.7 V LDO, while the decimating counter draws 1.3 μA from a 1 V LDO. 17% of the FLL's power consumption is used to drive the WB, 60% is used for the CB, and 16% is used for the CCO.

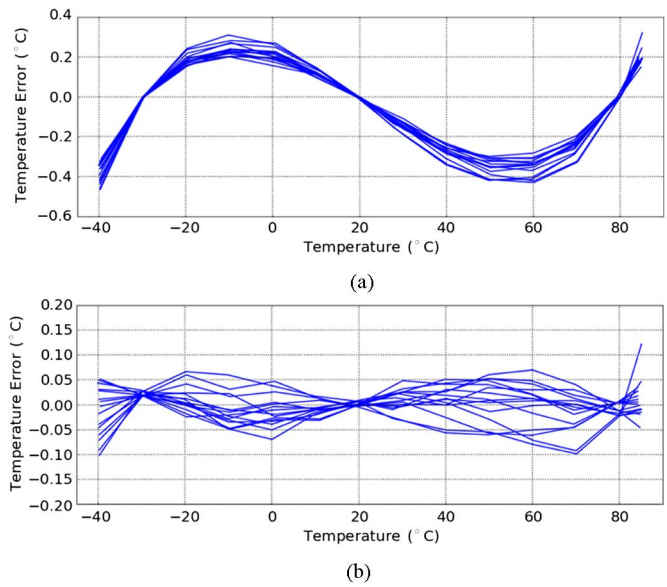

Fig. 12. Measured temperature error (a) after 3-point trim and (b) after removal of systematic error.

Fifteen devices were characterized in a temperature-controlled oven from −40 °C to 85 °C. As shown in Fig. 11, the FLL's output frequency (FL) changes from 1.03 MHz to 1.29 MHz over the temperature range from −40 °C to 85 °C. At room temperature, it exhibits ±2.5% spread around 1.18 MHz, and temperature sensitivity about 1600 Hz/°C. After a 3-point calibration, each sensor's characteristic was fitted to a second-order master curve. As shown in Fig. 12, the residual spread is then less than ±0.12°C (min-max). The remaining error is systematic and can thus be removed by a fixed third-order polynomial [Fig. 12(b)]. By varying the output voltage of the on-chip LDO, the FLL's voltage sensitivity was found to be about −0.4 °C/V.

The phase noise of FLL's output (FH) is plotted in Fig. 13 together with the estimated noise contributions of the VCO and the CB. The noise of the VCO and the CB are high-pass and low-pass filtered, respectively, by the FLL, as may be inferred from

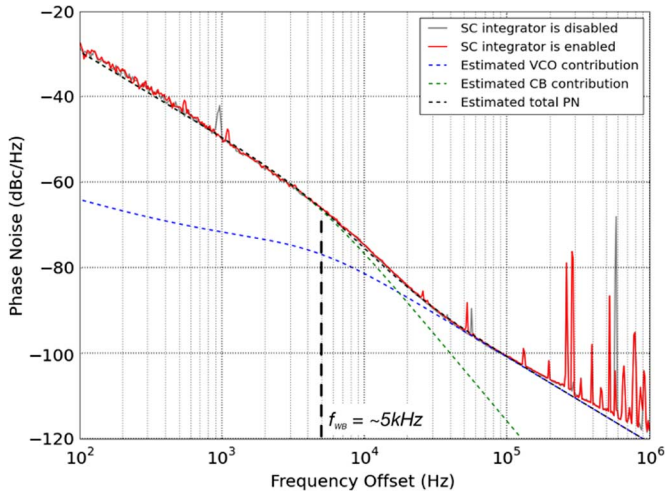

Fig. 13. Measured phase noise of the FLL's output (FH) with and without enabling SC integrator.

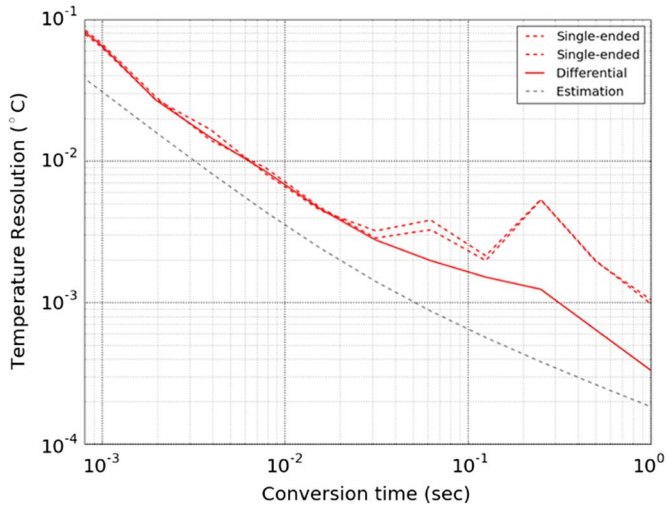

Fig. 14. Temperature resolution of the proposed sensor for various conversion times.

the fact that the slope of the resulting noise spectrum changes around the loop bandwidth, ~5 kHz. The spot phase noise at 1 kHz is about −50 dBc/Hz and corresponds to a CB current noise of ~ 0.9 pA/$\sqrt{Hz}$. From Fig. 13, it can be seen that the spurs at ~600 kHz are reduced by ~40 dB when the SC integrator is enabled. The sensor's resolution versus conversion time is shown in Fig. 14. It was obtained by logging the results of 5000 consecutive conversions at 30 °C. For short conversion times, the sensor's resolution is determined by the quantization error associated with the gated counter and so it decreases linearly with conversion time. After about 30 ms, the sensor's resolution begins to be dominated by thermal noise and so it decreases approximately with the square root of conversion time.

In order to accurately measure the sensor's resolution, especially for long conversion times, any ambient temperature drift should be removed. Since the ambient temperature drift behaves like a common mode signal, it is suppressed by taking the difference in the outputs of two temperature sensors mounted on the same heat-sink (a large aluminium block) and then scaling

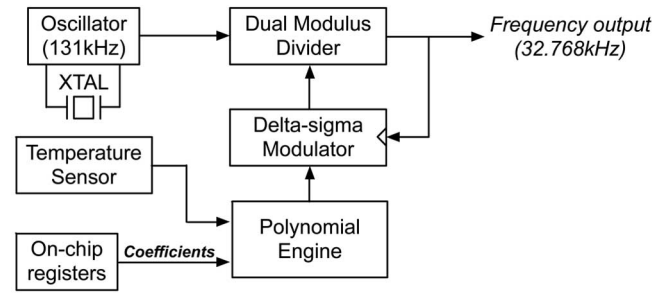

Fig. 15. Block diagram of the RTC and its temperature compensation scheme.

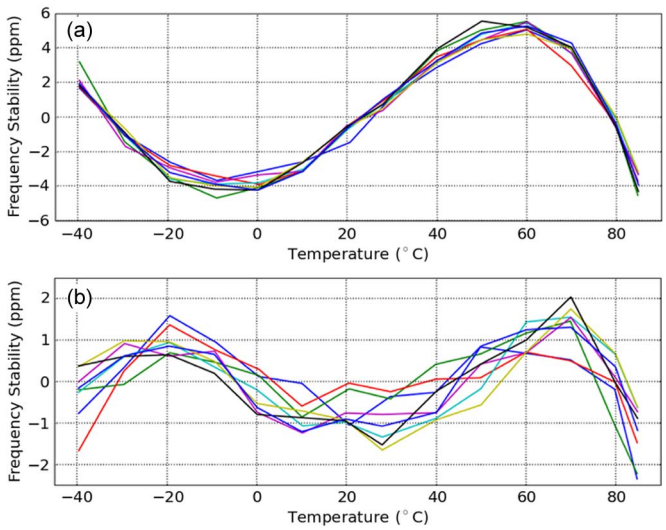

Fig. 16. Measured frequency stability of the temperature compensated 32 kHz output (a) after 3-point trim and (b) after removal of systematic error.

them by a factor of $\sqrt{2}$. In Fig. 14, the results of different measurement methods are plotted. The results shown in red dashed line are obtained from a single temperature sensor and show that the resolution is limited by oven drift for long conversion times. The result shown in red solid line is obtained from differential measurement and clearly shows that for longer conversion times, the sensor's resolution is significantly less than oven drift. The estimated resolution with a CB current noise density of 0.9 pA/$\sqrt{Hz}$ is also plotted with a gray dashed line that shows good agreement with the measurement results. In a 32 ms conversion time, the sensor achieves a resolution of 2.8 mK (rms), which drops to 1.5 mK (rms) for a 125 ms conversion time. As in [1], [4], the sensor can thus be duty-cycled to significantly reduce its average power dissipation.

In Table I, the temperature sensor's performance is compared with that of other high-resolution sensors. Despite the use of low-sensitivity poly-silicon resistors, instead of say n-well resistors, it is quite energy efficient, achieving a state-of-the-art resolution FOM of 8 pJK^2.

The parabolic temperature dependence of the 131 kHz quartz-crystal was also characterized and was found to vary by 200 ppm from −40°C to 85 °C with a maximum slope of ~ 6 ppm/°C. To compensate for this, an on-chip second-order $\Sigma\Delta$ fractional divider is used to generate a stable 32.768 kHz output (averaged over 32 s) as shown in Fig. 15 [1]. The division ratio is

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS THERMISTOR-BASED TEMPERATURE SENSORS

	This work	JSSC13 [3]	JSSC10 [4]	ESSCIRC13 [6]	
Sensor Type	**Poly Res.**	Resistor	N-well Res.	Poly Res.	N-well Res.
Chip Area	**0.09mm^2**	0.18mm^2	0.044mm^2	0.35mm^2	
Power consumption	**31µW**	13mW	30µW	36µW	
Temperature Range	**-40°C ~85°C**	-40°C ~85°C	0°C ~100°C	-40°C ~85°C	
Inaccuracy (Trim. method)	**±0.12°C†† (3-point)**	±0.015°C†† (5th order)	±0.33°C†† (3-point)	±0.15°C† (3-point)	±0.25°C† (3-point)
Resolution (T_{conv})	**2.8mK (32ms)**	0.1mK (100ms)	40mK (7.5ms)	6mK (100ms)	3mK (100ms)
Res. FOM	**8pJK^2**	13pJK^2	360pJK^2	130pJK^2	32pJK^2

Res. FOM = Energy/Conversion × (Resolution)^2 [15]
† : 3σ, †† : min./max.

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUS RTC SYSTEMS

	This work	JSSC14 [1]		JSSC15 [2]	JSSC13 [3]	JSSC10 [4]	MAXIM†
Technology	**0.18µm**	0.18µm		0.18µm	0.18µm	0.18µm	-
Type of Resonator	**XTAL**	XTAL	XTAL	MEMS	MEMS	Silicon resonator	MEMS
Temperature Range	**-40°C ~85°C**	-40°C ~85°C	0°C ~50°C	-40°C ~85°C	-40°C ~85°C	0°C ~50°C	-45°C ~85°C
Frequency Stability (Trim. method)	**±2ppm (3-point)**	4.5ppm (5-point)	1ppm (5-point)	±3ppm	±0.2ppm (12-point)	±10ppm (3-point)	±5ppm (-)

†: http://datasheets.maximintegrated.com/en/ds/DS3231M.pdf

a 3rd order polynomial function of temperature, whose coefficients were written to on-chip registers via the I2C interface. For each chip, the coefficients were determined by combining the fixed second-order temperature dependence of the oscillators with the individual sensor's second-order master curve. As shown in Fig. 16, this approach results in an RTC with a frequency stability of ±2 ppm from −40°C to 85°C.

In Table II, the performance of the RTC is compared with the state of the art. With the proposed WB-based temperature sensor, the RTC achieves ±2 ppm frequency stability with the minimum number of trimming points. Compared to [1], [4], the sensor enables the realization of an RTC with similar frequency stability, but with a wider temperature range and significantly less calibration effort.

V. CONCLUSION

A thermistor-based temperature sensor has been realized together with a low-power quartz-crystal-based 32 kHz RTC in a 0.18 μm CMOS technology. The sensor consists of a WB bandpass filter made up of polysilicon thermistors and stable fringe capacitors. The WB is embedded into a FLL, which locks the frequency of a ring oscillator to the temperature-dependent center frequency of the WB. The FLL's output is then digitized by a counter that is gated by the RTC's output frequency. A linear model of the proposed temperature sensor shows that its temperature resolution is mainly limited by the thermal noise of the readout circuitry. Chopping mitigates the effect of $1/f$ noise, while an edge-combining circuit uses the ring oscillator's phases to multiply the FLL's output frequency by 9× and so mitigate the effect of quantization noise. The prototype chip achieves a temperature resolution of 2.8 and 1.5 mK at 32 and 125 ms conversion time, respectively resulting in a resolution FOM of 8 pJK^2. The measured inaccuracy is ±0.12 °C (min-max) from −40 °C to 85 °C after a 3-point calibration. When used to stabilize a quartz-crystal oscillator, the result is a real-time clock with a frequency stability of less than ±2 ppm after a 3-point calibration, which compares favorably with the state of the art.

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