Introduction to the Special Issue on the IEEE 2014 Custom Integrated Circuits Conference

THIS Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is comprised of 17 papers selected from the 2014 IEEE Custom Integrated Circuits Conference (CICC). The issue spans contributions in analog/mixed signal techniques, data converters, power management, frequency synthesis, wireless/wireline communications, and memory. The selected papers advance the state-of-the-art in terms of power, area, performance, integration, and/or by demonstrating innovative circuit implementations and techniques.

The special issue begins with a paper by J. Charthad *et al.* that presents a proof-of-concept mm-sized implantable device using ultrasonic power transfer and a hybrid bi-directional wireless data communication link. The prototype measures 4 mm $\times$ 7.8 mm, and the 65 nm IC included within the device can support a maximum DC load of 100 μW for an incident acoustic intensity that is $\sim$5% of the FDA diagnostic limit. The next paper, by S. Jeong *et al.*, reports a CMOS wake-up timer designed for compact wireless sensors. The design utilizes a constant charge subtraction scheme to enable the use of a coarse clocked comparator (as opposed to a low-delay and hence potentially power-hungry continuous time comparator). The 0.18 μm prototype dissipates 5.8 nW while maintaining a temperature stability of 45 ppm/°C and line sensitivity of 1%/V. The third paper, by M. Kinyua *et al.*, shows a 55 nm class-D audio amplifier using a global closed-loop mixed-signal architecture. Digital control of the 4th-order loop's gain, poles, and zeros enables the prototype to achieve 105 dB SNR, 0.0031% THD+N, 92 dB PSRR, and 85% efficiency when supplying 1 W of power into an 8 Ω load. The fourth paper, by B. Wu and Y. Chiu, proposes an 8th-order Chebyshev-II active-RC band-pass filter with 85–225 MHz programmable center frequency. A new design technique (zero capacitance spread) is introduced to enable integrator frequency compensation. Realized in 40 nm CMOS, the filter features maximum in-band frequency response deviation of 0.2 dB and IIP3 of 31 dBm with 33 mA current consumption from 1.5 V.

The next two papers present innovative ADC architectures for sensor readout applications. The paper by P. Prabha *et al.* reports a VCO-based current-to-digital converter exploiting second-order noise shaping of quantization error and correction of the VCO non-linearity. Fabricated in 0.18 μm CMOS, the circuit consumes 77.8 μA and achieves 900 pA accuracy over 4 μA current range. The paper by C.-H. Chen *et al.* proposes a high-accuracy two-step incremental A/D converter. Fabricated in 65 nm CMOS, the converter demonstrates 99.8 dB dynamic range and 91 dB SNDR for 2.2 V_{pp} input signal and 250 Hz bandwidth. Power dissipation and active area are only 10.7 μW and 0.2 mm^2, respectively.

The next two papers focus on advances in power management circuits. The first of these two papers, by R. Jain *et al.*, describes switch conductance modulation techniques embedded into a 22 nm switched-capacitor DC-DC converter. Effective switch sizes and gate overdrives are adaptively modulated to maximize efficiency across a wide range of output voltages and currents, as well as to actively mitigate output ripple. These techniques are experimentally verified to provide up to 15% efficiency enhancement at low output voltage/current while maintaining a load-independent output ripple of $<$50 mV. The second of the two papers, by A. Shrivastava *et al.*, reports a 130 nm CMOS boost converter that operates with an input voltage as low as 10 mV in order to support energy harvesting from thermoelectrics even at low thermal gradients. The measured efficiency ranges from 53% for a 20 mV input to a peak efficiency of 83% for a 300 mV input, and the design includes support for cold-start from a 220 mV input or an RF kick-start with $-$14.5 dBm of input RF power at 915 MHz.

The next three papers cover a variety of advances in the area of frequency synthesis. The first paper in the section, by A. G. Roy *et al.*, presents enhanced swing ultra-low-voltage class-D differential and quadrature VCOs. The oscillators, realized in 65 nm CMOS, operate off of a 350 mV supply and demonstrate excellent phase noise and figure-of-merit. The clock generator proposed in the second paper, by S. Saeedi and A. Emami, utilizes a phase interpolation-based technique to inject the reference clock edge into an LC VCO and thus limit jitter accumulation to a single reference cycle. The 65 nm prototype operates from 8 to 9.5 GHz, and at 8 GHz achieves an integrated RMS jitter of 490 fs, peak-to-peak periodic jitter of 2.06 ps, and total RMS jitter of 680 fs while consuming 2.49 mW from a 1 V supply. The next paper, by T. Chi *et al.*, presents a frequency multiplier chain architecture exploiting multi-phase sub-harmonic injection locking to generate THz-frequency signals starting from a low mm-wave or RF frequency reference. The SiGe BiCMOS test chips deliver signals in the 485.1 GHz to 510 GHz frequency range with $-$16.6 dBm peak output power.

The next two papers describe advances in RF as well as mm-wave circuits. R. Chen and H. Hashemi present a reconfigurable receiver front-end supporting dual-carrier aggregation. Switched-capacitor RF signal conditioning and complex signal processing enable high flexibility and high selectivity on the filtering profile. Realized in 65 nm CMOS, the front-end supports single- and dual-carrier receiver modes over an input frequency range from 0.1 to 1 GHz. The next paper, by M. Taghivand *et al.*, proposes an efficient 60 GHz short-range OOK transceiver supporting communication with programmable data-rate and scalable power dissipation. The transmitter is supplied by RF energy harvesting circuits operating at 2.45 GHz. Implemented

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in 40 nm CMOS, the radio demonstrates communications over 5 cm with energy efficiency down to 2.6 pJ/bit.

The next three papers in this special issue describe state-of-the-art designs and techniques in the area of high-speed wireline transceivers. The first paper in this section, by M.-S. Chen and C.-K. K. Yang, presents a complete 65 nm CMOS 50–64.5 Gb/s serializing transmitter that achieves 3.1 pJ/bit efficiency while supporting 4 taps of feedforward equalization. These impressive results are enabled by an LC ladder-based design methodology for the equalizer and a novel, low-power 4:1 multiplexor design for the final stage of serialization. The second paper in this section, by T. Dickson *et al.*, demonstrates a 16-lane source-synchronous I/O operating at 12 Gb/s/lane and including support for scaling of link power along with channel conditions. The 32 nm CMOS SOI prototype demonstrates 1.4 pJ/bit (1.9 pJ/bit) efficiencies over 0.75" (20") Megtron-6 PCB traces. The last paper of this section, by Y. Frans *et al.*, describes a 0.5–16.3 Gb/s wireline transceiver embedded in a 20 nm FPGA. Several techniques at the circuit and architecture levels are discussed to achieve high flexibility and operation over a wide range of data-rate. The transceiver demonstrates BER $<10^{-15}$ over a 28 dB loss backplane and meets tight jitter requirements in both common-clock and spread-spectrum clocking.

The paper by K. Song *et al.* concludes the special issue by describing design techniques enabling an LPDDR4 2y-nm mobile DRAM implementation operating at up to 4.3 Gb/s and off of a 1.1 V supply. Specifically, the paper describes techniques such as a multi-channel-per-die architecture, multiple training modes, and a low-swing interface used to meet the aggressive efficiency and data-rate targets of LPDDR4.

The guest editors of this special issue would like to thank the authors for the timeliness and the high quality of their submissions, and would further like to thank the reviewers for their efforts in ensuring that the final manuscripts meet the high standards set by the journal. We sincerely hope you enjoy reading it!

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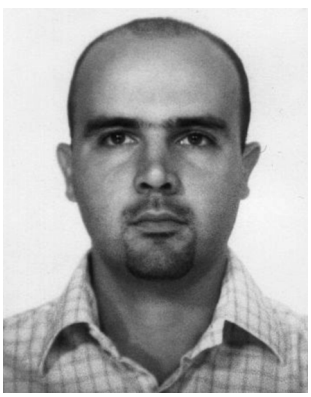

Andrea Mazzanti (S'02–M'09–SM'13) received the Laurea and Ph.D. degrees in electrical engineering from the University of Modena and Reggio Emilia, Italy, in 2001 and 2005, respectively.

During the summer of 2003, he was with Agere Systems, Allentown, PA, USA, as an intern. From 2006 to 2009, he was an Assistant Professor with the University of Modena and Reggio Emilia. In January 2010, he joined the University of Pavia, Italy, where he is now an Associate Professor. He has coauthored over 80 technical papers in journals and international conferences and was named one of the outstanding contributors for the 60 years anniversary of ISSCC. His main research interests cover device modeling and IC design for high-speed communications, RF and millimeter-wave systems. He has participated in several microelectronic research programs, funded by private companies and government. At present, he is in tight cooperation with STMicroelectronics (ST) within the Studio di Microelettronica, a research center supported by ST inside the Engineering Campus of the University of Pavia.

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