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A BJT-based Temperature-to-Digital Converter with ±60mK (3σ) Inaccuracy from -55°C to $+125$°C in 0.16μm Standard CMOS

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Abstract

This paper presents a precision CMOS temperature-to-digital converter (TDC), which senses the temperature-dependent base-emitter voltage of substrate PNPs. Measurements on 20 samples from one batch show that it achieves an inaccuracy of ±60mK (3σ) from -55°C to $+125$°C, after a single room temperature trim. This state-of-the-art result is mainly due to the extensive use of dynamic error cancellation techniques to generate the PNP's collector currents, thus minimizing the spread in their base-emitter voltages, together with a digital PTAT trim to correct for the spread in the PNP's saturation currents. The effect of process variation on the TDC's inaccuracy was investigated by measuring 80 samples from 3 different batches. With the same calibration parameters, they exhibit a maximum untrimmed inaccuracy of ±2°C (3σ) from -55°C to $+125$°C. This drops to ±100mK (3σ) after a single point trim. The proposed TDC thus reduces calibration costs by obviating the need for batch-specific calibration parameters, which would otherwise require the multi-point calibration of several samples. The effect of the PNP's current-gain β was also investigated with the help of a novel β-detection circuit. Implemented in 0.16μm CMOS, the TDC occupies 0.16mm^2 and draws 4.6μA from 1.5 to 2V supply voltages. It achieves a resolution FoM of 7.8pJ°C^2, and a state-of-the-art supply sensitivity of 0.01°C/V.

Index Terms

Temperature-to-digital converter, temperature sensor, substrate PNP, PTAT trim, batch calibration, low cost calibration.

I. Introduction

In precision systems and sensors, knowing die temperature is often quite important, because it can be used to mitigate their cross-sensitivity to temperature [1]–[5]. Temperature-to-Digital Converters (TDCs) have been used to compensate for the temperature dependency of MEMS resonators [1], [2], cancel the self-heating effect in shunt-based current sensors [3], [4], and compensate for curvature in a band-gap voltage reference [5]. In such systems, the TDCs inaccuracy is a significant part of the total error budget, and thus often limits their ultimate performance.

The TDCs in the above-mentioned examples exploit the fact that the base-emitter voltage, V_{BE} of a BJT, is a well-defined function of temperature. BJT-based TDCs have achieved 3σ-inaccuracies ranging from $\pm 0.1^{\circ}$C to $\pm 0.25^{\circ}$C over the military temperature range (-55°C to $+125^{\circ}$C) when implemented in CMOS technology nodes ranging from 0.7μm to 0.16μm [6]–[9]. However, achieving this performance requires a combination of batch calibration, to obtain a set of average calibration parameters, followed by a room temperature trim, to correct the errors of individual TDCs.

Batch-to-batch measurements on a precision TDC in 0.16μm technology [7] show that its average calibration parameters change significantly from one batch to another. Applying the parameters obtained from one batch to TDCs from another batch resulted in an additional error of about 1°C ([7], Table I). So to maximize accuracy, the parameters of each batch of TDCs must be determined as new, significantly complicating their production. This is because these parameters are determined by calibrating multiple samples at multiple temperatures, which is a time consuming and thus expensive process. Furthermore, the resulting parameters must then be associated with the samples of the correct batch, which is a logistical challenge in itself.

This paper presents a BJT-based TDC, which achieves state-of-the-art accuracy, and preserves it from batch-to-batch. In [10], the TDC was briefly described, along with the performance of one batch. This paper discusses the proposed TDC in more detail, and provides experimental data about its batch-to-batch inaccuracy. Compared to [7], the proposed TDC does not need an explicit batch-calibration. As a result, all batches can use the same set of average calibration parameters. These improvements are mainly due to a precision biasing circuit, which ensures that the sensing PNPs are biased at reproducible collector currents. The major remaining source of spread is then the spread in their saturation current I_S, which is corrected by a single room-temperature trim. Since substrate PNPs must be biased via their emitters, their collector current is necessarily a function of their current gain β, which is also process and temperature dependent. To investigate the effect of β, a new method for the direct detection of β is developed, which allows it to be measured for all the samples. Measurements on 80 samples of the TDC from 3 different batches are used to validate the effect of batch-to-batch and β variations.

The rest of this paper is organized as follows. Section II describes the operation of the PNP-based TDC, and discusses its main error sources. Section III discusses the temperature-sensing frontend in detail. Simulation results from a pair of ideally biased substrate PNPs are included to demonstrate that stable average calibration parameters can indeed be achieved in the chosen 0.16μm CMOS process. The precision biasing techniques and β detection circuit are then introduced. Section IV, briefly describes the TDCs readout circuit, which is similar to that of [7]. Section V presents the experimental results, and finally, section VI concludes the paper.

II. BACKGROUND & ERROR SOURCES

Fig.1 illustrates the basic operation of a PNP-based TDC [11]. The heart of the TDC consists of a pair of PNPs (Q_R, and Q_L) biased at a collector current density ratio of 1:p. The base-

emitter voltage, V_{BE} of Q_R (or Q_L) is complementary to absolute temperature (CTAT), while the difference between the two base-emitter voltages, ΔV_{BE}, is proportional to absolute temperature (PTAT). A linear combination of $V_{\text{BE}}$and ΔV_{BE} then results in a relatively constant voltage V_{REF}=V_{BE}+α·ΔV_{BE}, where α is a constant.

The PNPs temperature (T), can then be measured by digitizing α·ΔV_{BE} with respect to V_{REF} with the help of a co-integrated ADC. The result is μ_{PTAT} (=α·ΔV_{BE}/V_{REF}), which varies linearly from ∼0.3 to ∼0.7 over the military temperature range [11]. Alternatively, the ADC may digitize V_{BE} with respect to ΔV_{BE}. The result is X (=V_{BE}/ΔV_{BE}), which varies non-linearly from ∼28 to ∼8 over the military temperature range [7]. The ratio μ_{PTAT} can then be determined in the digital backend by noting that μ_{PTAT}= $\alpha/(\alpha + X)$, where α is a calibration parameter.

The ratio μ_{PTAT}, can then be translated to degrees Celsius by a linear fit as follows [11]:

$$D_{out} = A \cdot \mu_{\text{PTAT}} - B \tag{1}$$

where A (∼600), and B (∼273) are calibration parameters. Due to the non-linearity (curvature) in V_{BE}, μ_{PTAT} as defined above will be slightly non-linear. However, this non-linearity can be made small (<±100mK) by biasing the BJTs with a PTAT current [12], and by ensuring that V_{REF} has a slightly PTAT characteristic ([6], Fig. 3). Using a PTAT/R biasing-circuit can satisfy the first condition, and correctly choosing α in the digital backend satisfies the second. Given that the curvature in V_{BE} is relatively process independent, the key requirement for low-cost calibration is then that V_{BE} and ΔV_{BE} are reproducible over process and supply variations. These two voltages are ideally given by:

$$V_{\text{BE}} = \eta \frac{kT}{q} \ln(\frac{I_C}{I_S}) \tag{2}$$

$$\Delta V_{\text{BE}} = \eta \frac{kT}{q} \ln(p) \tag{3}$$

where η is a process-dependent non-ideality factor, k is the Boltzmann constant, q is the electron charge, T is temperature in Kelvin, I_C and I_S are the collector and saturation currents of the PNP, and p is their collector current density ratio.

In the ratio μ_{PTAT}, η cancels out, so its variation can be disregarded. In a typical single-well process, the PNPs must be biased via their emitters, and will also have non-zero base and emitter resistances. Taking into account their finite current gain (β), and an equivalent emitter resistance (r_S), V_{BE} (for the larger biasing current) and ΔV_{BE} can be rewritten as follows:

$$V_{\text{BE}} \approx \frac{kT}{q} \cdot \ln(\frac{p_E \cdot I_E}{I_S}) + \frac{kT}{q} \cdot \ln(\frac{\beta}{\beta+1}) + p_E \cdot r_S \cdot I_E \tag{4}$$

$$\Delta V_{\text{BE}} \approx \frac{kT}{q} \cdot \ln(p_E) + \frac{kT}{q} \cdot (\frac{\Delta\beta}{\beta \cdot (\beta+1)}) + r_S \cdot (p_E - 1) \cdot I_E \tag{5}$$

In these equations, I_E is the emitter current, and p_E is the emitter current density ratio. $\Delta\beta$ is the difference in β at the two different biasing current levels (I_E and $p_E \cdot I_E$).

As defined in (4), V_{BE} is dominated by the first term, which is a CTAT voltage (with a slope of about $-2\text{mV}/^\circ\text{C}$) and has a slightly non-linear characteristic. It has been shown [12], that the magnitude of this non-linearity is directly affected by the temperature dependency of the biasing current (I_E). A PTAT/R biasing circuit (Fig. 2) provides a PTAT current, which results in less non-linearity than when a constant biasing-current is used. In addition, it provides a supply-independent current, which increases the accuracy of V_{BE}. The PTAT/R circuit consists

of two other PNPs, which are operated at an emitter-current ratio (1:p_{Eb}). An amplifier forces their corresponding ΔV_{BEb} across a biasing resistor (R_b) to generate the biasing current ($I_b = \Delta V_{\mathrm{BEb}}/R_b$). The current mirror 1:$m$ then copies the biasing current to the bipolar core.

Spread in the PNP's saturation current (I_S in the first term of (4)) is the major source of V_{BE} variations. This is because PNP parameters such as base doping (N_B), base width (W_B), and emitter area (A_E) are highly process-dependent [11], [13]. In the chosen 0.16μm process, corner-simulations show that this results in equivalent temperature errors of greater than 5°C. If the spread in I_S ($= \Delta I_S/I_S$) is temperature independent, it will cause a PTAT error in V_{BE}. A single PTAT trim can then correct for this, as well as for other PTAT error sources (i.e., spread in values of R_b, p_{Eb}, or m). However, any temperature-*dependent* spread in these parameters will result in a residual error after trimming [11].

In previous TDCs [6]–[9], [14]–[16], different techniques have been used to reduce the effects of spread in the various parameters of (4) and (5). Choosing a small biasing current (I_E) mitigates the effect of r_S (i.e., the last terms in (4) and (5)) and its variation. Using a β-compensating biasing current [6], [7], effectively suppresses the effect of β on V_{BE} (the second term in (4)). As shown in Fig. 2, this can be implemented by incorporating a β-compensating resistor ($R_{\beta b}$) in the PTAT/R biasing circuit [17]. As a result, the generated biasing current $I_{b\beta} = I_b \cdot (\beta + 1)/\beta$, in which β is the current gain of the PNP (Q_{Rb}) in the biasing-circuit. This ensures that the collector current of the PNP (Q_R) in the bipolar-core is I_b, assuming that the two PNPs have the same current gain. This approach, therefore, will be limited by PNP mismatch.

In order to increase the accuracy of ΔV_{BE}, dynamic element matching (DEM) has been used [6]–[9], [14]–[16] to accurately define p_E (first term in (5)). This will improve the accuracy of ΔV_{BE}, provided that β is current independent (i.e., $\Delta\beta = 0$, in the second term of (5)), or that β

is sufficiently large. In a 0.7μm CMOS process where β is quite large (>25 at 25°C) and $\Delta\beta\sim$0, simulations show that the residual error in ΔV_{BE} corresponds to a temperature error of 10mK ($p_E = 5$, $\Delta p_E/p_E = 1\%$) [11]. In the chosen 0.16μm process, however, β is much lower (<5 at 25°C), and is more current dependent [18]. Therefore, using DEM is less effective. Choosing current levels to minimize the current-dependency in β ($\Delta\beta\sim$0) is still possible, and has been used in [7], [18], and also in this work.

III. SENSING FRONTEND

This section discusses the design of the TDC's temperature-sensing frontend. First, simulation results of a pair of BJTs biased at ideal PTAT currents are discussed, in order to explore the limits on their temperature-sensing accuracy, e.g. due to process-specific non-idealities that are not captured in equations (4) and (5). Some techniques are then proposed to mitigate the error sources in the biasing-circuit to a commensurate level. Finally, a new method for the direct detection of β is introduced.

A. Simulation Results

In order to evaluate the accuracy of a PNP-based TDC, the circuit in Fig. 3(a) is simulated. The PNPs are biased by ideal current sources, so that the emitter currents of Q_R and Q_L are PTAT, and $p_E = 5$. The resulting ΔV_{BE} ($= V_{BE2} - V_{BE1}$) and V_{BE} ($= V_{BE2}$) are then used to calculate D_{out}, as in (1). Over process corners, the temperature error ($D_{out} - T$) is as shown in Fig. 3(b). The untrimmed inaccuracy is quite poor (Fig. 3(b) top): $\pm$10°C over the military range. However, a PTAT-trim (Fig. 3(b) middle) corrects for V_{BE} spread, and substantially improves the results to $\pm$1°C. In order to observe the residual spread, the results are also given after a 3^{rd}-order fit (Fig. 3(b) bottom) to suppress the effects of residual curvature. In these results, the

same average calibration parameters (e.g., A, B, and α) are used for all the corners, as would be required for low cost calibration.

Fig. 4 shows the simulation results when the effect of β in both PNPs is ideally compensated. Therefore, the collector currents of Q_R and Q_L (Fig. 4(a)) are now PTAT, and their ratio $p = 5$. The resulting temperature errors are shown in Fig. 4 (b). The untrimmed error (Fig. 4(b) top) is still quite large, but it can be reduced to less than $\pm$100mK by a single PTAT trim (Fig. 4(b) middle). After a 1^{st}-order fit, however, the amplitude of the residual curvature is $\sim$50mK, which is larger than the residual spread. A 3^{rd}-order fit (Fig. 4(b) bottom) reduces the residual curvature to less than 5mK, revealing a residual temperature error due to spread of only 40mK.

These results show that the effect of process spread on a PNP-based TDC's accuracy can be effectively corrected by a single PTAT trim, provided that its biasing currents are well defined and β effects are properly compensated. In other words, batch calibration can be avoided by designing a precision biasing circuit that accurately defines the collector current of the PNPs.

B. Precision biasing-circuit

The proposed temperature-sensing frontend is shown in Fig. 5. Its basic operation is the same as that of the circuit shown in Fig. 2, however, extra techniques are used to mitigate circuit non-idealities. Each PNP has an area of 5μm$\times$10μm and is biased with a 1:5 emitter-current ratio in both the biasing-circuit, and the bipolar-core. At room temperature, the unit bias current is 160nA, a choice, which keeps $\Delta\beta$ small [18].

A poly resistor R_b (=250kΩ) defines the biasing current, while, as discussed above, a similar resistor $R_{\beta b}$ (=R_b/p_{Eb}=50kΩ) compensates for β variations. However, the effectiveness of this β-compensation scheme relies on their matching, as well as the matching of the BJTs (Q_R and Q_{Rb}). Careful layout was employed to minimize mismatch.

Although a PTAT trim corrects for spread in I_S and in the nominal value of R_b, it cannot correct for non-PTAT error terms in I_C . The main sources of such errors are finite opamp offset and gain, and temperature dependencies of p_{Eb} and m. Errors associated with finite offset and gain are mitigated by the use of a chopped folded-cascode opamp with 90dB of gain. The p_{Eb} current ratio, is implemented by PMOS (cascoded) current mirrors, which are biased in strong inversion. As in [19], the worst-case relative accuracy of this ratio ($\Delta p_{Eb}/p_{Eb}$), can then be approximated as:

$$\frac{\Delta p_{Eb}}{p_{Eb}} \approx \frac{2}{\frac{V_{gs}}{V_T} - 1} \cdot |\frac{\Delta V_T}{V_T}| + |\frac{\Delta \mu_p}{\mu_p}| + |\frac{\Delta C_{ox}}{C_{ox}}| + |\frac{\Delta W}{W}| + |\frac{\Delta L}{L}| \tag{6}$$

where μ_p is the hole mobility, C_{ox} is the oxide capacitance per unit area, L and W are the transistor sizes, V_T is the threshold voltage, and V_{gs} is the gate-source voltage of the two PMOS transistors. The dominant error source is then due to V_T variations [19], whose effect on the accuracy of p_{Eb} depends both on temperature, and on the value of V_{gs}/V_T.

It can be shown that, if $\Delta p_{Eb}/p_{Eb}$ is constant over temperature, it results in a PTAT error term in V_{BE}. Therefore, it can be corrected by the same PTAT trim used to correct for spread in I_S [11]. This is not the case for temperature dependent $\Delta p_{Eb}/p_{Eb}(T)$ spread. Another source of inaccuracy derives from errors in copying the currents in the biasing-circuit to the bipolar-core. The relative inaccuracy of this current-mirror ratio $\Delta m/m$ (Fig. 2), contributes to the overall error in D_{out} in exactly the same manner as $\Delta p_{Eb}/p_{Eb}$.

To mitigate such errors, the current mirror ratio p_{Eb} is dynamically matched (DEM1), in the same way as the current mirror ratio p_E (DEM2). For the same reasons, a similar approach was recently used in [16]. Furthermore, to ensure that biasing currents are accurately copied from the biasing-circuit to the bipolar-core, the two banks of current mirrors are dynamically swapped

(Bank-Swap). Since the two banks are designed to generate the same current levels, this is done by simply inserting some extra switches, in series with each current bank.

C. Current Gain Detection

Although the β-compensation scheme (Fig. 2 and Fig. 5) corrects for the effect of β on $V_{\rm BE}$, it does not correct for its effect on $\Delta V_{\rm BE}$. This is because, β is slightly dependent on current density in the chosen process, i.e., $\Delta\beta \neq 0$ in (5). If β does not spread, the resulting error in $\Delta V_{\rm BE}$ is reproducible (see (5)). However, simulations on the Fig. 4 circuit show that β changes significantly over temperature and process corners (Fig. 6). The corresponding temperature-dependent errors in $\Delta V_{\rm BE}$, cannot then be corrected by the PTAT trim.

To experimentally investigate the effect of β spread, the frontend of the proposed TDC (Fig. 5) is configured to determine the β of Q_{Rb}. Via switch S_β (Fig. 5), the β-compensation can be turned on and off, so that the generated biasing-current changes from $\Delta V_{\rm BE}/R_b$ to $(\Delta V_{\rm BE}/R_b)\cdot(1+\beta)/\beta$. The ratio of these two currents $((1+\beta)/\beta)$ contains β information. In this design, the biasing current are sensed via a sense resistor R_β (350kΩ). The resulting voltage V_β, is then digitized with respect to $\Delta V_{\rm BE}$ in the same way as $V_{\rm BE}$, resulting in the ratio $X_\beta = V_\beta/\Delta V_{\rm BE}$. The ratio of X_β when S_β is on/off can then be calculated in the digital backend to obtain β. Since the two conversions are made in quick succession ($<$200 ms), the die temperature and hence $\Delta V_{\rm BE}$ can be assumed to be constant. Since the measurement is ratiometric, gain errors e.g., due to spread in the current mirror ratios and the value of R_β, will not affect the accuracy of β detection. $\Delta V_{\rm BE}$ is also quite insensitive to the state of S_β, because the change in the biasing-currents is small (12% at 25°C, and $<$25% over the military range). Simulation show that the corresponding change in $\Delta V_{\rm BE}$ is 0.002% at 25°C, and is less than 0.04% over the military temperature range.

IV. Readout circuit

Fig. 7 shows the overview of the TDC. It consists of a frontend that generates V_{BE}, V_β, and ΔV_{BE}, which are then fed to an incremental ADC. The ADC's output in the normal mode is the ratio X ($= V_{\text{BE}}/\Delta V_{\text{BE}}$), however it can be configured to output $V_\beta/\Delta V_{\text{BE}}$, or $V_{ext.}/\Delta V_{\text{BE}}$. Adding an offset to X effectively adds a scaled version of ΔV_{BE} to V_{BE}, and thus realizes a PTAT trim. The ADC is designed for high resolution ($\sim$4mK$_{rms}$ in ¡100ms conversion time), to enable digital calibration and trimming.

As in [7], a 2-step SAR$-\Sigma\Delta$ architecture is used for ADC (Fig. 8), to digitizes X ($\sim$8 to $\sim$28). In the first step, a 31-element capacitor DAC whose unit value (C_S) is 120fF, the 1^{st} integrator, and the comparator implement a 6-step SAR algorithm to find the integer part of X. This is enabled by successively comparing V_{BE} with $K{\cdot}\Delta V_{\text{BE}}$, where $K = 1:31$. In the next step, a 2^{nd}-order $\Sigma\Delta$ modulator balances V_{BE} against reference voltages $(K_{SAR}-1){\cdot}\Delta V_{\text{BE}}$ or $(K_{SAR}+1){\cdot}\Delta V_{\text{BE}}$, where K_{SAR} is the result of the first step. From the resulting bit-stream (bs) average, $\mu_{\Sigma\Delta}$, the final result is then obtained as $X = K_{SAR} + 2\cdot\mu_{\Sigma\Delta}$.

Correlated double sampling (in the 1^{st} integrator), and system-level chopping in $\Sigma\Delta$ ensure ADC's low offset ($<1\mu$V at 25°C) and $1/f$ noise. As in [7], high accuracy is obtained by using dynamic element matching (DEM) of the sampling capacitors. This involves shuffling the position of the 1 and K sampling capacitors of the DAC array to average out mismatch errors in the $(V_{\text{BE}}\cdot C_S)/(\Delta V_{\text{BE}}\cdot K\cdot C_S)$ ratio.

Each of the ADC's integrators is built around an energy-efficient current-reuse OTA (Fig. 8). Such amplifiers have the same energy efficiency as the inverter-based amplifiers used in [20], [21], without the need for dynamic biasing. As a result, they benefit from lower complexity, lower noise (no additional kT/C noise from the biasing circuit), and fully differential properties. Using

the same architecture, the first amplifier draws 480nA, while the second draws 120nA ($0.25\times$ scaled in size).

V. Experimental Results

Implemented in a 0.16μm CMOS technology, the TDC core occupies 0.16mm^2 and draws 4.6μA from a nominal 1.8V supply. The chip micrograph is shown in Fig. 9 (top). For flexibility, the digital logic, which implements the SAR algorithm and the sinc^2 decimation filter for the $\Sigma\Delta$ modulator, were realized off-chip. The designed TDC is very robust to DC supply variations (0.01°C/V) as shown in Fig. 10 (b), which is mostly obtained due to the robustness of the precision biasing-circuit. When clocked at 35kHz, the TDC achieves a kT/C-limited resolution of 15 mK$_{rms}$ in 5ms of conversion time ($t_{conv.}$). Where necessary (e.g., at the trimming temperature), the resolution can be further improved by a factor of $\sqrt{2}$ with every doubling of $t_{conv.}$. Fig. 10 (a) shows the achieved rms-resolution as a function of $t_{conv.}$.

In order to investigate the TDC's robustness, 3 different batches have been characterized. Each batch corresponds to a different fabrication run with a time difference of a few months, and so can be expected to be somewhat different from each other. However, they do not represent batches from the corners of the technology. To explore the effect of switch leakage at high temperatures, 2 batches were fabricated in a different flavor, which allowed the TDC's sampling switches to be implemented with UHV_T (ultra-high threshold) switches, instead of the HV_T switches used in the other 2 batches. A summary of the fabricated batches is shown in Fig. 9 (bottom).

A. Batch-Calibration

To determine the TDC's inaccuracy after individual batch-calibration, 20 samples from batch-1 with UHV_T switches (grey in Fig. 9 (bottom)) were characterized. The samples were packaged in

ceramic and characterized from -55°C to $+125$°C. A PT-100 thermistor, which was calibrated to less than 1mK, and which was in a good thermal contact with the TDCs, was used as a temperature reference. The value of α is optimized for minimum curvature by fitting μ_{PTAT} to a straight line in a least-mean-square sense, this process also results in the values of A and B. The result is a 3σ-inaccuracy of $\pm$0.4°C (untrimmed), $\pm$0.1°C (PTAT-trimmed), as shown in [10]. The residual non-linearity is then only $\pm$40mK, which can be further reduced by using a fixed 3^{rd}-order polynomial. This results in a 3σ-inaccuracy of $\pm$380mK (untrimmed), and $\pm$60mK (PTAT-trimmed), as shown in Fig. 11.

In order to perform a PTAT trim, an offset trim on X is made in the following way:

$$X_{trim}(T) = X(T) + \Delta X(25°\text{C}) \tag{7}$$

$$\Delta X(25°\text{C}) = X_{avg}(25°\text{C}) - X(25°\text{C}) \tag{8}$$

where $X_{trim}(T)$ is the offset-trimmed value of X, $X(T)$ is the raw output of the TDC without trimming, and $\Delta X(25°\text{C})$ is the trimming factor calculated at room temperature. $X_{avg}(25°\text{C})$ and $X(25°\text{C})$ are the batch average, and the individual TDC's output at 25°C. The PTAT-trimmed output is then calculated as:

$$D_{trim}(T) = A \cdot \frac{\alpha}{\alpha + X_{trim}(T)} - B \tag{9}$$

The TDC's inaccuracy was also recorded for different modes of the biasing-circuit. Table. I summarizes these batch-calibrated results, and indicates how accuracy improves as the various techniques are applied. The same techniques also improve the TDC's supply sensitivity, and validating their effectiveness on the accuracy. Table. II summarizes the batch-calibrated perfor-

mance of the TDC, and compares it with previous works. The designed TDC shows a superior performance in terms of inaccuracy and supply-sensitivity.

B. Batch-to-Batch

Results of the same design in the same package have been also observed for different batches. Fig. 12 shows these results for the two HV_T batches (blue box in Fig. 9 (bottom)). These results are only shown with a 1^{st}-order fit (i.e., A, B, α). The average calibration parameters of the first batch, are applied to the second. Fig. 12 (top) and (bottom) then present the untrimmed, and PTAT-trimmed results respectively.

PTAT-trim is now effectively correcting the considerable (but PTAT) spread between the two batches (max=2°C), and maintaining their batch-calibrated inaccuracy ($<$100mK) over the military temperature range. The value of β of these samples was also measured as shown in Fig. 12 (right), indicating a similar average current gains for the two batches, but with a spread of $\pm$10%. The effect of this relatively small spread on ΔV_{BE} is negligible. Similar results were obtained for the third UHV_T batch with respect to the first batch (red box in Fig. 9 (bottom)), although this had a slightly smaller untrimmed PTAT spread (max=1°C). Again there was no significant shift in the average value of β.

C. Voltage calibration

Although thermal calibration accurately corrects for PTAT variations in D_{out}, a considerable amount of time is required to obtain good thermal equilibrium between the TDCs and the PT-100 temperature reference. A low cost alternative is voltage calibration, which is a two-step process, and uses ΔV_{BE} to estimate die temperature [23], [24]. In the first step, a known external voltage (i.e., $V_{ext.}$, which is measured by an external Keithely-2002) replaces V_{BE} (Fig. 6). From the

measured $X_{cal} = V_{ext.}/\Delta V_{\mathrm{BE}}$, ΔV_{BE} is extracted, based on which the die temperature can be calculated. Immediately after this, a second measurement is made to find $X = V_{\mathrm{BE}}/\Delta V_{\mathrm{BE}}$. Since the two measurements are done in less than 200ms, the die temperature can be assumed to be constant, and thus the obtained results can be used to trim the TDC.

The accuracy of voltage calibration relies on the reproducibility of ΔV_{BE}, which is relatively independent of process parameters, as can be seen from (3) and (5). In the implemented TDC, high accuracy is obtained by dynamically matching the ratio p_E and swapping the BJTs (Q_R and Q_L). Measurements on the first two batches (blue box in Fig. 9 (bottom)) show that the spread in ΔV_{BE} corresponds to less than $\pm$0.1°C error at room temperature (Fig. 13 (top)). The linear fitting parameters (C, and D in Fig. 13(a)) which are used to estimate T from ΔV_{BE}, are extracted from the first batch. As shown in Fig. 13 (bottom), the combination of voltage-calibration and PTAT trimming results in a 3σ-inaccuracy of $\pm$0.3°C over the military temperature range for the two batches.

VI. Conclusion

In this paper, a precision temperature-to-digital converter has been presented. The more accurate biasing-circuit for the PNPs combined with a PTAT-trim enabled a low-cost calibration. Samples of 3 different batches have been measured to verify the effectiveness of the techniques and calibration method, in the presence of process variations. As a result, the calibration parameters can be kept constant over the batches, while a single point trim corrects the variation between them. Unlike prior art, the proposed TDC verified that batch-calibration does not need to be a necessary step in its production. In addition, with the help of a new method, BJT's β is determined, which helped to observe its effect on the TDC's inaccuracy. Constant calibration parameters, combined with the voltage-calibration are showed, which provides a low-cost method

for production of the TDC.

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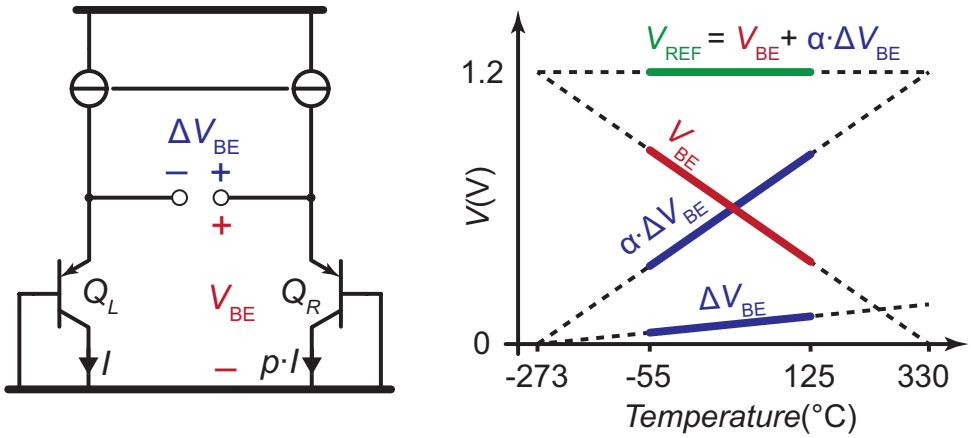


Figure 1. Basic operation of a PNP-based TDC.

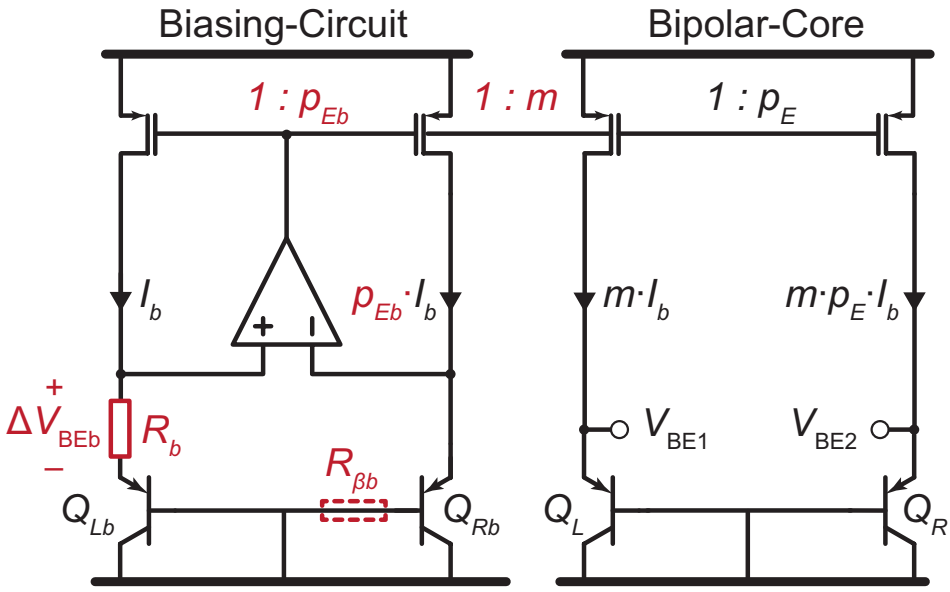
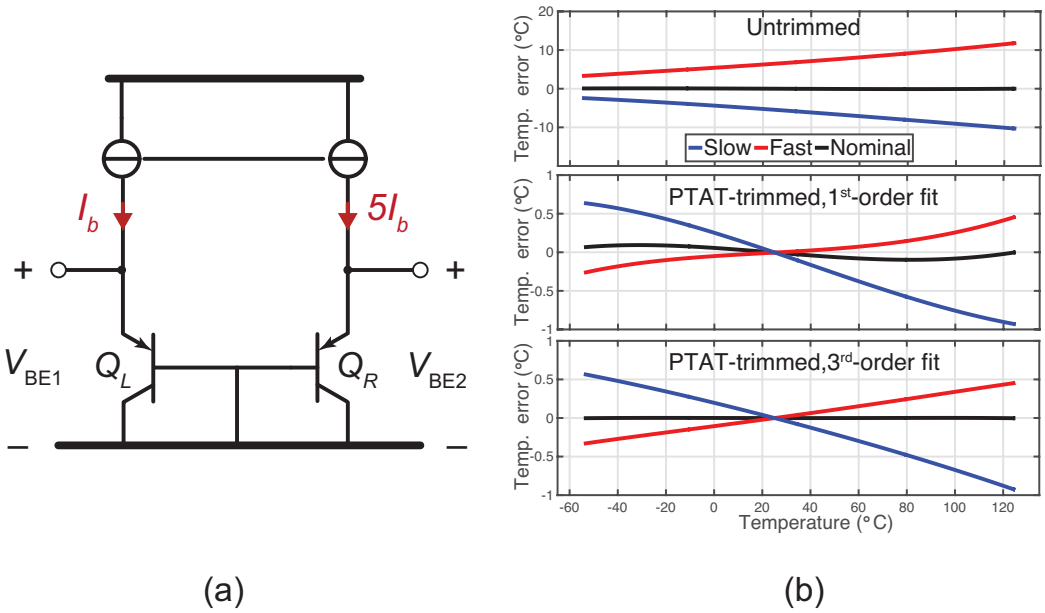


Figure 2. PTAT/R biasing circuit, with (optional) β compensation.



(a) (b)

Figure 3. (a) Simulated PNPs with ideal PTAT emitter currents. I_b = 160nA at 25°C, $Q_L = Q_R$ = 5μm×10μm. (b) Temperature errors are obtained using the same calibration parameters

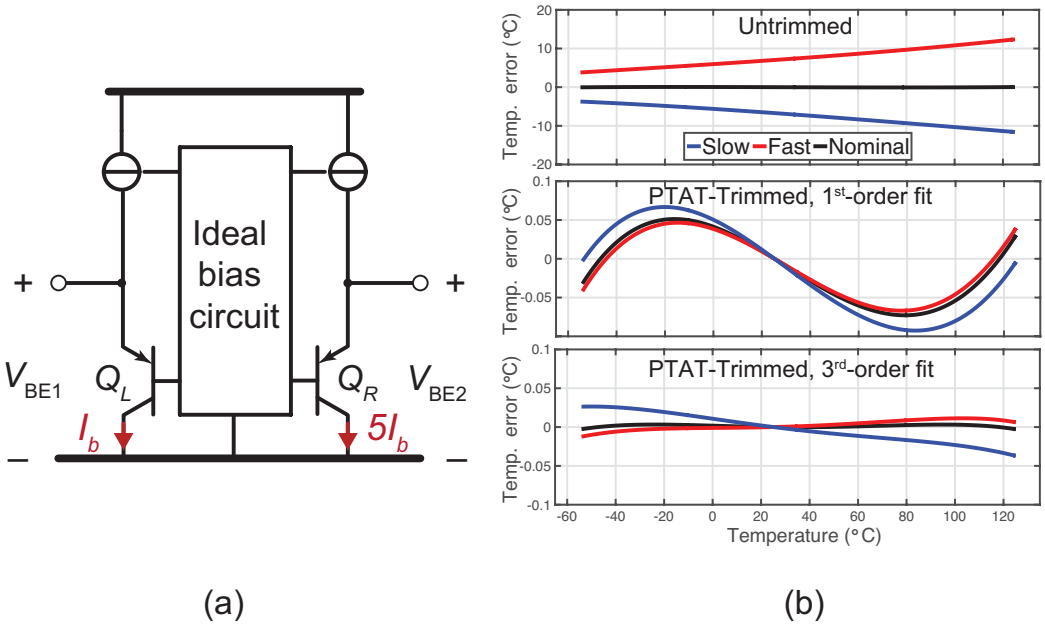


Figure 4. Simulated PNPs with ideal PTAT emitter currents. I_b = 160nA at 25°C, $Q_L = Q_R$ = 5μm×10μm. (b) Temperature errors are obtained using the same calibration parameters

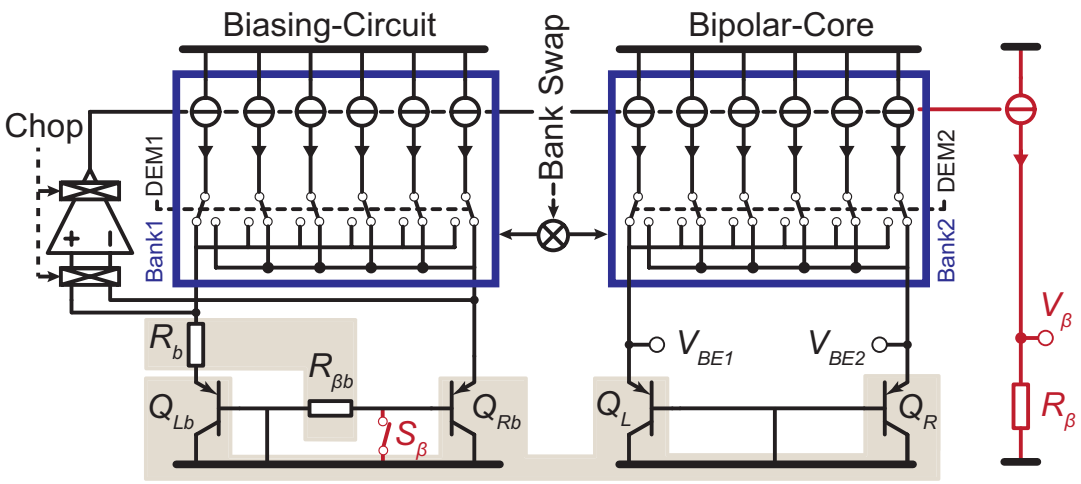


Figure 5. Sensing Front-end. $V_{BE}=V_{BE2}$, $\Delta V_{BE}=V_{BE2}$-V_{BE1}. (Grey) Inter-digitated, and symmetric layout. (Red) β-detection circuit.

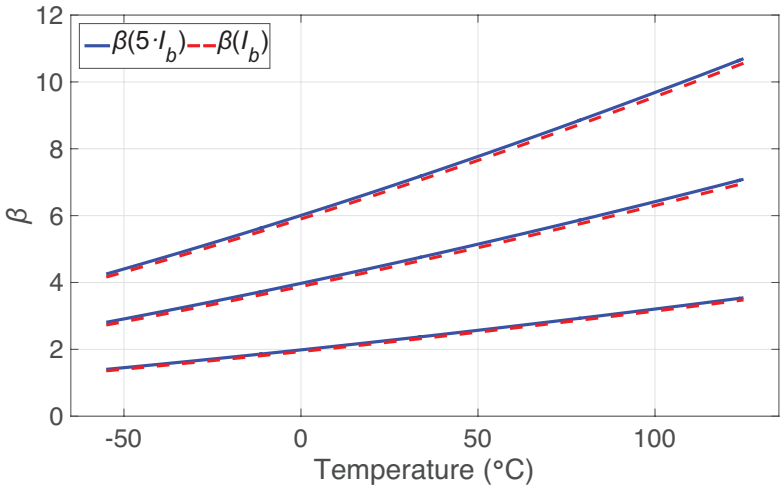


Figure 6. Simulated β at different corners, when biased at I_b (=160nA), and 5×I_b.

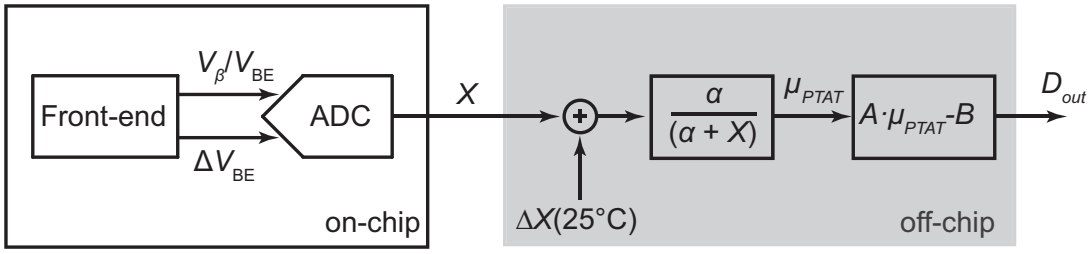


Figure 7. Overview of the temperature sensing system.

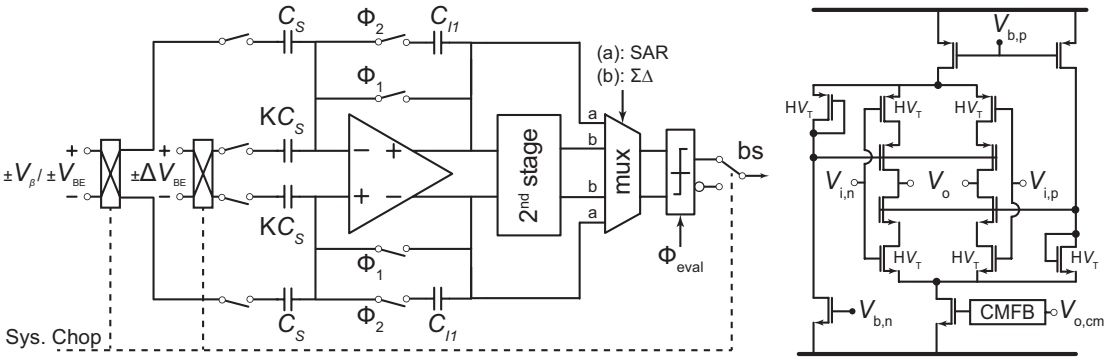
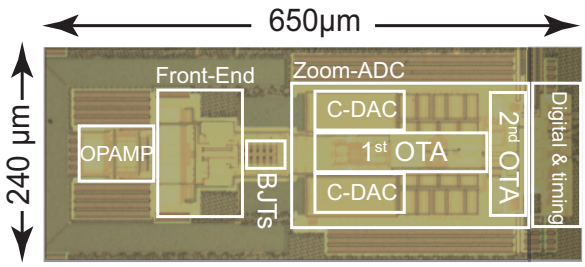


Figure 8. (Left) SAR-ΣΔ ADC. In SAR mode K searches for K_{SAR}. In ΣΔ mode K is selected depending on the bs. K = K_{SAR}+1 (bs=1), or K=K_{SAR}-1 (bs=0). (Right) current-reuse amplifier, which is used in both first and second stage integrators.



	HV_T	UHV_T
Batch-1	20-Samples	20-Samples
Batch-2	20-Samples	
Batch-3		20-Samples

Figure 9. (Top) chip micrograph. (Bottom) fabricated samples of the TDC, (grey) samples, which are used for batch-calibrated performance, (dotted boxes) samples, which are used for batch-to-batch measurements.

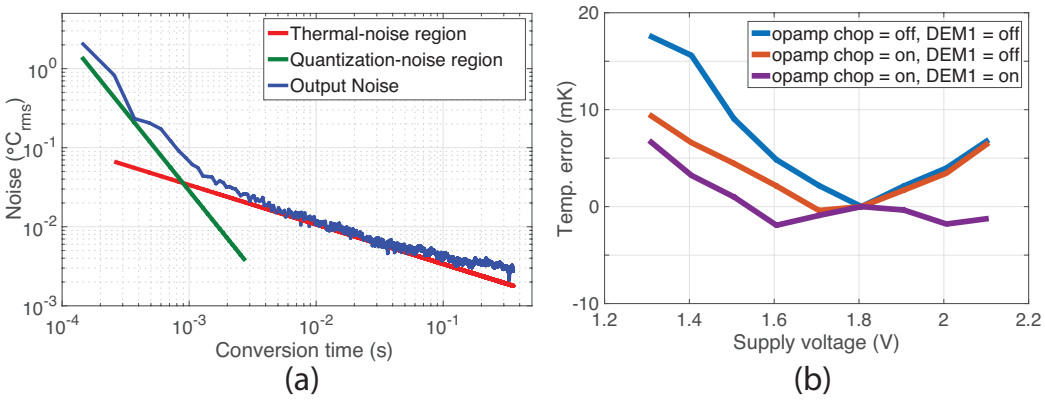


Figure 10. (a) Output noise versus conversion time. (b) Supply sensitivity.

TABLE I
ACCURACY IMPROVEMENT WITHIN A BATCH

Opamp chop	DEM1	Bank swap	Unrimmed InAcc. (3σ)	Trimmed InAcc. (3σ)
OFF	OFF	OFF	±700mK	±300mK
ON	OFF	OFF	±400mK	±100mK
ON	ON	OFF	±380mK	±70mK
ON	ON	ON	±380mK	±60mK

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

Item	Tech (µm)	Area (mm^2)	Supply (V)	Current (µA)	T. Range (°C)	Inaccuracy (±3σ error)	PSS (°C/V)	Res. (m°C) t_{conv} (ms)	Res. FOM* (pJ°C²)	Relative** InAcc. (%)	Reference type
This† work	0.16	0.16	1.5–2	4.6	-55 – 125	±60mK	0.01	15 (5)	7.8	0.07	Self-referenced
[6]	0.7	4.5	2.5–5.5	75	-55 – 125	±100mK	0.03	10 (100)	1875	0.11	Self-referenced
[7]	0.16	0.08	1.5–2	3.4	-55 – 125	±150mK	0.5	20 (5.3)	11	0.17	Self-referenced
[22]	0.065	0.2	1.5	0.5	-40 – 130	±400mK	N/A	125 (2)	23	0.47	External Voltage
[15]	0.7	0.8	2.9–5.5	55	-45 – 130	±150mK	0.05	3 (2.2)	3.2	0.17	External Frequency

* Res. FoM = (Power · t_{conv}) · (Res.)²

** Relative InAcc. = 2 · (Inaccuracy) / (T. Range) × 100

† Batch-calibrated results, with a 3rd-order fit.

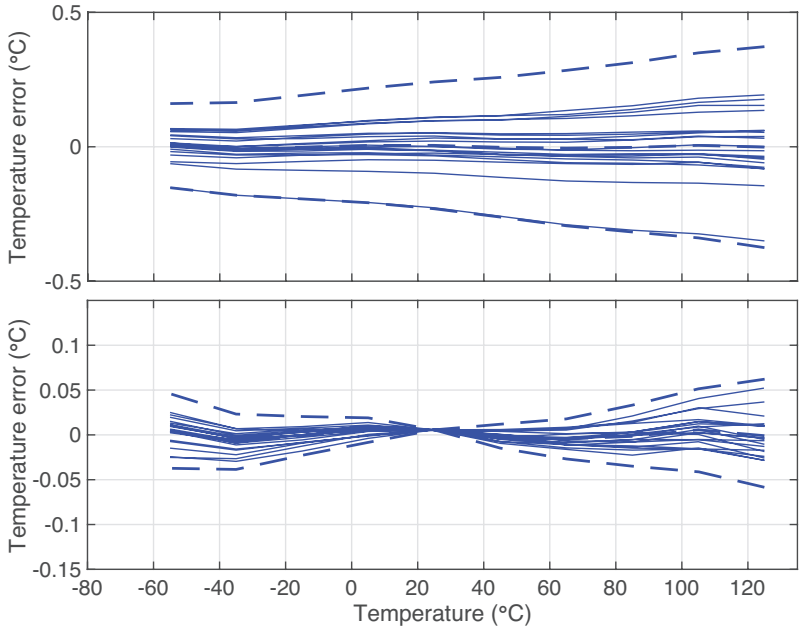


Figure 11. Measured temperature inaccuracy within a batch, using 3rd-order polynomial fit. (Top) untrimmed (Bottom) PTAT-trimmed. Dashed lines represent the average, and ±3σ limits.

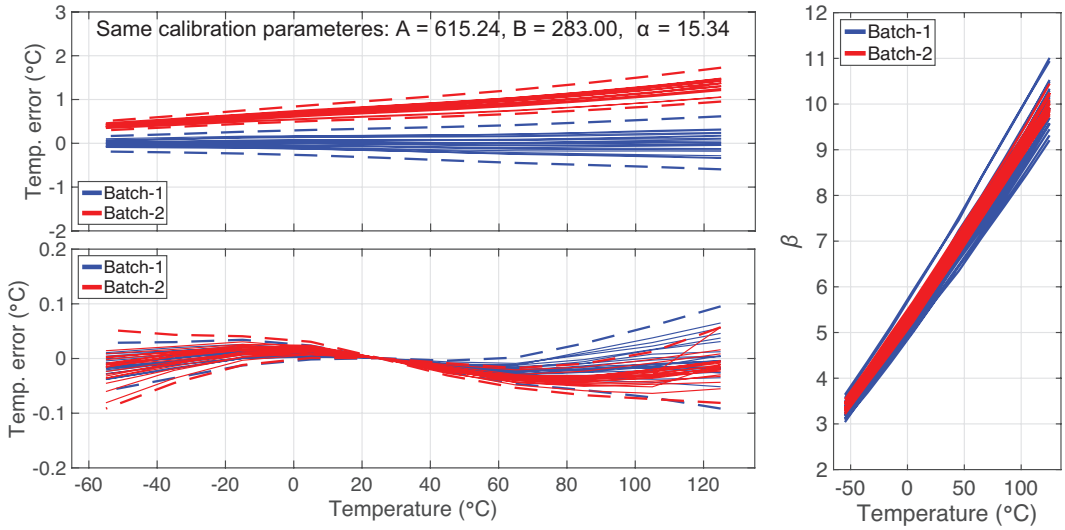


Figure 12. Measured temperature inaccuracy using the same calibration parameters A, B, and α. (Top) untrimmed (Bottom) PTAT-trimmed. Dashed lines represent the average, and ±3σ limits. (Right) measured β.

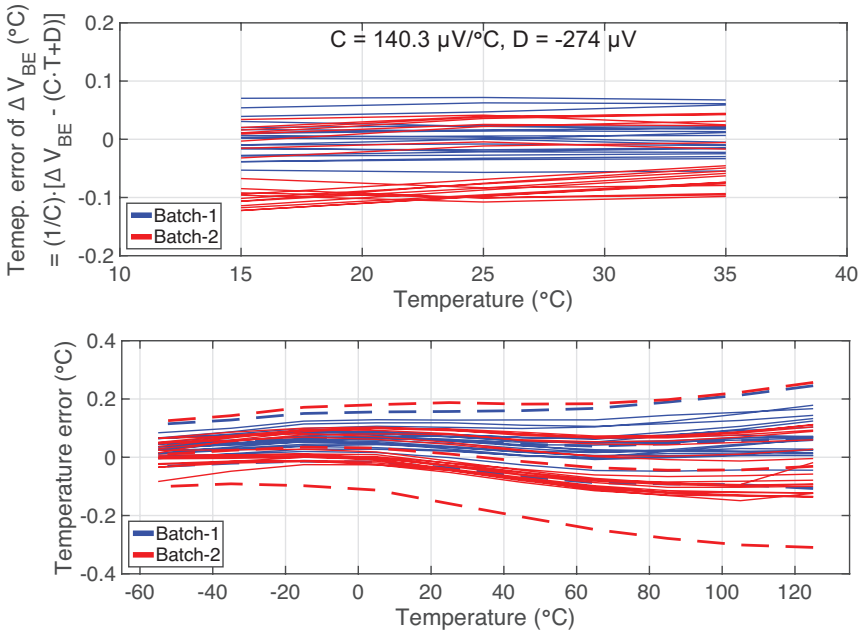


Figure 13. (Top) measured temperature inaccuracy associated with ΔV_{BE}. (Bottom) measured temperature inaccuracy after voltage calibration. The parameters C, and D are extracted from Batch-1. The parameters A, B, and α are as used in Fig. 12.