Outphasing Class-E Power Amplifiers: From Theory to Back-Off Efficiency Improvement

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***Abstract*— This paper presents an analysis of outphasing class-E power amplifiers (OEPAs), using load-pull analyses of single class-E PAs. This analysis is subsequently used to rotate and shift power contours and rotate the efficiency contours to improve the efficiency of OEPAs at deep power back-off, to improve the output power dynamic range (OPDR), and to reduce switch voltage stress. To validate the theory, a 65-nm CMOS prototype, using a PCB transmission-line-based power combiner was implemented. The OEPA provides +20.1 dBm output power from $V_{DD} = 1.25$ V at 1.8 GHz with more than 65% drain efficiency (DE) and 60% power-added efficiency (PAE). The presented technique enables more than 49-dB OPDR and 37% DE and 22% PAE at 12-dB back-off with reduced switch voltage stress.**

***Index Terms*— Class-E, efficiency contours, outphasing power amplifier (PA), power back-off efficiency, power contours, reliability.**

I. Introduction

NOWADAYS, modern communication systems necessitate complex modulated signals [e.g., orthogonal frequency division multiplexing (OFDM) and 64-quadrature amplitude modulation (QAM)] with high peak to average power ratios (PAPRs). The demands on the power amplifier (PA) in these systems are manifold: the PA mainly works in back-off, must be sufficiently robust, and must have sufficiently high efficiency.

Among the various classes of PAs, class-E PAs are of great interest. Zero voltage switching (ZVS) and zero slope switching (ZSS) conditions for the switch waveform in class-E PAs result in non-overlapping voltages and currents for the switch and hence yield high efficiency (ideally 100%) [1]. Due to switch-mode operation, a single class-E with constant supply voltage only allows phase modulation or ON–OFF keying modulation. Supply modulation through envelope elimination and restoration [2] or load modulation through outphasing [3] is necessary to also enable amplitude modulation.

Outphasing class-E PAs (OEPAs) are getting more popular. Their performance is weakly dependent on process variations due to the switch-mode operation of the branch amplifiers [4]. Other advantages of OEPAs include maintaining high efficiency at a relatively wide output power back-off range and digital compatibility due to the phase-only control [5].

However, some issues with OEPAs need to be addressed. Firstly, the maximum voltage of the switches can be very high [6], [7]. Being implemented by transistors, there is a trade-off between switch performance (e.g., on-resistance, drive power, and speed) and reliability (e.g., life time) which makes the design of class-E PAs challenging [8]. Secondly, high-order modulated signals require a high output power dynamic range (OPDR). However, mismatch between the two paths in outphasing system limits the OPDR. Thirdly, OPEAs require power combiners. For high efficiency at power back-off, non-isolating power combiners are used [9]. This results in load pulling between the two branch amplifiers yielding the ZVS and ZSS conditions to be violated and consequently dropping the efficiency well below its maximum (ideal) 100% [10].

Recently, some papers reported on improving the efficiency of OEPAs in power back-off. In [10], variable duty cycle combined with variable drain capacitance and with a tunable load network was used to maintain ZVS and ZSS conditions in power back-off up to (ideally) 9-dB back-off. The CMOS implementation of the technique, presented in [10], was employed in [11] at 1.85 GHz. For higher than (ideally) 9-dB back-off levels, the outphasing technique employed in [10] and [11] resulted in a reduction of the efficiency due to non-zero switching losses (non-ZVS condition). Due to practical limitations on the minimum feasible duty cycle at high frequencies in [11], the ZVS and ZSS conditions were satisfied for 6 dB of back-off range which yielding lower than 10% power-added efficiency (PAE) at 10-dB back-off. Furthermore, amplitude errors limited the OPDR to 30 dB in [10]. In [12], an isolating power combiner was used and supply voltage switching was implemented to maintain high efficiency at power back-off. However, this latter technique requires a highly efficient dc–dc converter not to compromise the overall efficiency of the OEPAs. Non-isolating package-integrated transformer-based power combiners with Chireix compensation elements along with cleverly chosen class-E PA design parameters (denoted as load-insensitive class-E PA) were introduced in [5]. This load-insensitive class-E design concept provides 100% efficiency only for ohmic loads while Chireix compensation elements null the imaginary parts of the branch PA loads at (typically) only two power back-off levels. However, for higher back-off levels, OEPA efficiency reduces rapidly due to the non-zero imaginary part of the loads. Adaptive compensation elements [13] or four-way outphasing systems [14] can be used to reduce the imaginary part of

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the loads at lower power levels but add complexity and lossy elements at the output that compromise the efficiency. Variable duty cycle was used in [15] to ensure load-insensitive design conditions across a wide frequency range. The technique in [15] aimed at minimizing the back-off efficiency drop in the frequency range 1.84–2.14 GHz with respect to the nominal design at 2.14 GHz.

In [7], we presented a new technique to improve the back-off efficiency for OEPAs with load-insensitive class-E designs. Output power contours and efficiency contours of the class-E PAs on the Smith chart were shown to rotate and the power contours were shown to shift by changing just a few class-E design parameters. This rotation and shift were used to considerably improve the efficiency of OEPAs at back-off. Moreover, it was shown that this technique also improves the OPDR and reduces switch voltage stress at back-off.

In contrast to [10] and [11], in [7] we used a load-insensitive design which ideally yields 100% efficiency at (almost) 0- and 10-dB back-off levels and more than 95% efficiency between 0- and 12-dB back-off levels. Moreover, theoretically this yields an infinite OPDR without requiring to tune any parameter. Using our technique in [7], the second compensation point can be shifted up to 20 dB into back-off. This not only can improve the average efficiency of the OEPAs for modulated signals with high PAPRs, but is also promising for applications with output power control or for multi-mode (standard) PAs with different average output power levels [16]–[18]. Also, our technique does not require to tune the load while parameter tuning is done prior to the series output filter of the class-E PAs to change the (very non-sinusoidal) voltage at the switching node. Moreover, parameter tuning is employed at power back-off which helps to obtain high efficiency both at back-off and at maximum output power. This paper provides more insight to the technique, shows detailed design considerations, and provides more measurement results at a higher frequency.

There are other previously published works on the derivation of class-E design equations as well as the effect of changing design parameters on performance and reliability of class-E PAs. The design equations for variable duty cycle, ZVS, and ZSS conditions were presented in [19], while [20] derives similar design equations for variable duty cycle and (only) ZVS condition. However, under non-nominal load conditions ZVS and ZSS conditions, both are violated. As a result, the design equations in [19] and [20] cannot be employed to load pulling nor to study the effect of changing design parameters on load-pull contours. Therefore, new mathematical design equations were derived for general switching conditions (non-ZVS and non-ZSS) similar to [6] and [21] but now including the dc-feed inductor loss as well as the switch conduction loss. These derivations are not included in this paper because of length reasons and only the results are summarized and used to explain our efficiency enhancement technique.

A few publications provide a theoretical model for OEPAs. The presented analyses in [22] and [23] are (only) for a special case; using ideal loss-less components, RF choke as the dc-feed inductor and 50% duty cycle. The presented semi-analytical design methodology in [24] is for a more general case of arbitrary dc-feed inductor and arbitrary duty cycle.

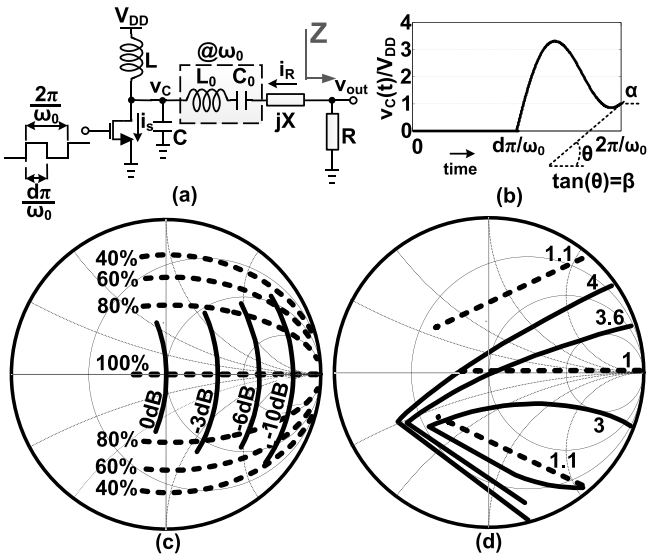

Fig. 1. (a) Single-ended class-E PA. (b) Normalized switch voltage. Load-pull plots for $q = 1.3$, $d = 1$, and $m = 0$. (c) Normalized output power (solid curve) and efficiency (dotted curve) contours. (d) Maximum switch voltage normalized to V_{DD} (solid curve) and normalized output voltage amplitude (dotted curve).

However, the presented theory only works for one outphasing angle where both the branch class-E PAs satisfy predefined switching conditions (e.g., the ZVS). Then, to have a full picture of the outphasing operation, in [24], simulations were conducted using a commercial computer program.

This paper is organized as follows. A review of the class-E PAs, a load-pull study of load-insensitive class-E PAs, and the effect of changing class-E design parameters on load-pull contours are presented in Section II. The presented approach in this paper to study the OEPAs (in Section III) and our efficiency improvement technique at back-off (in Section IV) is based on the load-pull study of the class-E PAs presented in Section II. This approach makes it possible to theoretically obtain the PA loads, normalized output power, efficiency, and reliability-related maximum switch voltage for all the outphasing angles and as a result the OPDR. The presented approach can be used with any arbitrary dc-feed inductor (including loss), arbitrary duty cycle, considering the switch conduction loss and we use standard Smith chart representation. Second-order effects that come into play for hardware realizations are discussed in Section V. The design of a demonstrator OEPA in 65-nm CMOS that implements the proposed technique and measurement results thereof are given in Sections VI and VII, respectively. Finally, the conclusions are summarized in Section VIII.

II. Class-E Power Amplifier Basics

Fig. 1(a) shows a class-E PA, where the MOS transistor acts as a switch driven by a square-wave input signal with (angular) frequency ω_0 and duty cycle scaling factor of d where $d = 1$ corresponds to 50% duty cycle. The general switching conditions are defined as

$$v_c\left(\frac{2\pi}{\omega_0}\right) = \alpha V_{DD} \quad \text{and} \quad \frac{dv_c}{dt}\left(\frac{2\pi}{\omega_0}\right) = \beta\omega_0 V_{DD} \qquad (1)$$

where v_c and V_{DD} are the switch and supply voltage, respectively. L and C form the primary LC tank to shape the switch voltage according to the required values of α and β, shown in Fig. 1(b) [25], [26]. The relative resonance frequency of this tank is defined [21] as

$$q = \frac{1}{\omega_0 \sqrt{LC}}. \tag{2}$$

The second tank, by L_0 and C_0, is a bandpass filter to filter out load current harmonics. A matching network (not shown here for simplicity) provides the load of the PA ($R + jX$) from the nominal 50-Ω antenna impedance. The relation between circuit elements (L, C, X, and R), V_{DD}, ω_0, and output power P_{out} is formulated by a K-design set [21]

$$K = \{K_L, K_C, K_X, K_P\} = \left\{ \frac{L\omega_0}{R}, RC\omega_0, \frac{X}{R}, \frac{RP_{\mathrm{out}}}{V_{\mathrm{DD}}^2} \right\}. \tag{3}$$

The K-design set for non-ZVS non-ZSS arbitrary d and q and taking into account the switch resistance R_{ON} is derived in [6], yielding $K = K(q, d, m, \alpha, \beta)$, where $m = \omega_0 R_{\mathrm{ON}} C$.

A. Load-Pulling Class-E PAs

For the so-called load-insensitive design [5], [27], a class-E PA is conventionally designed to have $q = 1.3$, $d = 1$, ZVS ($\alpha = 0$), and ZSS ($\beta = 0$). Assuming an ideal switch ($m = 0$), the K-design set elements can be obtained from, e.g., [6] as $\{K_L, K_C, K_X, K_P\} = \{1.04, 0.58, 0.28, 1.26\}$. For given P_{out}, ω_0, and V_{DD}, the component values in Fig. 1(a) can then be calculated from the K-design set equations in (3).

For a load-pulling analysis, this ideal class-E PA is subjected to different loads. For this, jX is kept constant and only the load impedance Z, represented by its nominal (real) value R in Fig. 1(a), is changed. For simplicity, we normalize both the real and imaginary parts of Z to R

$$Z = kR + jk'R. \tag{4}$$

Note that for the nominal load, $k = 1$ and $k' = 0$. For fixed q, d, and m, under non-nominal load conditions, ZVS and/or ZSS conditions are violated. A full mathematical derivation of the switch voltage and current is beyond the scope of this paper and can be found in, e.g., [6].

These equations can be rewritten to get important properties of both the switch voltage $v_C(t)$ and the switch current $i_s(t)$. This allows to derive, e.g., P_{out} normalized to that at nominal load conditions, the efficiency, the maximum switch voltage $V_{c,\mathrm{Max.}}$ normalized to V_{DD}, and the output voltage amplitude V_{out} normalized to that at nominal load conditions. All these can be derived as a function of k and k' as defined in (4), independent from P_{out} at nominal conditions, the frequency, and the nominal load value R. As a result, for any set of q, d, and m, we can now plot contours on a Smith chart with R as the reference impedance, showing the impact of load changes on the performance and behavior of class-E PAs.

For example, for a load-insensitive class-E PA with an ideal switch ($m = 0$), the load-pull contours are shown in Fig. 1(c) and (d) for a part of Smith chart. The normalized output power and the efficiency contours are shown in Fig. 1(c) with solid and dotted lines, respectively. Fig. 1(c) shows that for real loads (for impedances $\mathrm{Re}\{Z\} \geq R$), the efficiency is (ideally) 100% while the output power can be lowered. A non-zero imaginary part of the load will result in $\alpha \neq 0$ at switching moment and hence causes switching loss (because of discharging the non-zero capacitor voltage) which reduces the efficiency. $V_{c,\mathrm{Max.}}$ contours normalized to V_{DD} are shown in Fig. 1(d). For real loads ($\mathrm{Re}\{Z\} \geq R$) the $V_{c,\mathrm{Max.}}$ stays close to (but is lower than) that for the nominal load. Toward the upper side of the Smith chart, the $V_{c,\mathrm{Max.}}$ increases. Normalized output voltage amplitude across the load, shown in Fig. 1(d), shows a symmetrical behavior with respect to the real axis. These load-pull contours will be used in the next section to describe the behavior of OEPAs and to introduce our method to increase power efficiency in back-off.

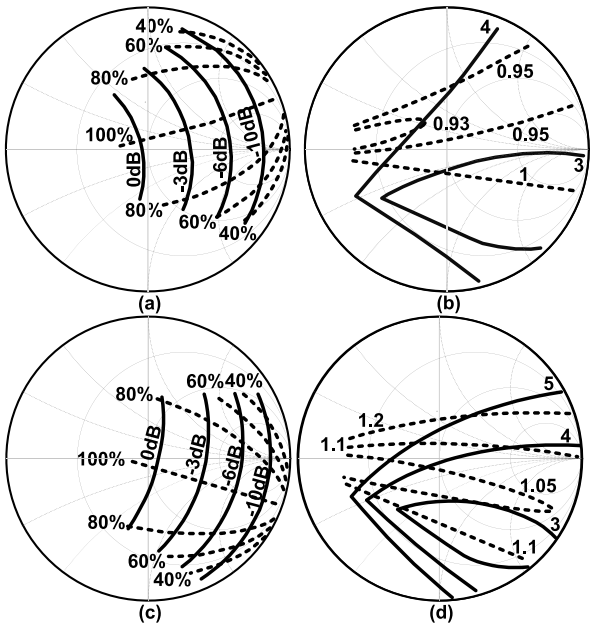

Fig. 2. Effect of changing q from 1.3 to 1.2 [(a) and (b)] and 1.4 [(c) and (d)] on the load-pull plots for $d = 1$ and $m = 0$, respectively. (a) and (c) Normalized output power (solid curve) and efficiency (dotted curve) contours. (b) and (d) $V_{c,\mathrm{Max.}}$ normalized to V_{DD} (solid curve) and normalized output voltage amplitude (dotted curve).

B. Effect of Changing q and d on the Load-Pull Contours

Parameters q and d have a major impact on the load-pull contours shown in Fig. 1. In this section, we assume that the class-E PA is initially designed for $q = 1.3$ and $d = 1$. Then we change the parameter q (by, e.g., changing the capacitor C) and/or change the parameter d and plot the resulting load-pull contours. Again, these contours are independent from P_{out}, ω_0, and the nominal load R.

The load-pull plots are shown in Fig. 2 for changing q from 1.3 to 1.2 (respectively, 1.4). The shape of the normalized output power, efficiency, and $V_{c,\mathrm{Max.}}$ contours hardly change except for a rotation: there is clockwise (anti-clockwise) rotation for higher (lower) q. The normalized output voltage contours, shown in Fig. 2(b) and (d), are rotated and changed in shape. Similar contours can be derived and plotted to

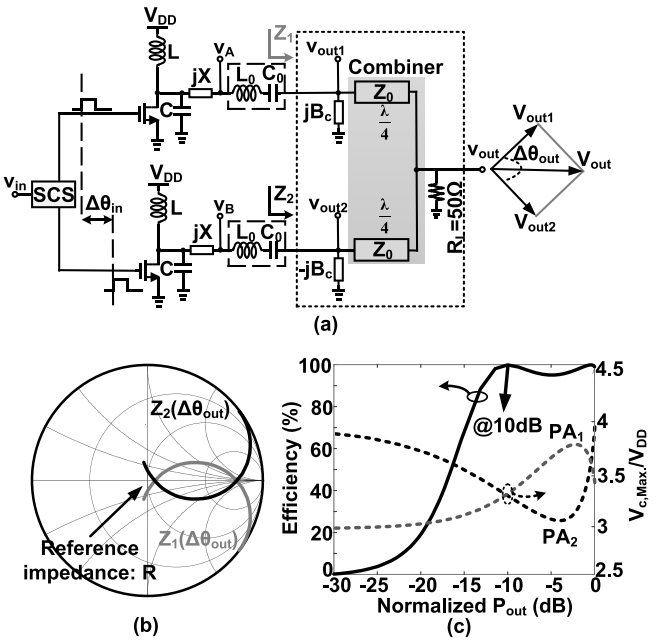

Fig. 3. (a) OEPA with transmission-line-based combiner. (b) $Z_{1,2}$ for $0 < \Delta\theta_{\text{out}} < \pi$ and compensation at outphasing angles $(\pi/5)$ and $\pi - (\pi/5)$. (c) Efficiency versus normalized output power (solid curve) and $V_{c,\text{Max.}}$ normalized to V_{DD} for PA1 (gray dotted curve) and PA2 (dark dotted curve).

show the effect of changing d; then clockwise (anti-clockwise) rotation occurs for lower (higher) d. These plots are shown in Appendix A.

III. Simplified Theory of OEPAs

An OEPA with a signal component separator (SCS), two class-E branch PAs, and a combiner is shown in Fig. 3(a). The SCS generates two driving waveforms with a phase difference of $\Delta\theta_{\text{in}}$ according to the input signal amplitude.

To be able to map the results of Section II, we assume that both class-E PAs, conventionally, are designed to have $q = 1.3$, $d = 1$, and $\alpha = \beta = 0$ for a load $Z_1 = Z_2 = R$. The combiner at the output sums the output voltages to reconstruct an amplified replica of the input signal. Two compensating elements, $\pm jB_c$, are used to compensate the imaginary part of the loads at two specific outphasing angles. In this paper, a transmission-line-based combiner is used.

Let us consider the part in the dotted box in Fig. 3(a) and assume voltages at the branch PAs' outputs as

$$v_{\text{out}_{1,2}}(t) = V_{\text{out}_{1,2}} \sin(\omega_0 t + \phi_{v_{1,2}}) \tag{5}$$

where $V_{\text{out}_{1,2}}$ and $\phi_{v_{1,2}}$ are the amplitudes and initial phases with respect to a reference time, respectively. The circuit is linear and can be solved in phasor domain which leads for the apparent load impedances of the two branch PAs to

$$\frac{1}{Z_1} = +jB_c + \frac{R_L}{Z_0^2}\left(1 + \frac{V_{\text{out},2}}{V_{\text{out},1}} e^{-j\Delta\theta_{\text{out}}}\right)$$
$$\frac{1}{Z_2} = -jB_c + \frac{R_L}{Z_0^2}\left(1 + \frac{V_{\text{out},1}}{V_{\text{out},2}} e^{+j\Delta\theta_{\text{out}}}\right) \tag{6}$$

where $\Delta\theta_{\text{out}} = \phi v_1 - \phi v_2$ is denoted as the outphasing angle. To simplify the analysis, let's assume $(V_{\text{out1}}/V_{\text{out2}}) = 1$. We will show the validity of this assumption later in this section. The $\Delta\theta_{\text{out}}$-dependent impedance seen by each PA, $Z_{1,2}$, then is

$$\frac{1}{Z_1} = \frac{2R_L}{Z_0^2}\cos^2\left(\frac{\Delta\theta_{\text{out}}}{2}\right) + j\left(-\frac{R_L}{Z_0^2}\sin(\Delta\theta_{\text{out}}) + B_c\right)$$
$$\frac{1}{Z_2} = \frac{2R_L}{Z_0^2}\cos^2\left(\frac{\Delta\theta_{\text{out}}}{2}\right) - j\left(-\frac{R_L}{Z_0^2}\sin(\Delta\theta_{\text{out}}) + B_c\right) \tag{7}$$

where we assume $Z_0 = \sqrt{2RR_L}$. For $B_c < (R_L/Z_0^2)$, there are two outphasing angles for which the imaginary part of the loads $Z_{1,2}$ is zero. $Z_{1,2}$ for a range $0 < \Delta\theta_{\text{out}} < \pi$ are shown in Fig. 3(b) on the Smith chart for $B_c = (1/2R\sin(\pi/5))$, assuming R as the reference impedance.

Having PA loads $Z_{1,2}$, shown in Fig. 3(b), on top of the load-pull contours of the normalized output voltage amplitude shown in Fig. 1(d), yields two important observations. Firstly, the output voltage of the branch PAs is not constant across different outphasing angles, and therefore, the PAs cannot be modeled as ideal voltage sources as was done in, e.g., [5] (although the same final results for $Z_{1,2}$ were obtained). Secondly, because of the symmetry of the PA loads $Z_{1,2}$ and of the normalized output voltages contours with respect to the real axis, for all outphasing angles, $(V_{\text{out},1}/V_{\text{out},2}) = 1$ which proves the validity of our assumption leading to (7).

To get the output power and the efficiency for an OEPA as a function of power back-off, the normalized power contours and the efficiency contours of Fig. 1(c) can be combined with the $\Delta\theta_{\text{out}}$-dependent load impedance for the two branch PAs of an OEPA, described in (7) and shown in Fig. 3(b). Then for each $\Delta\theta_{\text{out}}$, the output power and the efficiency of the branch class-E PAs follow. Due to symmetrical PA loads and contours with respect to the real axis, the output power and efficiency of both branch PAs are identical.

Combining the output power as a function of $\Delta\theta_{\text{out}}$ and the efficiency as a function of $\Delta\theta_{\text{out}}$ yields Fig. 3(c) that shows the efficiency of the OEPA plotted versus the (normalized) output power. The second compensation point is located at 10-dB back-off where the efficiency is (ideally) 100%. Similarly, the $V_{c,\text{Max.}}$ (normalized to V_{DD}) for the two branch PAs can also be derived as a function of the power back-off. Fig. 3(c) shows that the $V_{c,\text{Max.}}$ for PA2 increases at back-off. We will also address this issue in the measurement section. All plots of Fig. 3(c) are valid under the assumption of an ideal OEPA with an ideal combiner and assuming a very high loaded quality factor for the $L_0 - C_0$ filter.

A. Output Vectors' Amplitude Mismatch

In theory, the branch class-E PAs are identical and hence have 0% mismatch/error between the output voltage amplitudes $V_{\text{out},1,2}$. The normalized output power, shown in Fig. 3(c), is then 0 for $\Delta\theta_{\text{out}} = \pi$ which yields an infinite OPDR.

Any mismatch between the two paths in an outphasing system that causes amplitude errors between the two output vectors V_{out1} and V_{out2} reduces the OPDR. Using the vector diagram in Fig. 3(a) and assuming a relative amplitude error

ϵ between the two vectors, $V_{\text{out1}} = V$, and $V_{\text{out2}} = V(1+\epsilon)$, the maximum attainable OPDR can then be written as

$$\text{OPDR(dB)} = 20\log\left(\frac{\max(V_{\text{out}})}{\min(V_{\text{out}})}\right) = 20\log\left(1+\frac{2}{\epsilon}\right). \quad (8)$$

Using (8), to have an OPDR better than 60 dB [27], the amplitude error should be kept below 0.2% while mismatch less than 6.5% keeps the OPDR better than 30 dB [10].

One of the mechanisms that leads to amplitude error is the residual impedance of the series filter $L_0 - C_0$ due to, e.g., frequency deviations or components spread. For instance, the residual impedance at $\Delta\omega$ deviation from the center frequency $\omega_0 = (1/\sqrt{L_0C_0})$ can be written as

$$Z_r(\Delta\omega) = L_0(\omega_0+\Delta\omega)j - \frac{j}{C_0(\omega_0+\Delta\omega)} \approx 2L_0\Delta\omega j \quad (9)$$

For $\Delta\omega = 0$, $Z_r = 0$ and the filter passes the first harmonic of the signal without any error. However, non-zero Z_r causes a voltage division at the inputs of the combiner and hence creates error.

To find a simple quantitative model, consider the OEPA system, shown in Fig. 3(a) and assume that, for small $\Delta\omega$, the combiner, the q parameters, the compensation elements impedance, and the first harmonic of the signals at nodes A and B (before the filter) are not affected. Then we can assume identical first harmonics $V_A = V_B = V$ for nodes A and B for identical class-E branch PAs. For minimum output power, $\Delta\theta_{\text{out}} = \pi$, and therefore V_{out1} and V_{out2} can be written as

$$\begin{aligned} V_{\text{out1}}(\Delta\theta_{\text{out}}=\pi) &= \frac{Z_1V_A}{Z_1+Z_r} = \frac{V}{1-2L_0B_c\Delta\omega} \\ V_{\text{out2}}(\Delta\theta_{\text{out}}=\pi) &= \frac{Z_2V_B}{Z_2+Z_r} = \frac{V}{1+2L_0B_c\Delta\omega} \end{aligned} \quad (10)$$

where we replaced Z_1 and Z_2 from (7) for $\Delta\theta_{\text{out}} = \pi$ and Z_r from (9). Assuming the loaded Q of the filter as $Q_L = (L_0\omega_0/R)$ and locating the second compensation point at 10-dB back-off ($B_c = \sin(\pi/5)/2R$),

$$\frac{V_{\text{out1}}}{V_{\text{out2}}}(\Delta\theta_{\text{out}}=\pi) = \frac{1+Q_L\sin\left(\frac{\pi}{5}\right)\frac{\Delta\omega}{\omega_0}}{1-Q_L\sin\left(\frac{\pi}{5}\right)\frac{\Delta\omega}{\omega_0}}. \quad (11)$$

$Q_L = 5$, $(\Delta\omega/\omega_0) = +1\%$, and $(\Delta\omega/\omega_0) = +5\%$ yield $(V_{\text{out1}}/V_{\text{out2}})$ equal to 1.06 and 1.34, respectively. According to (8), and assuming that Z_r will not affect maximum P_{out}, these amplitude errors limit OPDR to 30 dB and 16 dB, respectively. Moreover, $(\Delta\omega/\omega_0) = -1\%$ and $(\Delta\omega/\omega_0) = -5\%$ results in $(V_{\text{out1}}/V_{\text{out2}})$ equal to 0.94 and 0.74, respectively, which limits OPDR to 31 and 19 dB, respectively.

IV. Back-Off Efficiency Improvement Technique

This section presents detailed discussions of the technique presented in [7] to improve the back-off efficiency of the OEPAs. The starting point is again a conventional OEPA with $q_1 = q_2 = 1.3$ and with the second compensation points located at 10-dB back-off.

A. Rotation

Adaptively changing the compensating elements $\pm jB$ in the OEPA or employing four-way outphasing system can improve the efficiency at more back-off levels. However, a more efficient way—both for efficiency and for integration—is to change the parameter q of both branch PAs. Fig. 2 shows that by increasing (decreasing) the parameter q, the power and efficiency contours rotate in the clockwise (anti-clockwise) direction.

Using Fig. 3(b), to shift the compensation point deeper into back-off, the contours for PA1 should rotate in the clockwise direction and simultaneously the contours for PA2 must rotate in the anti-clockwise direction. To accomplish this, for PA1, the q must be increased (e.g., from 1.3 to 1.4), and for PA2, it must be reduced (e.g., from 1.3 to 1.2).

To find the efficiency of the OEPA having different q for the two branch PAs, again the PA loads $Z_{1,2}$ need to be known. However, whereas in the previous section $V_{\text{out2}} = V_{\text{out1}}$ due to having the same q in both branch PAs, this condition is inherently violated now [see Fig. 2(b) and (d)]. Therefore, (7) cannot be used and the general equation (6) must be employed. For each outphasing angle $\Delta\theta_{\text{out}}$, we use a simple iterative method to find the PA loads; in it, we start at $V_{\text{out1}} = V_{\text{out2}}$ and estimate the loads from (6). For the calculated loads, we use the data in Fig. 2(b) and (d) to update the estimated $(V_{\text{out1}}/V_{\text{out2}})$ and to then recalculate the loads from (6). We terminated this iterative routine upon reaching a sufficiently low change in $(V_{\text{out1}}/V_{\text{out2}})$; typically lower than 1% error was reached within two or three iterations. The PA loads $Z_{1,2}$ and $(V_{\text{out1}}/V_{\text{out2}})$ for $q_1 = 1.4$ and $q_2 = 1.2$ are shown with dashed lines for $0 < \Delta\theta_{\text{out}} < \pi$ in Fig. 4(a) and (b). For comparison, the corresponding curves for a conventional OEPA ($q_1 = q_2 = 1.3$) are shown using solid curves.

After obtaining the PA loads $Z_{1,2}$ as a function of $\Delta\theta_{\text{out}}$, for specific q_1 and q_2, and using the load-pull contours in Fig. 2, the output power, efficiency, and the normalized $V_{c,\text{Max.}}$ can directly be obtained. These are shown in Fig. 4(c) and (d) with dashed lines.

Fig. 4(c) shows that the second compensation point is shifted from the initial 10-dB back-off (for $q_1 = q_2 = 1.3$) to almost 17 dB into back-off for $q_1 = 1.4$ and $q_2 = 1.2$; here the power efficiency is 100% [see Fig. 4(c)]. Fig. 4(a) shows the PA loads $Z_{1,2}$; the negative real part of Z_2 for $\Delta\theta_{\text{out}}$ close to π implies that PA2 absorbs part of the power provided by PA1. The extension of the load-pull contours, presented in Fig. 1(c) and (d) for positive loads, toward negative impedances is presented in Appendix B. Note that for the OEPA shown in Fig. 3(a), there is no risk for the stability as the loop gain, for the loop consists of the nodes $V_{\text{DD}} - v_A - v_{\text{out},1} - v_{\text{out}} - v_{\text{out},2} - v_B - V_{\text{DD}}$, is always less than unity due to the loss of the components, switch loss, and mainly due to the fact that $P_{\text{out}} >= 0$.

The (almost) 10% unbalance between the two branch PAs, visible in Fig. 4(b) for $q_1 = 1.4$ and $q_2 = 1.2$, limits the OPDR according to (8) to about 27 dB. Shifting the second compensation point more into back-off with extra rotation will limit the OPDR more. The unbalance due to rotation,

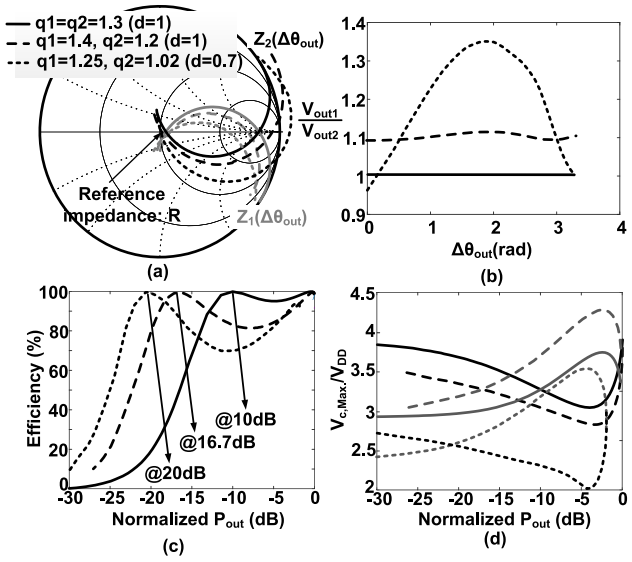

Fig. 4. Ideal OEPA results for $0 < \Delta\theta_{\text{out}} < \pi$ for conventional design with $q_1 = q_2 = 1.3$ (solid curve), for rotation with $q_1 = 1.4$ and $q_2 = 1.2$ (dashed curve), and for shift-rotation with $d = 0.7$, $q_1 = 1.25$, and $q_2 = 1.02$ (dotted curve). (a) PA loads Z_1 (gray curve) and Z_2 (dark curve). (b) $(V_{\text{out1}}/V_{\text{out2}})$ versus $\Delta\theta_{\text{out}}$. (c) Efficiency versus normalized output power. (d) $V_{c,\text{Max.}}$ normalized to V_{DD} for PA1 (gray curve) and PA2 (dark curve).

however, can be used to compensate the amplitude error due to, e.g., frequency deviations, discussed in Section III-A. For negative frequency deviations where $(V_{\text{out1}}/V_{\text{out2}})$ goes below one, the rotation according to Fig. 4 can be employed to increase the amplitude ratio toward unity and to improve the OPDR. For positive frequency deviations, where $(V_{\text{out1}}/V_{\text{out2}})$ increases above unity, rotation in reverse direction by reducing q_1 or/and increasing q_2 should be employed to reduce the amplitude ratio. In this case, however, the back-off efficiency will reduce compared with the conventional design having $q_1 = q_2 = 1.3$. The next section extends the shift technique with the rotation to compensate for this efficiency drop.

Fig. 4(d) shows the $V_{c,\text{Max.}}$ versus the normalized output power (back-off), illustrating that the $V_{c,\text{Max.}}$ in back-off can be reduced with shifting the second compensation point further into back-off.

B. Shift

Reducing the parameters d and q for both branch PAs results in rotation in the opposite directions. Therefore, for a lower d (e.g., 0.7), a lower q (e.g., 1.1) can be found to have almost the same efficiency contours for the branch PAs at a lower output power level. This corresponds to a shift of power contours to the left on Smith chart for almost the same efficiency contours. As a result, the output power at the second compensation point can be lowered while the efficiency is 100%: the second compensation point can be shifted to a lower output power level.

This technique can be combined with the rotation technique to shift the second compensation point more into back-off. For this, the d values for both branch PAs are reduced to 0.7 for $q_1 = q_2 = 1.1$ to shift the power contours. Subsequently, q_1 is increased to 1.25 and q_2 is reduced to 1.02 to rotate both the power and the efficiency contours. Following the same procedure as in the previous section, the load-pull contours can be plotted and a simple iterative procedure can be used to find $(V_{\text{out1}}/V_{\text{out2}})$ for each $\Delta\theta_{\text{out}}$ which results in the PA loads $Z_{1,2}$. For length reasons, the load-pull contours are not shown here but the effect of the shift-rotation technique on the OEPA performance and behavior is shown in Fig. 4 with dotted lines. Fig. 4(b) shows that the output voltage amplitude error first increases with $\Delta\theta_{\text{out}}$, and again reduces when $\Delta\theta_{\text{out}}$ approaches π, which therefore helps to improve the efficiency without sacrificing the OPDR.

Fig. 4(c) shows that the second compensation point is now shifted to almost 20 dB into back-off with lower switch voltage stress deep in back-off. However, by fine tuning of the parameters d, q_1, and q_2, the second compensation point can be easily shifted to any arbitrary back-off level between 10 and 20 dB. Furthermore, shifting the power contours can lower the maximum output power. For maximum output power and to benefit from the high back-off efficiency that the presented shift-rotation technique brings to the OEPA, one can tune the parameters d and q dynamically according to the required instantaneous output power.

V. Second-Order Effects

A. Switch Conduction Loss

In the previous sections, the switch was assumed to be ideal ($m = 0$). However, being implemented by transistors, the switch-on resistance R_{ON} is non-zero which causes conduction loss for the time period during which the switch is closed. For a non-zero m, the output power and efficiency contours in Fig. 5(a) for a single class-E PA with $q = 1.3$ and $d = 1$ follow for a switch-on resistances with $m = 0.05$.[1]

Compared with the ideal load-pull contours shown in Fig. 1(c), the elliptical shape of the efficiency contours is noticeable and, for real loads, the efficiencies between 3 and 6 dB back-offs are higher (>85%) than the efficiency at peak output power (<80%). Moreover, the elliptical shape of the efficiency contours seriously impacts the improvement that the rotation technique of Section IV brings to the OEPAs.

Fig. 5(b) shows the effect of reducing q and d on the power and efficiency contours; not only the power contours are shifted to the left, but that also the efficiency at back-off is improved. At, e.g., the cross sections of the -10 dB contours and the real axis in Fig. 5(a) and (b), the efficiency is improved from almost 70% to 90%. To benefit from these improved efficiency contours at back-off, the rotation technique can now be employed to optimally place the contours on the Smith chart for the actual load at back-off.

To demonstrate the effect of the shift-rotation technique in the case of lossy switch with $m = 0.05$, we follow the same procedure as Section IV and derive the efficiency and the output power, yielding the plots in Fig. 5(c) and (d) for $B_c = \sin(\pi/5)/2R$ (corresponding to compensation at 10- dB

[1]It is shown that m depends only on the technology and the operation frequency [25]. For this paper, at the frequency of interest (1.8 GHz) for a cascode switch in 65-nm CMOS technology, $m = 0.05$ shows a fair agreement between theory and simulation results.

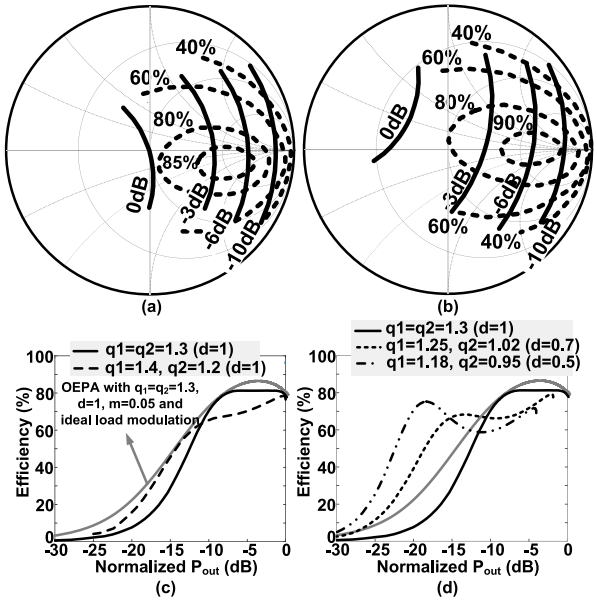

Fig. 5. Output power (solid) and the efficiency (dotted) contours for a single class-E PA with (a) $q = 1.3$, $d = 1$, and $m = 0.05$. (b) q and d are reduced to 1.1 and 0.7, respectively. (c) and (d) Efficiency versus normalized output power for an OEPA with $m = 0.05$ for the class-E branch PAs and with conventional design and compensation at 10-dB back-off (solid dark curve), with an ideal load modulation with zero imaginary part (gray solid curve), with the rotation (dark dashed curve), with the shift-rotation with setting Sett. 1 (dark dotted curve), and the shift-rotation with setting Sett. 2 (dark dashed-dotted curve).

back-off for $m = 0$).[2] The results for the conventional OEPA design ($q_1 = q_2 = 1.3$ and $d = 1$) are shown with solid dark lines. For comparison, the efficiency of an OEPA with $q_1 = q_2 = 1.3$, $d = 1$, and $m = 0.05$ with (ideal) real load modulation (zero imaginary part) is also shown in Fig. 5(c) and (d) with a solid gray curve. For this, the efficiency and the output power are obtained from Fig. 5(a) for real loads in the range of $[R, \infty]$. This curve also corresponds to the maximum reachable efficiency for techniques that rely on reducing the imaginary part of loads for the branch PAs at back-off to improve the back-off efficiency, e.g., the adaptive Chireix compensation elements technique [13] or four-way OEPA systems [14].

Fig. 5(c) shows that compensation at 10-dB back-off for a conventional OEPA, with $q_1 = q_2 = 1.3$, $d = 1$, having a lossy switch can achieve the maximum reachable efficiency (80% for $m = 0.05$) at full power and near 10-dB back-off. Fig. 5(c) also shows that the rotation technique can improve the efficiency at more than 15-dB back-off. Comparing Figs. 4(c) and 5(c) also clearly shows that the switch conduction loss seriously impacts the improvement of our proposed rotation technique as well as achieved by the adaptive tuning (or four-way OEPA). On top of that, also additional losses of the tuning elements or due to extra components at the output can compromise this improvement. This last issue is also addressed in Section VII.

[2]Non-zero m ($m = 0.05$) slightly changes the power contours. It can be shown that for $m = 0.05$, $B_c = \sin(\pi/5)/2R$ corresponds to the compensation of the imaginary parts of the loads at (almost) 9-dB back-off. But in this paper, for simplicity, we ignore this small difference.

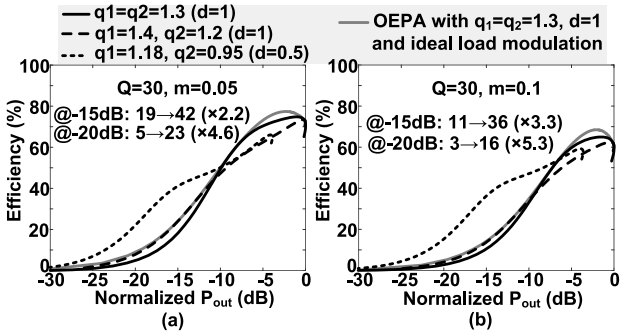

Fig. 6. Efficiency versus normalized output power for a conventional OEPA with $q_1 = q_2 = 1.3$ and compensation at 10-dB back-off (dark solid curve), with an ideal load modulation (gray solid cuve), the rotation (dark dashed curve), and the shift-rotation with setting Sett. 2 (dark dotted curve). (a) $m = 0.05$. (b) $m = 0.1$.

Fig. 5(d) shows the effect of shift-rotation technique on the efficiency for two different settings Sett.1: $\{q_1, q_2, d\} = \{1.25, 1.02, 0.7\}$ and Sett.2: $\{q_1, q_2, d\} = \{1.18, 0.95, 0.5\}$ with dotted and dashed-dotted curves, respectively. The shift-rotation technique can significantly increase the efficiency in back-off, e.g., the efficiency is improved from less than 10% to more than 75% at 20-dB back-off (more than $\times 7.5$ improvement).

B. Limited Quality Factor of the DC-Feed Inductor L

Another important loss mechanism is due to the limited quality factor (Q) of the dc-feed inductor L, shown in Fig. 3(a). This inductor can be a separate component [7] or it can be a part of the transformer-based combiner [5], [27]. To study this effect, one can derive a new set of load-pull equations using Q as a parameter. This derivation is not given here for simplicity and length reasons.

The resulting efficiency versus power curves for $m = 0.05$ and $m = 0.1$ and for quality factor value $Q = 30$ are shown in Fig. 6 for the conventional OEPA design (solid curve) with compensation at 10-dB back-off, using the rotation technique (dashed curve), and for the shift-rotation with setting Sett.2 (dotted curve). For comparison, both graphs in Fig. 6 include a gray solid curve that corresponds to the maximum efficiency of an OEPA with conventional design and ideal real load modulation, for the specific Q and m listed for each graph. Again, these curves represent the upper efficiency limit for any technique that optimizes efficiency by reducing the imaginary part of loads for the branch PAs at back-off [13], [14].

For the both cases, employing only the rotation technique can improve the efficiency to the maximum reachable efficiency (gray curve) at back-offs up to around 20 dB. However, the improvement with respect to a conventional OEPA (black solid curve) almost vanishes for high m or low Q. This is due to compression of the elliptical efficiency contours. However, the rotation technique can be used both to reduce the switch voltage stress at back-off and to improve the OPDR.

The proposed shift-rotation technique, however, improves the efficiency at back-off to levels significantly higher than the maximum reachable efficiency with real load modulation.

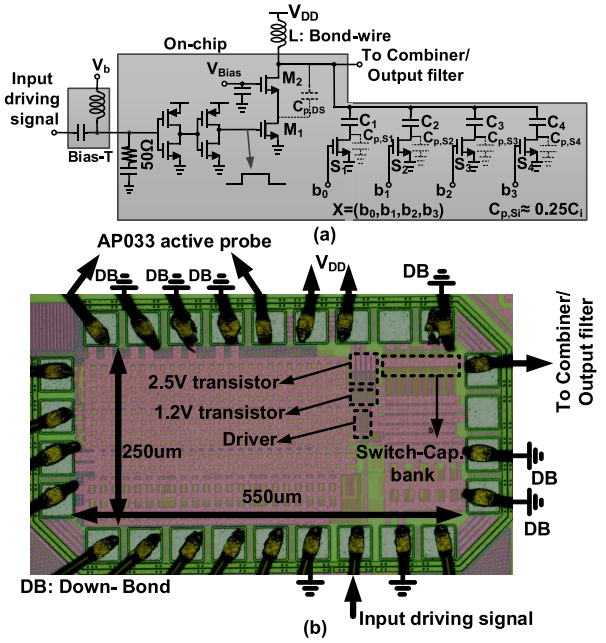

Fig. 7. Branch class-E PAs. (a) Schematic. (b) Chip microphotograph.

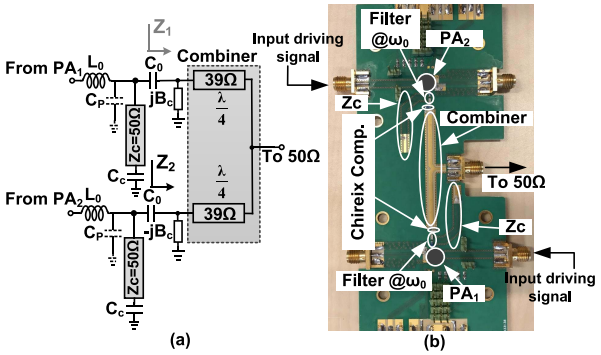

Fig. 8. (a) Detailed schematic of the combiner. (b) Designed PCB.

Also, the improvement ratio increases with increasing switch conduction loss for a constant Q (the absolute efficiencies are lower though). For instance, at 20-dB back-off, more than $\times 4.6$ and $\times 5.3$ higher efficiencies with respect to the conventional design are obtained for, respectively, $m = 0.05$ and 0.1. It can be concluded that this shift-rotation technique is quite promising to improve the efficiency of an OEPA with an integrated combiner at high frequencies, e.g., [27], where the switch conduction is the dominant loss mechanism.

VI. Implementation in 65-nm CMOS Technology

The schematic of a single class-E branch PA and its driver stage is shown in Fig. 7(a). Note that this system serves to demonstrate the performance increase of our shift-rotation technique, and does not aim at a specific transmit standard or application. The switch is implemented by a cascode structure employing a 1.2-V thin-oxide transistor ($W/L = 0.84$ mm/60 nm) as switch transistor and a thick-oxide 2.5-V transistor ($W/L = 1.65$ mm/280 nm) as cascode device. The cascode structure allows $V_{c,\text{Max.}}$ up to 4 V for reliability reasons.

Using the K-design set elements for $q = 1.3$, $d = 1$, $m \approx 0.05$, and $\alpha = \beta = 0$ and for $R = 15\ \Omega$, $\omega_0 = 2\pi 1.8$ GHz, yields $L = 1.4$ nH, $C = 3.3$ pF, and $X = 0.5$ nH. The dc-feed inductor L is implemented by two parallel bond-wire inductances to provide a relatively high quality factor $Q(\approx 25)$. The tank capacitor C at the switching node was implemented with the drain-bulk and gate-drain parasitic capacitance of the cascode transistor. Moreover, the drain and the source of the cascode transistor were laid out close to each other to introduce some parasitic capacitance $C_{P,\text{DS}}$ to achieve slightly better efficiency [28]. Two cascaded inverters were used as the driver for the switch where the duty cycle can be controlled by the off-chip control voltage V_b.

Two switched capacitor banks with four control bits X1 and X2 were used at the switching nodes to tune the q parameter of the branch PAs independently. Circuit simulations in 65-nm CMOS technology suggest that a total switchable capacitance of 1.5 pF is more than sufficient to employ the shift-rotation technique with shifting the contours up to 5 dB. This 1.5-pF capacitor is divided into four sections with $C_1 = 150$ fF, $C_2 = 300$ fF, $C_3 = 450$ fF, and $C_4 = 600$ fF, shown in Fig. 7(a), being controlled with four control switches S_i, $i \in \{0, 1, 2, 3\}$.

When each switch S_i is OFF, it needs to tolerate the maximum voltage at the switching node which can be up to 4 V. The switches S_i are implemented by 2.5-V thick-oxide transistors. There is a parasitic capacitance C_{p,S_i} associated with the switch S_i, shown in Fig. 7(a). The switches S_i are sized to have $C_{p,S_i} \approx (1/4)C_i$ to make sure the maximum voltage across the switches S_i does not exceed (almost) 3 V. This switch-capacitor network at the switching node introduces extra capacitive loading at this node when all control bits are zero, which amounts to 0.3 pF or 10% of the total drain capacitance. To compensate for this extra capacitance, the switch size was reduced by 10%. This increases m by 10% which impacts the (simulated) efficiency at maximum output power and at the back-off by less than 3%.

To have the high and low level of the voltages at the driver output well defined, the driver and the main switch share the same ground, and to reduce the bond-wire inductance at ground, six parallel down-bonds with minimum length were used [shown in Fig. 7(b)]. The switches S_i are controlled quasi-statically, driven from off-chip sources; no dynamic tuning is provided for this paper. The microphotograph of the implemented branch class-E PA is shown in Fig. 7(b).

The detailed implementation of the off-chip transmission-line-based combiner and the output series filters $L_0 - C_0$ are shown in Fig. 8(a). The combiner is implemented on I-Tera MT RF substrate with a dielectric constant 3.45 and 0.5-mm thickness. The characteristic impedance Z_0 is obtained for $R = 15\ \Omega$ and $R_L = 50\ \Omega$ as $Z_0 = \sqrt{2RR_L} \approx 39\ \Omega$. The total series inductance at the branch class-E PAs' outputs $(X + L_0)$ is implemented partly by the bond-wire inductance and partly by an off-chip component. The loaded quality factor of the output filter for $R = 15\ \Omega$ is roughly 5. Due to the small thickness of the substrate and the relatively

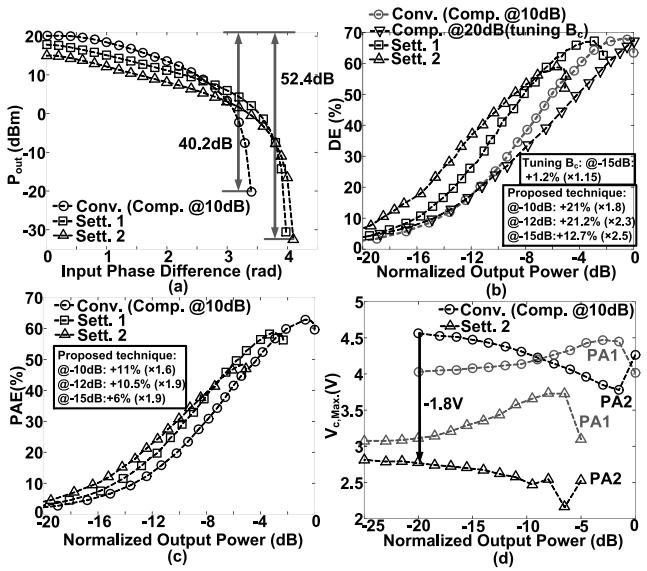

Fig. 9. (a) Measured P_{out} versus $\Delta\theta_{\text{in}}$ for compensation at 10-dB back-off and three different settings; conventional with $V_b = 0.6$ V, $X_1 = 0000$, and $X_2 = 0000$ (corresponding to $\{q_1, q_2, d\} \approx \{1.3, 1.3, 1\}$), Sett.1 with $V_b = 0.43$ V, $X_1 = 0011$, and $X_2 = 1010$ (corresponding to $\{q_1, q_2, d\} \approx \{1.25, 1.02, 0.7\}$), and Sett.2 with $V_b = 0.36$ V, $X_1 = 0000$, and $X_2 = 1111$ (corresponding to $\{q_1, q_2, d\} \approx \{1.18, 0.95, 0.5\}$). (b) Measured DE for conventional compensation at 10-dB back-off, Sett. 1 and 2 and for conventional setting and compensation at 20 dB back-off (by tuning B_c). (c) Measured PAE for compensation at 10-dB back-off and three different settings. (d) Measured $V_{c,\text{Max.}}$ for compensation at 10-dB back-off and two different settings.

high loaded quality factor of the series filter, the parasitic capacitance C_p becomes notable and changes the impedance level and impedance behavior $Z_{1,2}$ with $\Delta\theta_{\text{out}}$. To reduce this effect, a parallel quarter-wavelength transmission-line terminated with a capacitor $C_c = (1/C_p\omega^2 Z_c^2)$ was used. The final designed PCB is shown in Fig. 8(b) with the mounted branch class-E PAs.

VII. Measurement Results

Measured P_{out} versus $\Delta\theta_{\text{in}}$ for three different conditions is shown in Fig. 9(a) for compensation of the imaginary part of the PA loads at 10-dB back-off. +20.1 dBm maximum output power ($P_{\text{out,Max.}}$) is achieved for the conventional design from 1.25-V supply voltage at 1.8 GHz while the mismatch between the branches limits OPDR to 40.2 dB. Changing the PA settings to Sett. 1 shifts the power contours by almost −2.3 dB and rotates them which result in better than 50-dB OPDR. Reducing duty cycles (setting 2) results in almost −5.15 dB shift in power contours and in an OPDR improvement to more than 52 dB. The improvement in the OPDR is (mainly) due to tuning the voltage ratio ($V_{\text{out1}}/V_{\text{out2}}$) to cancel out the amplitude mismatch between the two branches, discussed in Section III-A.

Fig. 9(b) shows the drain efficiency (DE) versus power back-off for four different conditions. Compensation at 20-dB back-off (dark-triangle (down)), by tuning B_c, with respect to compensation at 10 dB (gray circle), brings less than ×1.15 improvement at 15-dB back-off at the cost of reducing the efficiency at higher power levels. Employing adaptive elements [13] or using more components at the output to implement a four-way system [14] will limit the improvement even more. However, as shown in Fig. 9(b) and (c), the presented shift-rotation technique can effectively improve the DE and PAE.

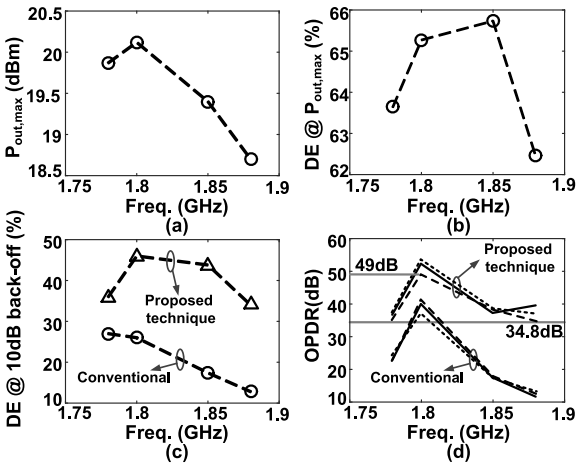

Fig. 10. (a) Measured maximum P_{out}, (b) DE at maximum P_{out}, (c) DE at 10-dB back-off, and (d) OPDR (for three different PA realizations, each with two (unselected) class-E PA ICs) versus frequency for conventional design with $V_b = 0.6$ V, $X_1 = 0000$, and $X_2 = 0000$ and for the proposed technique with $V_b = 0.43$ V, $X_1 = 0000$, and $X_2 = 1111$ at 1.78 GHz, with $V_b = 0.36$ V, $X_1 = 0000$, and $X_2 = 1111$ at 1.8 GHz, with $V_b = 0.36$ V, $X_1 = 0000$, and $X_2 = 1000$ at 1.85 GHz, and with $V_b = 0.36$ V, $X_1 = 0000$, and $X_2 = 0000$ at 1.88 GHz.

Fig. 9(b) shows that measured DE at $P_{\text{out,Max.}}$ for the conventional setting and compensation at 10-dB back-off is 65.3% and maximum DE is 68% at 1-dB back-off. PAE at $P_{\text{out,Max.}}$, shown in Fig. 9(c), is 60.7%. By our proposed shift-rotation technique, ×2.5 better DE and almost ×2 better PAE at 15-dB back-off were achieved. PAE at 0-dBm output power (20-dB back-off) is also improved from 2% to more than 4%. Therefore, to transmit 1-mW power, the presented technique reduces supply power from 50 to less than 25 mW.

Measured $V_{c,\text{Max.}}$ for both PAs at 1.8 GHz for compensation at 10-dB back-off are shown in Fig. 9(d). For this, the transient waveforms were measured against the power back-off using an AP033 active probe and an 80-GSa/s Agilent oscilloscope. Maximum voltage, for the conventional configuration at maximum P_{out} and for both switches, is almost 4 V. For PA2, however, it increases to more than 4.5 V at 20-dB back-off which can cause reliability issues. Fig. 9(d) shows that our proposed shift-rotation technique can significantly reduce the $V_{c,\text{Max.}}$ in power back-off; −1.8 V reduction was measured for PA2 at 20-dB back-off which reduces transistor degradation and hence improves the PA life time.

We also measured the system performance across a frequency range from 1.78 to 1.88 GHz (see Fig. 10). The maximum P_{out} at conventional setting is higher than 18.7 dBm with more than 62% DE. Increasing the frequency from 1.8 to 1.88 GHz results in 1.4-dB reduction in the maximum output power. Increasing the frequency, for both the branch class-E PAs, the parameter q reduces which rotates and slightly shifts the power contours to the left [shown in Fig. 2(a)]. Also, the positive residual impedance of the series filter at higher frequencies rotates the PA loads toward the right-hand

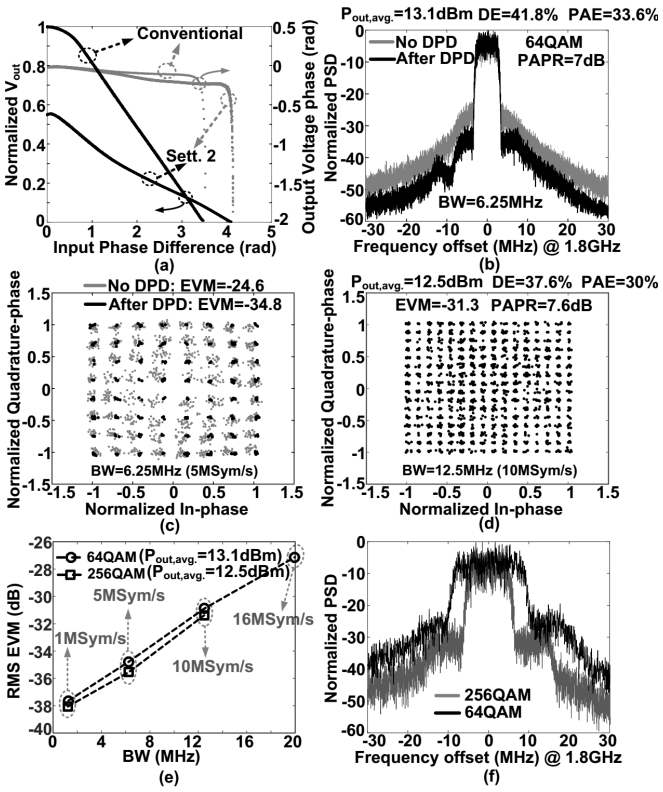

Fig. 11. (a) Measured output voltage (V_{out}) amplitude (dark curve) and phase (gray curve) versus input phase difference for two different settings at 1.8 GHz. The effect of DPD on (b) PSD and (c) symbol constellation for the conventional setting and for a 64QAM signal. (d) Measured symbol constellation (after DPD) for the conventional setting and for a 1.8-GHz 256QAM. (e) EVM versus modulation BW for the conventional setting. (f) Measured PSD for the 256QAM and 64QAM modulations with 12.5- and 20-MHz modulation bandwidths, respectively.

side of the Smith chart which further reduces the maximum output power. And finally, our transmission-line-based power combiner is a narrow-band combiner which further impacts the maximum output power by deviating from the center frequency [35].

The DE for conventional setting at 10-dB back-off shown in Fig. 10(c) reduces with increasing frequency due to the rotation of both efficiency contours in the same direction (counter-clockwise due to reduced q). However, the proposed technique improves the 10-dB back-off efficiency to more than 34%.

Executing the measurements with different samples, (almost) the same numbers for the maximum output power and efficiency at maximum output power and at 10-dB back-off were obtained. However, the OPDR is sensitive to the mismatch between the two samples. Fig. 10(d) shows the OPDR for three different PA realizations, each of these using their own set of (unselected) class-E PA ICs from the same batch. The OPDR for conventional design at center frequency (1.8 GHz) is more than 37 dB and it reduces sharply with deviating the frequency from 1.8 GHz. The OPDR reduces to almost 11 dB (solid curve) at 1.88 GHz (4.45% deviation from 1.8 GHz). This is mainly due to the residual impedance of the filter at frequencies different from the ω_0, discussed in Section III-A. The presented technique, however, improves

TABLE I

MEASURED EFFICIENCY (AFTER DPD) FOR 7.6-dB PAPR 256QAM MODULATION WITH 6.25 MHz (5 MSym/s) AND 12.5 MHz BW (10 MSym/s) AND DIFFERENT AVERAGE P_{out}

$P_{\text{out,avg.}}$	DE (%)		PAE (%)		EVM (dB)			
					6.25MHz		12.5MHz	
	Con.	Set.2	Con.	Set.2	Con.	Set.2	Con.	Set.2
12.5dBm	37.6	–	30	–	-35.6	–	-31.3	–
7.5dBm	14.8	29	11.3	17.9	-33.4	-36.1	-30.3	-31.5
2.5dBm	4.2	10.1	3.7	6.3	-32.1	-35.9	-30.1	-31.2

the OPDR to more than 49 dB at 1.8 GHz and to more than 34.8 dB across 100-MHz bandwidth. As discussed in Section IV-A, toward higher frequencies, we rotate the contours of PA2 in reverse direction by increasing q_2. For this, X_2 is reduced from 1111 at 1.8 GHz to 0000 at 1.88 GHz for the same V_b. Toward lower frequencies, however, we need to rotate the contours more, in the same direction that we rotate at 1.8 GHz. This is done by slightly increasing d.

The designed OEPA was also characterized using single carrier 1.8-GHz amplitude-modulated signals. For this, first, the output voltage amplitude [V_{out} in Fig. 3(a)] and phase are measured versus $\Delta\theta_{\text{in}}$ for two different settings, shown in Fig. 11(a) to implement a memory-less digital predistortion (DPD).

The output power spectral density (PSD) and symbol constellation for a single carrier 7-dB PAPR 64QAM signal with 5-MSym/s symbol rate are shown in Fig. 11(b) and (c) for two cases, without DPD and using a memory-less DPD. For this, the polar representations (the normalized envelope and the angle) of the time domain base-band IQ signals were generated in MATLAB. Then, we constructed two carrier signals (at 1.8 GHz) where the phase difference between the two carries was obtained from inverse cosine of the envelope (non-DPD case) and for the DPD, the inverse of plots shown in Fig. 11(a) (in dark). The common mode phase of the carriers is equal to the angle of the IQ signal (no-DPD). However, for the DPD, the output voltage phases, shown in Fig. 11(a) (in gray), were derived from the common mode phase of the carriers. The two carrier signals were then uploaded to a 12-GS/s M9502A Agilent arbitrary waveform generator with two output channels to drive the two class-E branch PAs. Fig. 11(c) shows that, for the conventional design, DPD improves the RMS error vector magnitude (EVM) from -24.6 to -34.8 dB with 13.1-dBm average P_{out} ($P_{\text{out,avg.}}$), 41.8% DE, and 33.6% PAE. The measured symbol constellation (using DPD) for a single carrier 7.6-dB PAPR 256QAM signal with 10-MSym/s symbol rate and for the conventional setting is also shown in Fig. 11(d). $+12.5$ dBm average output power with 37.6% DE and 30% PAE was measured at -31.3 dB RMS EVM level. Dynamic tuning of parameters d and q was not implemented in this paper. However, if dynamic tuning would be used to tune the parameters d and q according to the instantaneous output power level, it can be estimated that the PA then could provide about 48%[3] DE for 7.6-dB PAPR 256QAM signals.

[3]The average efficiency was estimated from the integral $\int_{-\infty}^{0} \text{pdf(BF)}.\max(\text{DE(BF)})\text{d(BF)}$ where pdf(BF) is the probability density function of back-off level BF for a modulated signal and max(DE(BF)) is the maximum achievable efficiency at back-off level BF for the three different settings shown in Fig. 9(b).

TABLE II
PERFORMANCE COMPARISON

	[11]	[12]	[27]	[29]	[30]		[31]	[32]	[33]	**This Work**	
CMOS Technology	0.13(um)	65(nm)	40(nm)	45(nm)	65(nm)		40(nm)	65(nm)	90(nm)	**65(nm)**	
Topology	OEPA	OEPA	OEPA	ODPA(e)	Class-G+DLTM(f)		Doherty	Polar	OBPA(j)	**OEPA**	
Combiner	On-chip	Off-chip	On-chip	Off-chip	On-chip		On-chip	On-chip	Off-chip	**Off-chip**	
Frequency (GHz)	1.85	2.4	5.9	0.9-2.4	2.4		1.9	2.4	0.9	**1.8**	
Supply (V)	2.8	2.5-0.85(a)	1.2	1.2	2.8-1.55(g)		1.5	1.2	2.5	**1.25**	
$P_{out,Max}$ (dBm)	29.7	27.7	22.2	25-25	24.6		28	22.8	20	**20.1**	
DE at $P_{out,Max}$	39.8	NR(b)	49.2	60-52	39		NR	46	NR	**65.3**	
PAE at $P_{out,Max}$	36.9	45	34.9	55-45	NR		34	NR	56	**60.7**	
DE/PAE at 12dB back-off (%)	NR /≈5(c)	NR /<22(c)	<18(d) <13	20/14-12/8(c)	21.8 /NR		NR /19.7	NR /NR	NR /<20	**37.2 /22.1**	
Signal	LTE	OFDM	64QAM	LTE	64QAM	256QAM	16QAM	64QAM	WCDMA	**64QAM**	**256QAM**
(PAPR(dB))	(7.5)	(7.5)	(7.2)	(6)	(7)	(7.3)	(8.36)	(6.5)	NR	**(7)**	**(7.6)**
BW (MHz)	10	20	20	10-10	NR(h)	NR(i)	20	20	5	**12.5/20**	**6.25/12.5**
Fractional BW (%)	0.54	0.83	0.34	1.11-0.42	NR	NR	1.05	0.83	0.55	**0.7/1.11**	**0.35/0.7**
$P_{out,avg.}$(dBm)	24.7	20.2	16.4	18.9	17.6	17.3	23.4	16.8	13	**13.1**	**12.5**
DE at $P_{out,avg.}$	NR	31.9	23.3	NR-NR	27.5	26.7	NR	24.5	NR	**41.8**	**37.6**
PAE at $P_{out,avg.}$	20.8	27.6	16.1	32-22	NR	NR	23.3	19.3	30	**33.6**	**30**
RMS EVM(dB)	-30.5	-31.3	-30	NR	-25.6	-30.4	-23	-28	-16.6	**-30.9/-27.1**	**-35.6/-31.3**
$\frac{V_{cmax}}{V_{DD}}$ at $P_{out,Max}$ / 15dB back-off	NR /NR	NR /NR	NR /NR	NR /NR	NR /NR		NR /NR	NR /NR	NR /NR	**<3.3 /<2.6**	

(a) Multi-level supply, (b) Not Reported, (c) obtained from publication figures, (d) DE=18% and PAE=13% at 9dB back-off, obtained from publication figures, (e) Outphasing class-D PA, (f) Dynamic Load Trajectory Manipulation, (g) full and half V_{DD} mode, (h) 20MSym/s reported symbol rate, (i) 10MSym/s reported symbol rate, (j) Outphasing class-B PA

Measured EVM as a function of the modulation bandwidth is shown in Fig. 11(e) for both 64QAM and 256QAM modulations at a constant average output power. The EVM increases with increasing bandwidth (signal symbol rate). The limited bandwidth of the OEPAs is both due to 10∼15x bandwidth expansion that comes with the non-linear SCS operation in outphasing mode [34] and due to the limited bandwidth of the output series filter and the combiner. The ways to improve the modulation bandwidth include a lower loaded quality factor for the output filters and using transformer-based combiners [35]. The output PSDs for the 256QAM and 64QAM amplitude modulations with 12.5-MHz (respectively, 20-MHz) modulation bandwidths are shown in Fig. 11(f).

Finally, we measured the OEPA performance with 256QAM modulated signals with different $P_{\text{out,avg.}}$ to demonstrate the effect of the proposed technique in the efficiency improvement of the OEPA at back-off. A summary of the measured DEs and PAEs is given in Table I. At 5-dB back-off ($P_{\text{out,avg.}} =$ 7.5 dBm), the DE and PAs are improved from 14.8% and 11.3% for the conventional design to 29% (× 1.96) and 17.9% (× 1.6) at a better EVM level. At 10-dB back-off ($P_{\text{out,avg.}} =$ 2.5 dBm), DE and PAE are improved by × 2.4 and × 1.7 with better RMS EVM.

In Table II, the measured results at 1.8 GHz are benchmarked against the other CMOS PAs. The designed PA at conventional settings provides the best DE and PAE for single tone excitation at maximum output power. Furthermore, the presented technique improves the DE at 12-dB back-off to more than 1.7 times better than other published works with a comparable PAE. The presented demonstrator PA has 20.1-dBm maximum output power which is lower than some other reported works. However, the outphasing theory and the back-off efficiency improvement approach described in this paper are not limited to a specific frequency or power level or technology: on purpose we (re)normalize voltages, power levels, and impedances and use Smith chart representations to be as independent from frequency, power, and technology as possible. Scaling our PA to achieve higher than 20.1-dBm maximum output power levels in first order (ideally) has no impact on DE and PAE numbers [36].[4] Section V-B already discussed the impact of the operating frequency on the merits of the efficiency enhancement technique.

All the measured efficiency numbers include the loss of the dc-feed inductor L (with $Q = 25$), output bond-wire inductance loss (1 nH with $Q = 15$), the loss of the off-chip inductor L_0 (which has a series resistance 0.5 Ω), and the combiner loss (0.3 dB). Therefore, replacing the PCB-based combiner with an on-chip transformer-based counterpart will not considerably affect the efficiency [38]. Due to the lack of relevant data in the literature, we cannot benchmark the effect of the presented technique on $V_{c,\text{Max.}}$ against the other efficiency improvement techniques.

VIII. CONCLUSION

A simple analysis of the OEPAs based on the load-pull analyses of the class-E PAs was given. The results of the study, then, further were used to rotate and shift the power contours and to rotate the efficiency contours to improve OEPAs performance and reliability aspects. Measurements in 65-nm CMOS technology showed more than ×2 DE improvement at deep back-off for single tone excitation at 1.8 GHz as well as for 7.6-dB PAPR 12.5-MHz 256QAM signals.

Class-E PAs (and the outphasing systems that employ class-E PAs as the branch amplifiers) are tuned amplifiers and hence are optimized for narrow-band applications. However, measurement results across a wide frequency range

[4]The matching network should also be adapted with the scaling; if a matching network with a higher quality factor were to be used to get higher output power (from a low-voltage PA), the Bode–Fano theorem [37] shows a limitation of the bandwidth. This is, however, a secondary effect, not inherent to the presented efficiency enhancement technique.

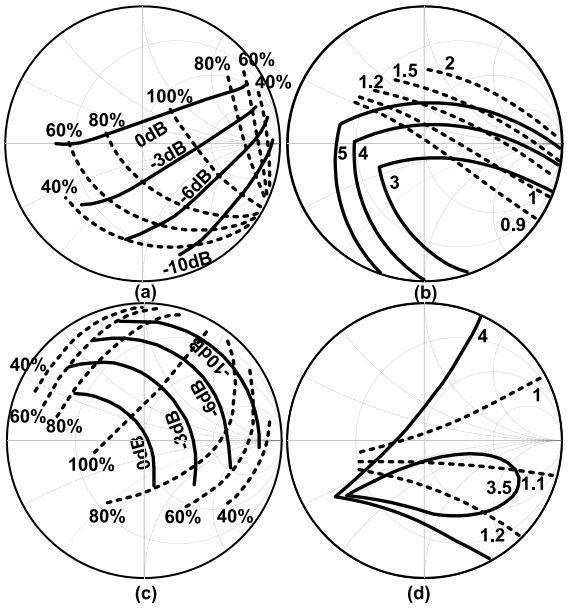

Fig. 12. Effect of changing d from 1 to 0.7 [(a) and (b)] and 1.2 [(c) and (d)] on the load-pull plots for $q = 1.3$ and $m = 0$, respectively. (a) and (c) Normalized output power (solid curve) and efficiency (dotted curve) contours. (b) and (d) $V_{c,\text{Max.}}$ normalized to V_{DD} (solid curve) and normalized output voltage amplitude (dotted curve).

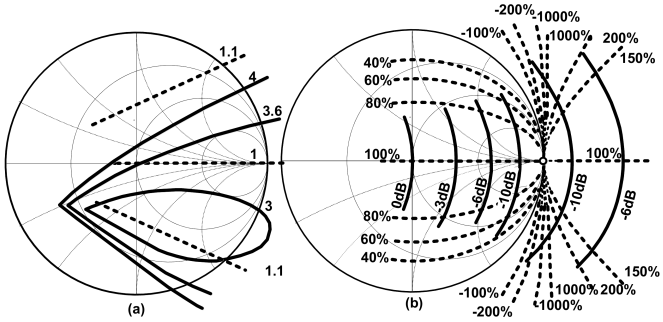

Fig. 13. Load-pull contours of a class-E PA with load-insensitive design and $m = 0$. (a) Maximum switch voltage normalized to V_{DD} (solid curve) and normalized output voltage amplitude (dotted curve). (b) Normalized output power (solid curve) and efficiency (dotted curve) contours.

1.78–1.88 GHz showed that the presented technique can improve the OPDR to more than 34.8 dB with at least 34% DE at 10-dB back-off in this frequency range.

Appendix A
Effect of Changing Duty Cycle on the Load-Pull Contours

The effects of changing parameter d from 1 to 0.7 (respectively, to 1.2) on the load-pull contours are shown in Fig. 12; clockwise (anti-clockwise) rotation occurs for lower (higher) d. Note that the normalized maximum switch voltage as well as the normalized output voltage amplitude contours change with the rotation. This can potentially impact the OEPAs' reliability and the OPDR which were taken into account in our efficiency improvement technique.

Appendix B
Extension of the Load-Pull Contours Toward Negative Impedances

The load-pull contours of a class-E PA with load-insensitive design, including negative impedances, are shown in Fig. 13. Outside the Smith chart, the real part of the load is negative and the direction of the output power is toward the switch (negative P_{out}). Positive efficiencies ($\eta > 100\%$) imply that the supply voltage V_{DD} sinks a fraction of the power that comes from the load (negative P_s). Since the switch loss is always positive, then $|P_s| < |P_{\text{out}}|$ which results in efficiencies more than 100%. Infinite efficiency shows that the whole power that comes from the load is dissipated in the switch and $P_s = 0$.

Negative efficiencies show that both the load power and the supply power are dissipated in the switch. Fig. 13 shows an intersection point where all the efficiency contours converge. At this point the load in open, $P_{\text{out}} = 0$, there is no loss in the switch, which then results in $P_s = 0$. Therefore, at this point, the efficiency is not defined; $\eta = (P_{\text{out}}/P_s) = (0/0)$.

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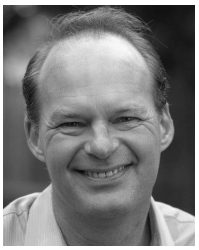

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