Capacitively-Coupled, Pseudo Return-to-Zero Input, Latched-Bias Data Receiver

Dissertation

Presented in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy in the Graduate School of The Ohio State University

By

Brandon Lee Mathieu, B.S.E.C.E., M.S.E.C.E

Graduate Program in Electrical and Computer Engineering

The Ohio State University

2018

Dissertation Committee

Dr. Waleed Khalil, Advisor

Dr. Steven Bibyk, Committee Member

Dr. Brian Dupaix, Committee Member

Dr. Hossein Miri Lavasani, Committee Member

Dr. Tawfiq Musah, Committee Member

Abstract

The ever-increasing demand for data throughput from both wired and wireless networks is continuously burdening high-speed chip-to-chip links. With proposed processor-memory interface standards exceeding multiple Tb/s of data [1] and leading-edge data converters requiring tens of Gb/s of data, power and area efficient data transfer is of utmost importance.

This work focuses on the development of a small, low-power, fully-integrated, clock-less capacitively-coupled data receiver. The architecture utilizes small on-chip termination and coupling capacitors in order to avoid parasitics, impedance discontinuities and density limitations associated with their board-mounted counterparts. The small coupling capacitors transforms non-return to zero data streams into bi-polar return-to-zero pulse trains. The pulses' polarities are digitally latched into the receiver via input bias switches, generating pseudo return-to-zero (PRZ) waveforms that reduces baseline wander and eliminates the need for data encoding or scrambling. A model of the PRZ signal is presented and compared to traditional AC coupled pulse receivers. Common mode feedback is included in the core of the receiver to account for process, voltage and temperature variation and mitigate duty-cycle distortion. Enhanced bandwidth digital inverters amplify the signal into a low-jitter full-scale digital signal that can directly interface with standard digital cell libraries, while rail-to-rail digital feedback serves as the

digital control signals for the bias switches. The coupling scheme enables a wide acceptable input common-mode range and compatibility with legacy applications targeted for short chip-to-chip links in die stacking and heterogeneous integrated packing solutions.

A 130 nm SiGe BiCMOS implementation of the receiver was analyzed, re-packaged and re-tested. Wire-bond inductance is eliminated via stud bumping and flip-chip die-on-board attachment. Calibrated testing resulted in a peak data rate of 10 Gb/s while consuming 5.1 mW and generating 23.2 ps p-p jitter. A peak power efficiency of 0.46 mW/Gb/s with 29.4 ps p-p jitter was realized at 8 Gb/s.

An optimized implementation of the PRZ receiver was fabricated in a 45nm CMOS silicon-on-insulator (SOI) process. This design includes broadband termination, reduced coupling capacitance, eliminated level-shifting, and minimized feedback delay. Testing revealed a peak data rate of 30 Gb/s with 7.8 p-p jitter and consuming 12.02 mW. A peak efficiency of 0.24 mW/Gb/s was recorded at 24 Gb/s with 15.0 ps p-p jitter. Both the SiGe BiCMOS and CMOS SOI designs exhibit BERs less than 10^{-12} with PRBS15 data as small as 100 mV peak-to-peak amplitude and occupy 0.012 mm^2 and 0.007 mm^2, respectively, including the on-chip coupling capacitance.

In honor and loving memory of Elizabeth Ann Crothers.
Your love and compassion made this possible.
I love you Grandma.

Acknowledgments

A thank you to all my family, specifically my parents and grandparents. Your unconditional love and support in all aspects of my life cannot be replaced. You have made me the man I am today, and all my accomplishments are because of you.

A sincere thank you to my undoubtedly favorite sister, Erica. Without your love and guidance I would not have completed all the challenges I have faced. Following your footsteps was the best decision I could have made. I'm proud share "Dr. Mathieu" with you.

I want to thank all the lab group members I have crossed paths with. We have shared a vital time of our lives with each other and I hope it has been beneficial to you as it has been to me. A special thank you to Dr. Jamin McCue, our spiraling conversations influenced this work and myself more than you know. Thank you to Dr. Lucas Duncan, without your guidance I would not be the circuit designer I am today. An additional thank you to Dr. Brian Dupaix, your mentorship paved the way even when I was not on the path.

Thank you to all my AFRL colleagues. Your expertise made this work possible, while your friendship made it enjoyable. Thank you to all my undergraduate and graduate friends, you are the reason why I never left OSU.

Many thanks to Dr. Steven Bibyk, you have taught me lessons that cannot be learned in a classroom.

A final thank you to my advisor, Dr. Waleed Khalil. Thank you for pushing and developing me far beyond what I understood. My respect and appreciation for your technical expertise and persistence cannot be expressed.

-Thank you.

Vita

Oct. 2012 – Feb 2016 …..... Test Development Engineer,

Advanced Integration LLC. (Advint)

May 2014…..... Bachelors of Science in Electrical and Computer Engineering,

The Ohio State University, Magna Cum Laude

Aug. 2014 – Aug. 2017 …..... Dayton Area Graduate Studies Institute Fellowship

May 2015…..... Masters of Science in Electrical and Computer Engineering,

The Ohio State University

Feb. 2016 – Present …..... Electronics Research Engineer,

United States Air Force Research Lab

Publications

B. L. Mathieu, J. J. McCue, L. Duncan, B. Dupaix, H. M. Lavasani and W. Khalil, "A Capacitively Coupled, Pseudo Return-to-Zero Input, Latched-Bias Data Receiver," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2500-2511, Sept. 2018.

B. Mathieu, J. J. McCue, B. Dupaix, V. J. Patel, S. Dooley, J. Wilson, H. Lavasani, W. Khalil, "An AC Coupled 10 Gb/s LVDS-compatible Receiver with Latched Data Biasing in 130 nm SiGe BiCMOS," in *2017 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct 2017.

L. Duncan, B. Dupaix, J. McCue, **B. Mathieu**, M. LaRue, V. Patel, M. Teshome, M. J. Choe, and W. Khalil, "A 10-bit DC-20-Ghz multiple-return-to-zero DAC with >48-dB SFDR," *IEEE Journal of Solid-State Circuit*, vol. 52, no. 12, pp. 3262–3275, Nov 2017.

L. Duncan, B. Dupaix, J. McCue, **B. Mathieu**, M. LaRue, M. Teshome, M. J. Choe, and W. Khalil, "A 10b DC-to-20Ghz Multiple-Return-To-Zero DAC with >48dB SFDR," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 286–287.

J. J. McCue, B. Dupaix, L. Duncan, **B. Mathieu**, S. McDonnell, V. J. Patel, T. Quach, and W. Khalil, "A time-interleaved multimode ΔΣ RF-DAC for direct digital-to-rf synthesis," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1109–1124, May 2016.

Field of Study

Major Field: Electrical and Computer Engineering

Minor Area: Computer Engineering

Specialization: Mixed Signal Integrated Circuit Design

Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction

1.1 Motivation

With the explosive growth of global data traffic over the recent decades forecasted to continue for the foreseeable future [1] [2], efficient transmission of digital data is top a priority in both wired and wireless networks. High-resolution video displays, multimedia systems, broadband internet, smart devices, the internet of things (IoT), and widespread adoption of data-intensive applications - including video streaming, cloud-based computing, and virtual presence devices - have contributed to an overwhelming demand for data throughput and processing [2] [3] [4] [5] [6]. Calls for aggregate data rates of over 1 Tb/s per chip are becoming more common [7], with the Hybrid Memory Cube and High Bandwidth Memory requiring greater than 8 Tb/s of throughput [8]. Mixing the evolving spectrum of standards while maintaining legacy support has increased the need for flexibility, adaptability and re-configuration of traditional analog functions via the digital domain. In addition, the popularity of mobile and attritable platforms continually constrains area, power and thermal resources curbing the ability to achieve high data throughput.

1.2 Contributions

This work involves the development and refinement of a standalone small area power efficient high-speed data receiver. The target application is high-speed data converters for next generation software defined radios. However, the need for a robust

independent data receiver block far exceeds this one application. A preceding design established a functional implementation [9]. The expansion of the architecture was needed in order to full-fill new requirements and hone operation. The existing implementation was analyzed, leading to the expansion of the architecture's model in order to capture the proposed latched-bias receiver behavior.

Additional investigation on the preceding design found unnecessary penalties were incurred due to outdated wire bond packaging being utilized. A series inductance due to the wire bond to all pads increased power and ground ripple and channel loss on both the input and output of the test article. To reduce the series inductance experienced on all of the pads, a new printed circuit board (PCB) was designed and fabricated to utilize stud-bump and die-on-board attachment packaging. The repacking and employment cable calibration via transmitter pre-emphasis decreased p-p jitter and reduced power consumption.

The expanded model was leveraged to complete a new implementation of the proposed latched-bias receiver in an advanced complementary metal oxide semiconductor (CMOS) silicon on insulator (SOI) technology. The CMOS SOI technology was chosen due to favorable switching speed and efficiency of the transistors. The design was created, fabricated, tested, and results are presented.

1.3 Outline

This dissertation documents the board design and testing of the legacy receiver along with the modeling, design, implementation, and testing of the capacitively-coupled, pseudo return-to-zero input, latched-bias data receiver circuit implementation in a 45 nm

SOI CMOS technology. Chapter 2 provides background and explanation of the challenges that high-speed data transfer encounters. Chapter 3 introduces the capacitively-coupled, pseudo return-to-zero (PRZ) input, latched-bias data receiver architecture and PRZ signal model. Chapter 4 reviews the legacy receiver design along with the retesting of validation completed. Chapter 5 details the 45 nm CMOS SOI circuit design and testing. Finally, chapter 6 gives a summary of the work along with future goals of the capacitively-coupled, PRZ input, latched-bias data receiver.

Chapter 2: Background

2.1 Non-Return to Zero Digital Signal

In order to successfully implement high-speed error free data transfer, the wide bandwidth nature of digital signals must be understood. By far the most common digital signal type is non-return-to-zero (NRZ). A NRZ digital signal can be represented as a square wave with period equal to twice the data stream's bit period. In the frequency domain, a square wave is composed of a DC component, a fundamental frequency and odd harmonics of the fundamental. An ideal square wave with zero rise/fall time, has an infinite number of odd harmonics and therefore an infinite bandwidth. While infinite bandwidth is not physically realizable, a finite bandwidth and therefore finite rise/fall time is the typical NRZ digital signal model. The number of odd harmonics present influences the flatness and rise/fall time of the signal. If a small number of harmonics are included, the NRZ signal resembles a sine wave with linear step edges characteristics. When all of the odd harmonics are removed, only the DC component and fundamental are present and the waveform has a bandwidth equal to one-half the data rate (DC to data-rate/2). If a NRZ digital signal is toggled at the maximum bit rate, the signal represents a balanced, 50% ones 50% zeros, clock signal (i.e. 010101 pattern). This repetitive pattern, depicted in Figure 1, has the same frequency components at every time instance.

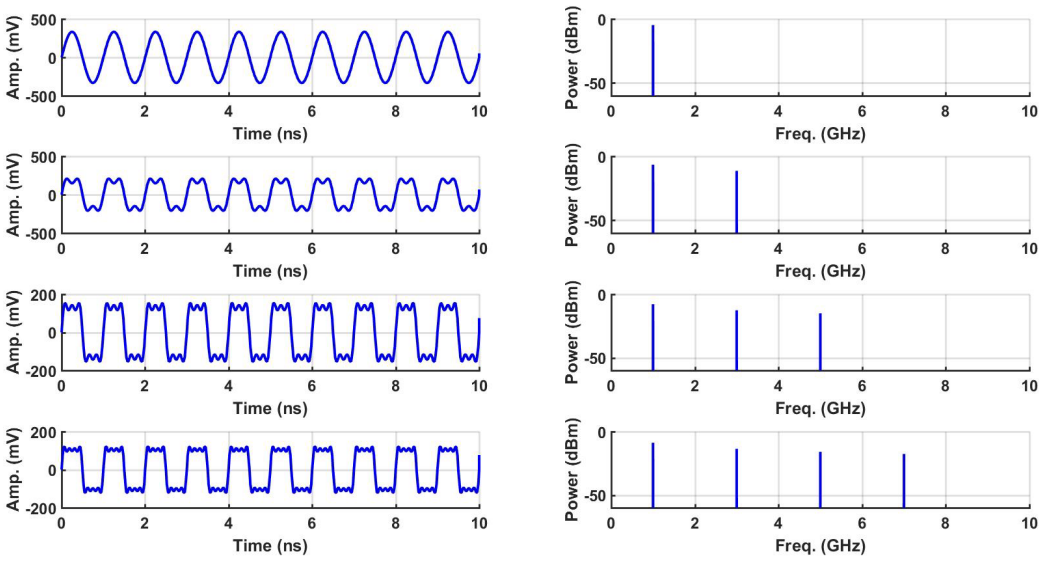

Figure 1 – 2 Gb/s toggling data stream and harmonic content

If the pattern becomes irregular or unbalanced (i.e. 101110), the fundamental frequency and odd harmonics shift based on the bit pattern. This shift has an inverse relationship to the number of consecutive identical digits (CIDs) [10]. When the frequency spectrum of a busy or pseudo random bit stream (PRBS) is viewed, an average of all the individual shifts is present. Figure 2 shows a small portion of an example pseudo random bit stream and power spectrum averaged over 1,000-bit periods.

The power spectrum over a large number of random bit value reveals a sinc response with nulls at multiples of the data rate [11]. These characteristics are of a near ideal single data stream. If additional data streams are added to a system, the behavior of the individual signals becomes complex when non-idealities and environmental factors come into play, such as cross-talk. Multi-lane system analysis is outside the scope of this work.

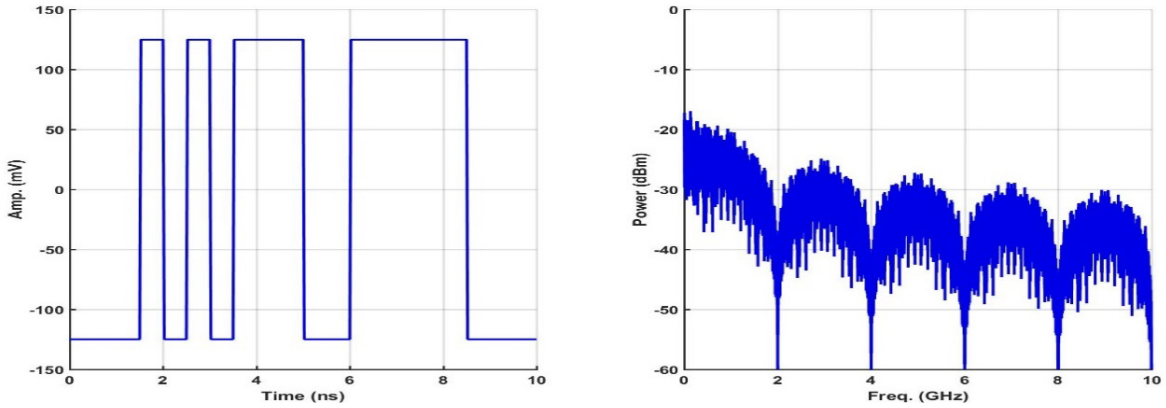

Figure 2 – 2GB/s PRBS data stream and harmonic content

2.2 Parallel vs. Serial

If a system requires data at a higher throughput or lower latency than the current channel can provide, either the data rate or number of data channels must increase. To meet high chip-to-chip data rates, solutions have evolved to utilize either a large number of low-speed parallel channels or a limited number of high-speed channels that implement serializing/deserializing (SERDES) functionality. Parallel solutions place the burden of high data throughput on the design's manufacturability, and cost (via pad and connector area). Highly parallel data schemes reduce design complexity and risk by leveraging verified, low performance, and power inefficient I/O cell libraries.

Alternatively, SERDES architectures combine multiple independent data streams into a serial stream, transmits it at an increased data rate, and then de-serializes it into its original form. The increase of a channel's data rate directly affects the signal's bandwidth. Such solutions require non-standard high-speed transmitters and receivers. The inclusion of channel equalization is common as dielectric loss and the skin effect increase with frequency. The required high-speed and complex equalization shifts the burden of data

transmission from an area concern to a performance and power consumption challenge. While the speed and power consumption of transmitters and receivers scales with technology, channel equalization greatly affects the power efficiency of a design, with transceiver efficiency trends decreasing by an order of magnitude for every 30 dB of channel loss [12].

The choice between parallel or serial communication schemes is highly dependent upon the application. Parallel schemes can provide rapid expansion capability, while a serial scheme can enable high levels of integration. In order to leverage advantages of both, parallel SERDES schemes have evolved to enable expandable highly integrated standards, with the peripheral component interconnect express (PCI Express) being one of the most utilized. While feature rich standards enable communication between various modular system level components, the complexity of such highly-capable transceivers can unnecessarily limit performance in low-level applications.

2.3 Chip-to-Chip Interfaces

High data throughput integrate circuits (ICs) such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), memories, field programmable gate arrays (FPGAs), system-on-chip (SoC) architectures continually push the limits of technology. High-speed chip-to-chip data interfaces span a variety of implementations including printed circuit boards (PCBs), inter-package, heterogeneous integration, and three dimensional integrated circuits (3DICs) [8] [13] [14]. These all pose various packaging challenges including: high-loss responses (30+ dB), impedance mismatches/discontinuities, and stringent alignment/spacing requirements.

While PCBs provide an inexpensive solution to packaging integrated circuits (ICs), they come with increased channel loss and impedance discontinuities due to lower quality material, large vertical interconnect access (VIAs) and limited manufacturing tolerances. Wire bonding is highly utilized in inter-package solutions. However, low perimeter pad density and excessive parasitics, including substantial series inductance, decrease individual and aggregate bandwidths [15]. Heterogeneous integration and 3DICs pose particular challenges associated with varying ground, common-mode, and signal swing levels. These differences require level-shifters or alternating current (AC) coupling to transfer signals between the integrated dies [8] [15].

Close-proximity links have emerged as a solution for data throughput and packaging limitations for chip-to-chip data interfaces. Close-proximity links include: flip-chip, micro bumps, buried solder bumps, through/backside VIAs and air-gap packaging methods. One advantage of these techniques is that they allow pads to be placed throughout the area of the chip, increasing I/O density and supporting wide communication parallelism. This advantage scales well with chip complexity, is less expensive, and enables smaller footprints [15] [16]. An additional benefit of close proximity links is the advantageous expansion in the vertical direction reducing communication distance drastically. This minimizes channel loss and is well suited for AC coupled interfaces. AC connections can increase I/O density and chances for rework [13] [17], which eases manufacturing concerns and maximizes freedom for commercialization and intellectual property reuse [18]. However, specialized circuitry is needed in order to take full advantage of these techniques and meet data throughput demand.

2.4 Coupling Schemes

The packing and integration of ICs not only define the physical constrains but also define the electrical behavior. As technology scaling has progressed, transistors' figures of merit have increased into the 100's of GHz, reducing parasitics and power consumption. However, the main limitation to the speed of a transceiver design is the channel response.

Traditionally and most often, the coupling scheme is a continuous DC interconnect that is composed of conductive material allowing signals of all frequencies to pass (ignoring parasitic attenuation). This is desired, as it does not remove any of the signal content when transferred from one circuit to another. When parasitics are included, the channel response generates a low pass filter response, as shown in Figure 3. High frequency attenuation can be counteracted with various equalization, including pre-emphasis at the transmitter and analog continuous time linear equalizers and digital decision feedback equalizers in the receiver.

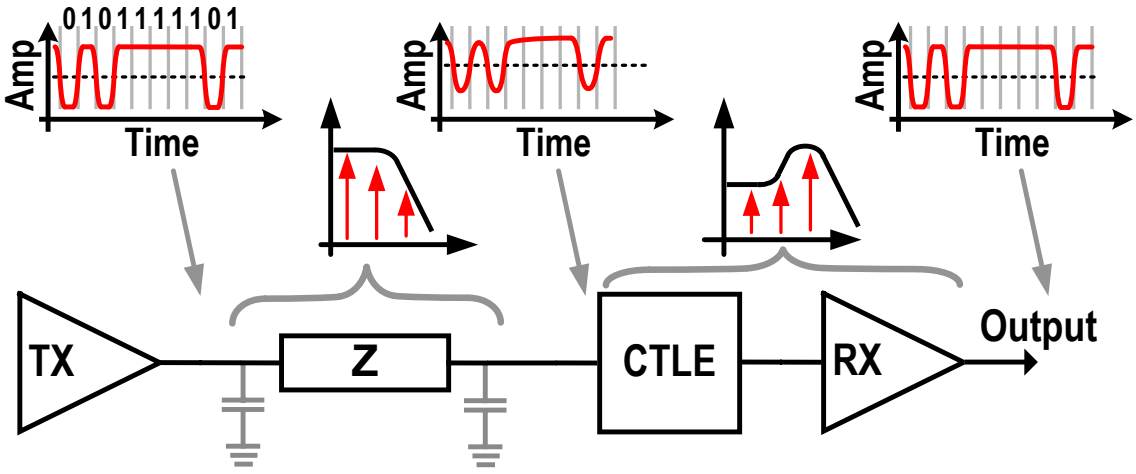

Figure 3 – DC coupled high-speed data channel block diagram

Parasitic attenuation can affect all frequencies including DC as a series resistance between the transmitter and receiver. This resistance can alter the signal's common-mode creating a mismatch between transmitter and receiver. The introduction of heterogeneous integration and 3DICs increases the potential mismatch as dissimilar technologies and circuit architecture can utilize signals with common modes varying by multiple volts. Both small and large common-mode mismatch can cause duty-cycle distortion [3] resulting in crippling output jitter.

An alternative to DC coupling is AC coupling. AC coupling introduces a physical gap in the channel, which removes the DC connection between transmitter and receiver. This facilitates isolation between transmitter and receiver while allowing independent optimization of common-modes [3]. A fundamental point to understand when implementing AC coupling is that the DC value of a NRZ digital signal carries no information [13] [17] [19] [20]. The information in a digital signal is carried in the timing, polarity and amplitude of the transitions. The transition timing is based on the baud rate of the signal, while the polarity and relative magnitude is determined by the signaling scheme (e.g. NRZ, RZ, PAM4, etc.). The amplitude of the signal depends on driver signal strength and channel response attenuation.

The addition of AC coupling generates a band-pass channel response that is composed of two parts. The AC coupling forms a high-pass filter response, while circuit and transmission line parasitics creates a low-pass response [19]. The band-pass response can exceed that of a second order due to significant parasitic capacitance at the output of the driver [17]. The idea of passing a digital signal through a channel with a band-pass

response has been studied as far back as the 1960's [21]. If the data stream is highly active or "busy" and the high-pass corner frequency is kept much lower than the bit rate, the band-pass response highly resembles the traditional DC coupled interconnect low-pass response while enabling DC isolation. However, if the data stream is static for large numbers of bit periods, bit errors can occur due to the lack of a DC driver. There are two forms of AC series coupling: inductive and capacitive, by means of transformers and capacitors, respectively [17].

2.4.1 Inductive Coupling

Inductive coupling is formed via the placement of at least one transformer between the transmitter and receiver, as shown in Figure 4. Inductors are placed in a shunt configuration, introducing the channel's band-pass frequency response. The low-pass corner of the band-pass behavior is inversely controlled by the value of inductance chosen while the high-pass corner is governed by the channel and circuitry parasitics. Inductive coupling easily delivers low frequency signals, and can be used to enable power harvesting to low power circuits. This allows for extremely high power efficient data transfer [22].

Inductive coupling interconnections (ICI) have been used extensively in smart cards, radio-frequency identification (RFID) systems, and in other contactless systems to communicate both power and signal information across an interface [15]. Inductive coupling has also been used for 3DICs due to the reduced co-planarity requirements compared to other topologies [17]. At the expense of circuit complexity, inductive AC coupling can be used to bring I/O pad pitches down to 75μm and maintain a controlled impedance connection [17].

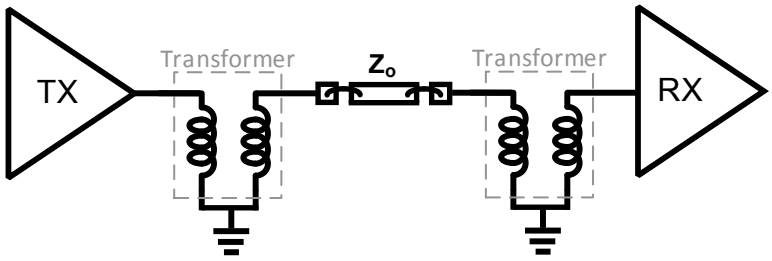

Figure 4 – Inductive coupling interconnect block diagram

On-chip inductive coupling of high-speed data channels is challenging as state-of-the-art CMOS technologies provide feature sizes in the nanometer range. While microscopic feature sizes minimize transistor and trace capacitance, metal-stack selection and fabrication yield design rules limit maximum metal trace thickness and widths which contribute notable series resistance to the metal coils. This results in low quality factor (Q-factor) inductors and consequentially creates a trade-off between bandwidth and loss. In addition, the relatively high cost of chip area limits the size and number of coils, therefore defining the maximum inductance value and I/O density. For this reason inductive coupling is better suited for low speed, low pin count, power efficient applications [22].

2.4.2 Capacitive Coupling

Capacitive coupling adds series capacitance between a transmitter and receiver, as shown in Figure 5. When low power I/O buffers are utilized, capacitive coupling offers better performance than inductive coupling [17], enabling highly efficient transceivers. Similar to inductive coupling, a bandpass channel response is generated via the coupling capacitor and channel parasitics [19]. The capacitance value contributes the high-pass component while the parasitics (dielectric loss, skin effect, shunt capacitance) are responsible for the low-pass response. Capacitive coupling is extensively used in testing

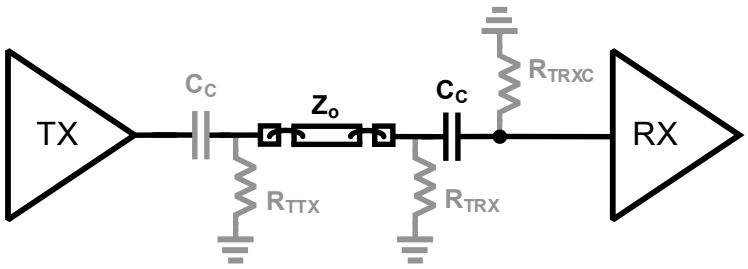

Figure 5 – Capacitively coupled interconnect block diagram

and in analog through millimeter RF design. In testing, DC blocks and bias tees utilize large capacitors to protect test equipment from hazardous DC potentials without affecting the integrity of AC measurements. These filters are designed with 3 dB cutoff frequencies in the hertz to low megahertz range. In analog and millimeter wave designs, series capacitors provide DC isolation and means to create matching networks for various circuit topologies.

In addition to these uses, capacitive coupling has long been a solution for coupling digital signals. Various standards and protocols implement capacitive coupling with one of the most popular standards being PCIe. Capacitive coupling can be implemented by placing a capacitor before, after, or at both ends of a channel. Single-sided termination can be used, however double termination reduces transmission line reflections and cross-talk between traces at the expense of reduced signal swing. These interconnects have been called capacitive coupling interconnect (CCI) [15] and AC capacitive coupled interconnect (ACCI) [4] [13] [19].

The deep sub-micron CMOS minimum feature sizes enable fabrication of various capacitor types, with typical values in the femto to nano Farads. These small feature sizes enable high quality (high Q) metal-insulator-metal (MIM) and interdigitated capacitors

with self-resonant frequencies in the 100's of GHz. The high Q capacitors enable high frequency coupling and are much smaller than their inductive equivalent. These reasons contribute to the dominance of capacitive coupling in high-speed digital applications.

2.5 Capacitive Coupling Challenges

Capacitive coupling offers great flexibility with the removal of common mode limitations. The tradeoff with this flexibility is the introduction of an imperfect capacitor into the signal path adding signal attenuation, impedance mismatches and discontinuities, and baseline wander. To overcome these challenges, previous designs have utilized varying equalization, impedance matching networks, data manipulation schemes and latching techniques [17].

2.5.1 Signal Attenuation

AC coupling effectively blocks DC and filters low-frequency components. This filtering can provide bandwidth extension up to 3 times higher than a DC connected channel [22], which is very attractive as data rates increase. The extension of 3dB bandwidth is a result of passive equalization generated by the coupling capacitor which attenuates low frequencies and does not amplify high frequencies. However, this bandwidth increase comes at a cost of signal amplitude. The majority of a digital signal strength is in the fundamental frequency of the signal (the lowest non-DC frequency), therefore if the series capacitor's high-pass response encroaches on the digital signal's low frequency content the signal's amplitude decreases. If the amplitude dips below the receiver's sensitivity, bit error rate (BER) increases and date is lost. The low frequency attenuation and bandwidth extension are apparent when DC and AC coupled transfer

functions are plotted verses magnitude, Figure 6. The smaller the coupling capacitance the more observed attenuation encroaches on both CID fundamental and toggling fundamental frequencies. This reduces the amplitude of the digital waveform and increases the sensitivity requirements of AC coupled receivers to compensate for the signal power lost.

2.5.2 Capacitors: On-Board vs. On-Chip

For legacy and low speed (kilo- to mega- baud) data links, the waveforms (typically with 100's ps rise/fall times) contain little high frequency content. In order to limit affecting the coupled waveform's integrity, the high-pass corner frequency of the capacitive coupled channel needs to be kept well below the bit rate; with one author deriving the high-pass corner frequency should be set less than 15% of the bit rate [23]. These implementations, with the assumption of a 50-Ω transmission line and termination, require capacitors in the

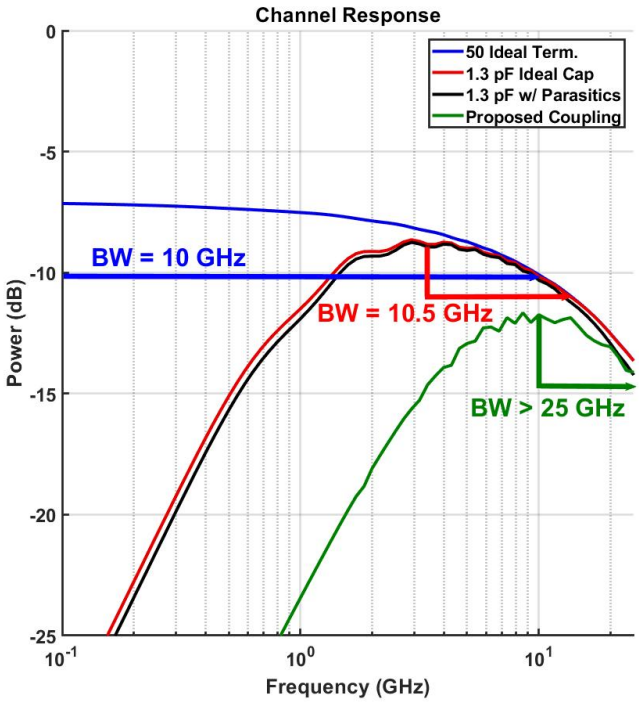

Figure 6 – AC Couple channel response of a modeled 2.5 cm FR4 trace

pico- to nano- Farads. These capacitive values require extensive area along with high parasitic values. For ease of integration and flexibility, on-board (typically surface mount) capacitors are used. These large coupling capacitors (C_C) are capable of generating large coupling time constants and must be designed to accommodate the lowest frequency data frame expected. This methodology has been thoroughly investigated and is widely practiced today. This approach, however, is problematic when designing for universal or general purpose busses where the lowest frequency data frame is unknown.

With the advancement of technologies and increased data rates (giga-baud), waveforms now have extensive high frequency content (typically with 10's ps rise/fall times). On-board capacitors have become a limiting factor in that they require VIA stubs, which create complex channel responses due to input stage impedance discontinuities, loss, dispersion and reflections [10]. The addition of just two mounting VIA stubs, loss can surpass 3 dB [18]. In addition, board technology miniaturization and cost have not kept pace with very large scale integration (VLSI) technology scaling. This has led to off chip-capacitors becoming relatively equal to and even larger than an integrated receiver itself. This can limit I/O density and manufacturability due to minimum trace widths and spacing, driving the cost of board manufacturing. Large computing networks that employ tens, hundreds and even thousands of data channels can greatly benefit from the elimination of off-chip capacitors' area [10].

Realizing coupling capacitors on-chip reduces their overall size and limits the impedance discontinuities due to standard on-board 50-Ω transmission lines and elimination of VIA stubs. 3DICs especially benefit from the removal of on-board

capacitors and allowing the top metal layers of the stacked die to be utilized as the parallel capacitor plates, easing vertical integration and increasing connection density compared to DC connections [17]. Though miniature, on-chip capacitors can be relatively costly due to occupying expensive die area and typically requiring a dedicated footprint. Because of this, designers must use the minimum acceptable capacitance in order to reduce size and therefore cost. On-chip capacitors (assuming MIM and interdigitated capacitors) have high self-resonance frequencies, which allow for less distortion and higher data rates operation.

Termination follows the same trajectory as coupling capacitors. On-board termination requires VIA stubs, while on-chip termination can achieve broad matching with less attenuation at high frequencies. With high-speed data channels favoring 50-Ω transmission lines, reduction of reflections and cross-talk is required [19]. Termination placement needs to be carefully examined based on application requirements and channel characteristics (discontinuities, stubs, connectors, VIAs, etc.) [17]. Typical termination schemes include at transmitter, at receiver or both.

In both methods of AC coupling capacitor sizing (large/board-mount: low corner frequency or small/on-chip: pulse generating), varying compensation, latching and equalization are needed. With large capacitances, data manipulation and high frequency compensation are required to achieve reliable high-speed operation. The data manipulation ensures the signal's energy is located above the low frequency cutoff of the bandpass response, while the high frequency equalization enables channel correction and recovery of short bit periods. Small coupling capacitors provide passive equalization, reducing the need for high-frequency equalization while adding increased sensitivity requirements and

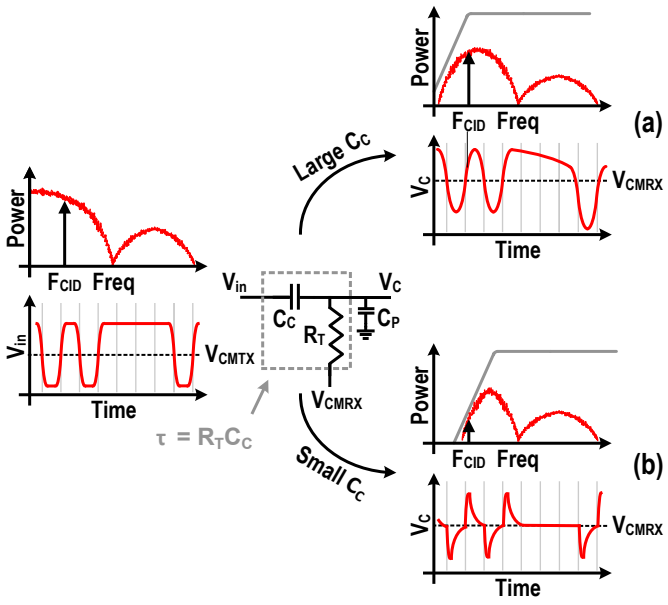

Figure 7 – Time and frequency representations of NRZ input signal, (a) large board-mount capacitor AC-coupled signal, and (b) on-chip small capacitor AC-coupled signal.

low frequency/DC recovery. Figure 7 displays the effects of large board-mount and small on-chip capacitive coupling of an NRZ data stream in both the frequency and time-domain.

2.5.3 Baseline Wander

Traditionally, AC coupling is used in analog and RF circuits which have narrow periodic/balanced signals. Digital transceivers are subject to wide band unbalanced signals with arbitrary sequences of ones and zeros. As previously discussed in Section 2.1, when CIDs are included in data streams, the frequency content of the signal shifts towards DC. If this frequency shift enters the lower stop-band of the band-pass channel response, a low frequency meander of the coupled signal is generated, also known as baseline wander. When an AC coupled NRZ digital signal is plotted, the DC value of the signal wanders up and down based on the balance of ones and zeros. An increase in baseline wander indicates a balance favoring the zero/low value, while a decrease indicates a balance favoring the

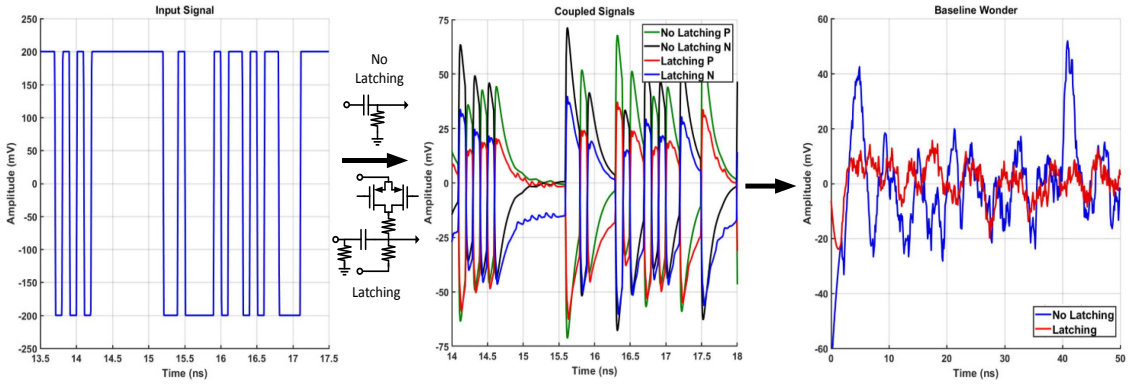

Figure 8 – Baseline wander comparison with and without proposed latching

one/high value. Figure 8 shows a NRZ input signal and resulting differential capacitively coupled signal and baseline waveforms. The coupled waveform experiences high levels of baseline wander and evident by large spikes nearing 25% of input amplitude near times of large CID counts. Baseline wander is effectively a dynamic data dependent common-mode mismatch between transmitter and receiver and can hinder performance greatly. This baseline wander can be combated with data manipulation and the use of pulse receivers.

2.5.4 Encoding & Scrambling

Random data streams include periods of varying degrees of balanced and unbalance sequences. In the extreme case of a completely unbalanced signal (all 1's or all 0's), the digital signal resembles a DC signal. Random data streams can include such behavior and much be accounted for when transferred across AC coupled interfaces. One approach is to manipulate the data stream with encoding or scrambling. These data manipulation techniques bound the lowest frequency content of the signal by transforming unbalanced data streams into statistically balanced streams. This ensures the frequency content does

not drop below the high-pass channel response limiting baseline wander to a known level that can then be designed and tested to.

The ability to ensure long-term balanced signals has enabled continual expansion of AC coupled data interfaces. Commonly used encodings range from 8b/10b (i.e. Serial ATA) to 128b/130b (PCIe 3.0) [6]. Xb/Yb encodings build packets Y bits wide from X bit wide data. Therefore, the encoding reduces the effective data rate with the encoding efficiency computed as X/Y*100. These extra bits guarantee data transitions every so often at the expense of added power, area, latency and system complexity.

Scrambling is used to constrain the largest number of CIDs transmitted. As PRBSs are known to have a finite number of CIDs, they can be used as a map to invert bits in an arbitrary data sequence. Statistically, this generates sequences with certain levels of DC balance. Scrambling does not add any additional bits to the stream and therefore does not reduce the effective data rate, but it also does not guarantee a truly balanced signal. For this reason, scrambling is sometimes paired with encoding to increase the level of DC balance in data streams with near full effective data rates (i.e. PCIe 3.0 uses 128b/130b with PRBS23 scrambling) [4]. The data manipulation can be done in software domain, but in order to encode and scramble data at real-time speeds, hardware implementations must be used. In both methods, additional power and latency is added from encoding and/or scrambling before the transmitter and decoding and/or descrambling on the receiver side.

2.5.5 Pulse Receivers & Data Latching

The flexibility of AC coupled interfaces without the limitations of baseline wander or the burdens of data manipulation is ideal. When a small coupling capacitance is utilized

and coupled node time constant can be near that of a bit period, a bi-polar pulse train, which corresponds to the NRZ signal's transitions is generated, as shown in Figure 9. This coupled waveform highly resembles a return-to-zero (RZ) or duo binary signal, achieving a single settled value near the end of each bit period and eliminating baseline wander. Unfortunately, standard digital cell libraries cannot operate on coupled RZ signal and require the original NRZ to be restored. This has driven the development of pulse receivers.

Pulse receivers employ latching mechanisms, such as positive feedback or hysteresis, to hold the polarization of the previous pulse until the next incoming transition, as shown in Figure 9. This allows for an indefinite number of CIDs to be recovered error free. A challenge associated with this methodology is that the bandwidth of the latch must match or exceed that of the original NRZ data stream to ensure error-free recovery. The gain-bandwidth tradeoff of transistors can limit these high-speed latches and required a great deal of power consumption. The benefits of using a pulse receiver can be seen by comparing the magnitude of baseline wander with and without latching. Figure 8 shows

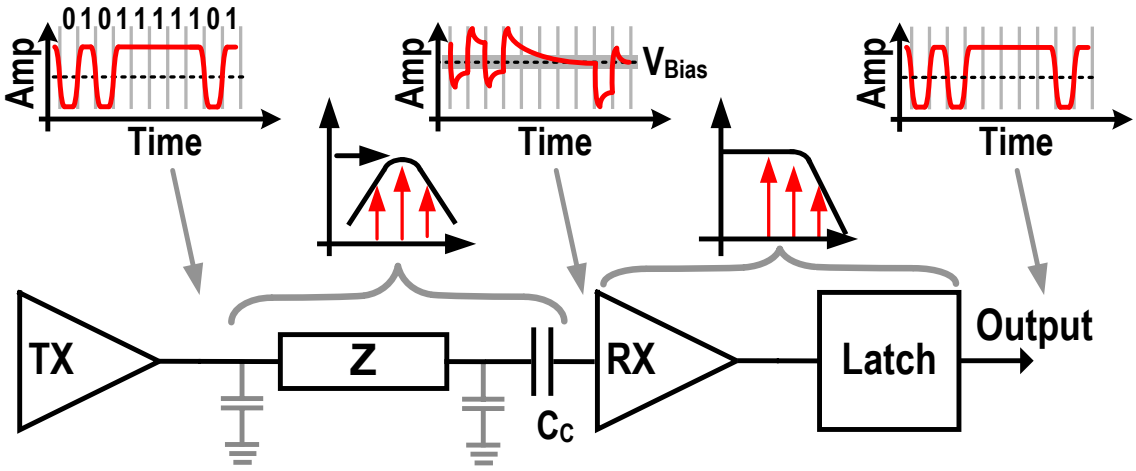

Figure 9 – Small on-chip AC coupled high-speed data channel block diagram

the coupled waveforms of the proposed pulse receiver implementing input bias latching and the corresponding baseline wander. Baseline wonder is still present in the coupled waveforms, but the magnitude is reduced and bounded due to the inclusion of latching.

For an ideal RZ waveform to be achieved, a single settled value must be reached prior to following transition. This requires the coupling time constant to be less than one-bit period. Figure 10 shows the high-pass RC network and resulting coupled RZ waveforms when driven by a 2 Gb/s NRZ signal with swept capacitance values of 100 fF to 2 pF. Upon comparison of the two transitions presented in Figure 10, the key difference between the various waveforms is the peak amplitude values. A larger capacitance increases the amount of energy transferred, which decreases sensitivity requirements, while a small capacitor limits the amount of energy coupled. This energy is then exponentially discharged at rate governed by the node's RC time constant, which then determines the width of the RZ pulse.

In Figure 10, targeted pulse generation is achieved with capacitor sizes of less than 1 pF, since the signal achieves the bias voltage within a bit period. If a capacitor size of greater than 1 pF is used, a voltage error (V_{ERROR}) occurs. V_{ERROR} is a measure of baseline wander on a bit-by-bit level and is calculated as the difference between a bias voltage and voltage achieved at the next bit transition (e.g. $V_{ERROR} \approx 50$ mV for 2 pF). This voltage difference can result in both reduced signal-to-noise ratio and timing margin. The resulting amplitude modulation can be seen by comparing the absolute of the peak values achieved for each transition. If amplified linearly, the amplitude modulation translates to reduced signal to noise ratio. If the signal is amplifier non-linearly, V_{ERROR} reduces timing margin in the form of timing jitter. This energy is representative of inter-symbol interference (ISI)

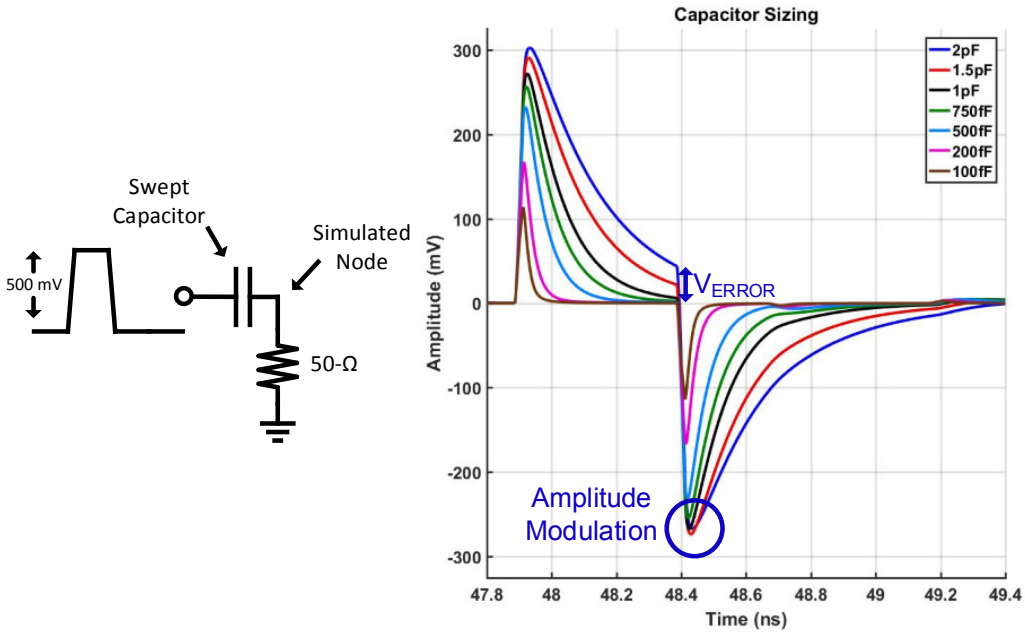

Figure 10 – Pulse receiver capacitor coupling sizing effects

with one bit "bleeding" into subsequent bits. By achieving a true RZ waveform this source of ISI is eliminated.

2.6. State-of-the-Art AC Coupled Pulse Receivers

Pulse receivers can be implemented in both the clocked and clock-less domains. In the clocked domain, a synchronous clock signal is used to sample and hold data values. In the clock-less domain, positive feedback and hysteresis circuits achieve a continuous time latching of the previous bit transition.

Due to the trend towards air gap application like 3DICs and heterogeneous integration, I/O density and power efficiencies have been of particular interest. Transmitters' power and area efficiencies have been on the rise due to the use of small modest circuitry, typically voltage mode drivers in the form of digital inverters. This is possible as close proximity do not require 50-Ω interfaces. These voltage mode drivers

provide increased power and area efficiencies that scale with technology but limit the opportunities to include transmitter equalization. Receivers' power and area efficiencies are governed by their architecture. Clocked data receivers include large complex, power hungry circuitry such as clock recovery and low phase noise phase locked loops. Small clock-less data receivers can operate at higher power efficiencies by eliminating the high power current-mode logic circuitry. However a forwarded clock from transmitter to receiver must be included to enable synchronous data transfer.

Clock-less pulse receiver architectures include: cross-coupled (NMOS or PMOS) load transistors, cross-coupled inverters, parallel linear and non-linear hysteresis paths, feed forward restore (FFR), Decision Feedback Restore (DFR), and average verses instantaneous comparisons. These architectures will be reviewed in the following subsections.

2.6.1 Cross-Coupled Transconductance

The most common form of a latch is achieved with cross-coupled load transconductance [14] [24] [25] [26]. This transconductance is generated by cross-coupled transistors (either NMOS or PMOS), typically placed in parallel with an amplifier's transconductance stage, see Figure 11. This architecture can be viewed as an amplifier with hysteresis. Clocked variations of this method resemble CML D flip-flops [14] [24].

Many of the reported designs implementing this latching method achieve data rates in the low Gb/s with only deep submicron designs achieving tens of Gb/s. This is due to

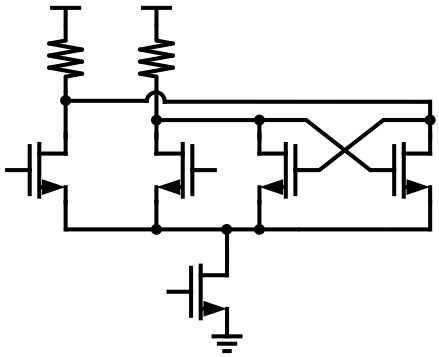

Figure 11 – Cross-coupled transconductance latch

the implicit capacitive loading of the cross-coupled pair placed on the amplifier. With the gates and drains of the cross-coupled pair attached to the output of the amplifier, parasitic capacitances (including the miller capacitance) load the amplifier, therefore decreasing bandwidth. In order to regain this bandwidth, continuous time linear equalizers (CTLEs) or digital feedback equalizers (DFEs) can be used at the expense of power, area and complexity. Additionally, inferior common-mode rejection and mismatch in the receiver can lead to jitter, as the strength of the latch is dependent on the output biasing. In [26], the authors implement this method with the addition of a parallel bandwidth extended path, achieved by the use of negative feedback. The outputs of the parallel paths are then combined with a four-port amplifier. This design achieves a respectable speed of 14 Gb/s but with decreased efficiency of 2.29 mW/Gb/s in a 90nm CMOS process.

2.6.2 Cross-coupled Inverters

A digital approach to the required latching is cross-coupled inverters [15] [17] [19]. Figure 12 (a) and (b) show cross-coupled inverters in both a series single-ended and parallel differential implementations, respectively. These methods provides reduced risk, simple

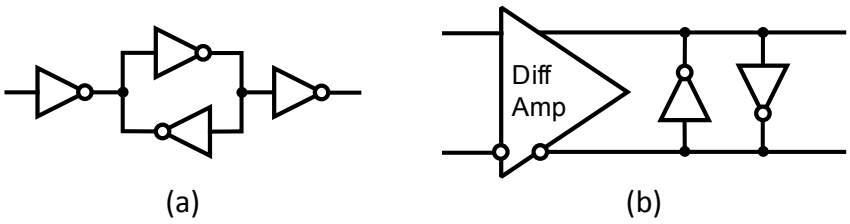

Figure 12 – Single-ended (a) and differential (b) cross-coupled inverter latches

latching mechanism for low speed designs, 2.5 Gb/s in 0.18µm CMOS [15] and 0.35 µm CMOS [19], 4 Gb/s in 0.35 µm CMOS [17] and 8 Gb/s in 65nm CMOS [27].

A limitation of cross-coupled inverters is two signals are driven onto the same node, the input signal and feedback signal. This configuration requires a strong input signal to overpower the feedback inverter in order for the latch to toggle; this is evident by the inclusion of pre-amplification stages. With drivers employed against one another, timing is unreliable and significant jitter is added to the signal. In addition, the skew between the inverters' trip point and input driver common mode of the amplified signal can add duty-cycle distortion.

This method has multiple inverters' parasitic capacitances hanging off the latching nodes, which ultimately limits bandwidth. In addition to the unavoidable nonlinearities of digital inverters, dynamic trip points of the inverters add to ISI. For these reasons, this approach has been limited to modest data rates.

2.6.3 Feed Forward Restore

A method that does not rely on a latch but modifies the AC coupling itself is the feed forward restore (FFR), presented in [4]. Figure 13 shows the top-level schematic of the presented FFR methodology. FFR places a resistive path ($R_{DC} + R_{FF}$) in parallel with

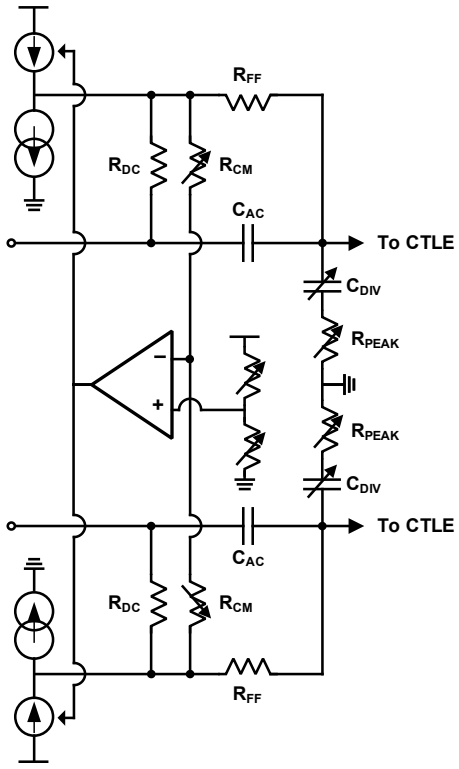

Figure 13 – FFR receiver input network diagram

the coupling capacitor; this generates a frequency dependent input impedance while maintaining a DC connection. At low frequencies, the impedance is dominated by the resistive component while at high frequencies the impedance approaches the resistance in parallel with the capacitance, this attenuates low frequencies compared to high ones. The low frequency attenuation is adjustable by changing the impedance on the coupled input node, accomplished by switched resistor banks (R_{PEAK}). The DC path is attenuated based on the implemented resistance values, R_{DC} and R_{FF}. In order to recover the NRZ signal, limiting amplifiers apply non-linear amplification to recover the attenuated low frequency and DC content.

This method allows for high-speed operation with [4] achieving 16 Gb/s in 22nm CMOS at 3.8 mW/Gb/s, but limits input common mode range to rail-to-rail. This limitation is appropriate for die stacking and multi-chip modules of technologies implementing the same or similar common-mode potentials. This method is ineffective for applications that experience variance in ground potentials or requires large differences in signal common-modes. An additional concern is the various nodes' parasitic loads. The various switched resistor banks on the input node and the common-mode regulation needed on the CTLE input limit obtainable bandwidths. Passive equalization is present, yet a CTLE is included in order to recover the signal's high frequency content across lossy channels.

2.6.4 Decision Feedback Restore

In [24] the authors use decision feedback restore (DFR) circuitry to detect and compensate for CIDs. The block diagram of the architecture is shown in Figure 14. This method requires a DAC and sample and hold (S&H) circuitry, therefore a clock is needed in this implementation. Based on the CFR logic, the coupled input nodes DC levels are adjusted by the DAC when CIDs are present.

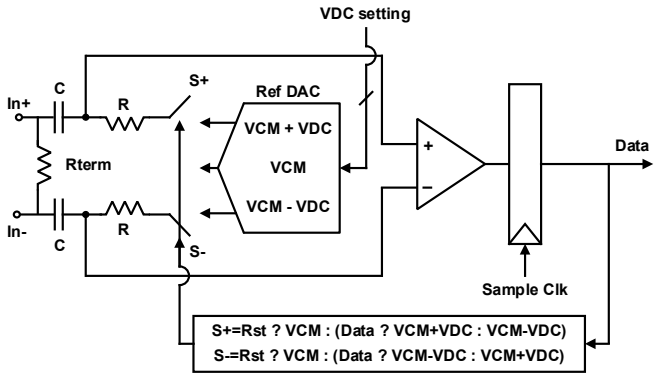

Figure 14 – Receiver block diagram implementing DFR

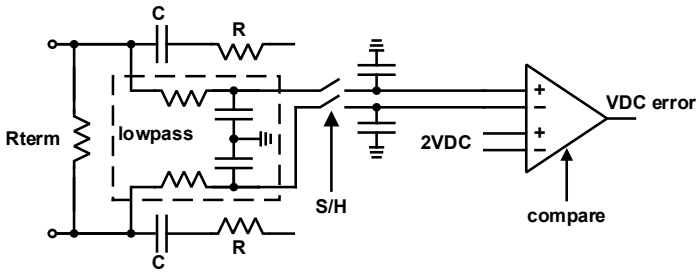

Figure 15 – S&H circuitry required for automatic adjustment of DAC output

The S&H circuitry, shown in Figure 15, is used to calibrate the DC levels applied to the coupled nodes. Implemented as a low pass filter and switched capacitor on the receiver's input, the S&H samples the- common mode of the input signal during CIDs. A differential comparator is used to recover the VDC error and enable automatic calibration during runtime.

This method is useful but drawbacks include: a long feedback delay, presence of a DC path to the pads, and wide swing S&H circuitry. The author reports operation at 5.2 Gb/s with eye diagram shown in Figure 16. From this diagram, the eye widens after

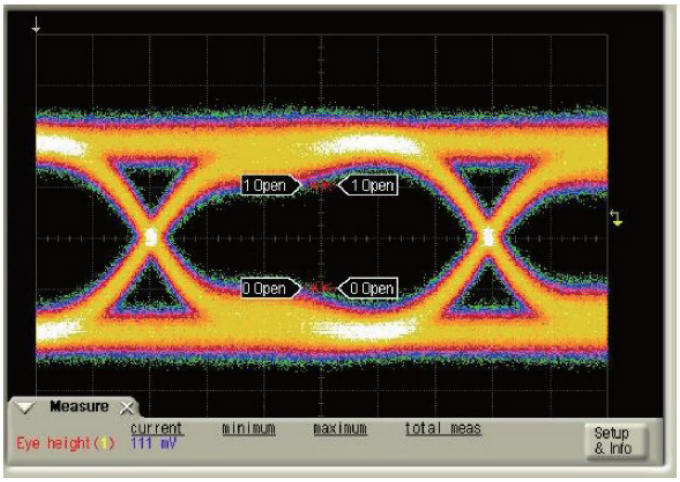

Figure 16 – DFR reciever eye diagram from [22]: Horz. 32.3 p/div

approximately 90-100 ps. It is hypothesized, this is when the adjusted common mode levels are latched onto the coupled input node. This delay is relatively large with respect to the design node of 65nm SOI and may be an artifact of synthesized logic. The presence of the S&H circuitry requires a DC path to the pads of the die. This limits the usefulness of AC coupling by ultimately limiting appropriate signal swing and common-mode levels. Since the S&H circuitry is connected to the pads, it needs to handle a wide common-mode range. However, the S&H only needs to operate at low speeds which eases the S&H design.

2.6.5 Average vs. Instantaneous Comparison

In [6], the authors present a baseline-wander common-mode-rejection (BLW-CMR) technique. As shown in Figure 17, BLW-CMR achieves common-mode recovery via two amplification stages and low-pass filters. The first amplification stage of the BLW-CMR compares an average of the coupled signal value with instantaneous coupled signal. This provides a delta in voltage that can be used to capture transitions. The delta in voltage is data dependent and therefore suspect to baseline wander, as shown in Figure 18 (1). The second amplification stage is an inverted copy the first stage and it too also experiences baseline wander, as shown in Figure 18 (2). The individual baseline wanders track in opposite directions of one another and therefore enables the cancelation of the duty-cycle distortion caused by the baseline wander, as show in Figure 18 (3).

The author does not report details on circuit implementation. Initial review of the technique reveals the need for a trans-impedance amplifier (TIA) prior to the AC capacitor, two amplification stages and data manipulation. With placement of the TIA prior to the AC

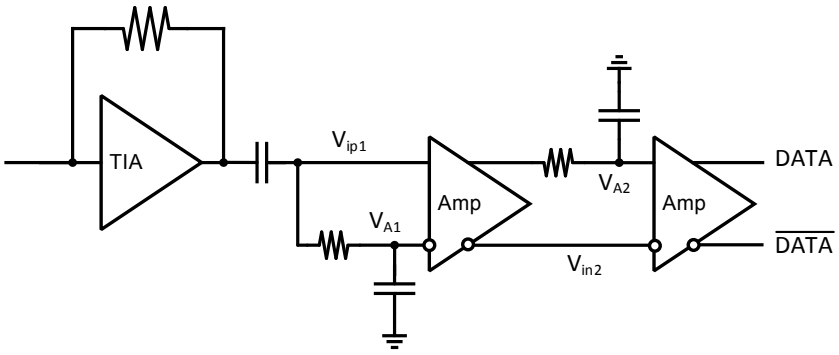

Figure 17 – BLW-CMR receiver block diagram

coupling capacitor, it is used as a pre-amplifier. It is assumed that this is needed in order to obtain the required sensitivity. One drawback of this is the common mode of the TIA must align with the detector's output in order to avoid duty-cycle distortion. Additionally, the cascaded amplification stages and unequal loading of the amplifier inputs by the addition of the low-pass filters increase sensitivity to mismatch and power consumption. With no calibration or adjustment circuitry presented, the circuit would be susceptible to process, voltage and temperature (PVT) variations. This technique does reduce the effects of duty-cycle distortion and is tolerant to strings of CIDs, but an indefinite string could cause bit

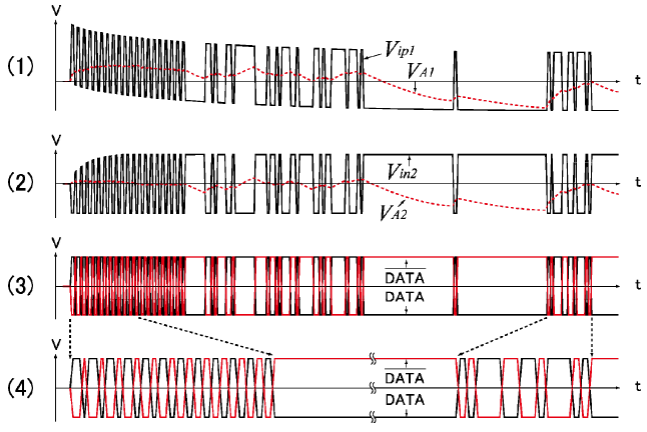

Figure 18 – BLW-CMR receiver waveforms from [7]

errors. Errors could occur when the averaged and instantaneous nodes approach one another and for this reason, data manipulation would still have to be added to the transceiver. The number of CIDs that could be recovered can be improved by increasing the time constant of the low pass filters; however, increasing capacitor and resistor sizes would decrease amplifier bandwidth via parasitic loading. Additionally the plots in Figure 18 are misleading; the Vip1 and Vin2 nodes do not show any AC coupling decay. If added, the plots would show a decrease in the number of CIDs this technique can recover successfully.

Chapter 3: Capacitively-Coupled, PRZ Input, Latched-Bias Data Receiver Architecture

As highly integrated microsystems continue to evolve, heterogeneous integration and 3DICs packing solutions are increasing the viability of close-proximity links for high-speed data transfer. These tightly mated ICs can increase performance while reducing size, weight, and power by compacting specialized technologies into highly compact multi-chip designs. High-speed data lanes benefit from drastic channel length reductions, however differences in acceptable common-mode ranges between transmitter and receiver can induce crippling performance degradation. This work focuses on the development of a fully-integrated capacitive AC coupled data receiver with latched input biasing that enables error free data recovery of PRBS data streams without the burden of data encoding or scrambling. By employing on-chip capacitive coupling, a wide acceptable common-mode range is achieved, while a common-mode feedback (CMFB) biasing schemes enables optimal biasing across PVT conditions. Enhanced bandwidth digital inverters are utilized to generate rail-to-rail signals which provide a direct interface to further on-chip digital processing. In this chapter, the proposed latched-bias receiver design is introduced and optimization of the generated pseudo return-to-zero (PRZ) waveform is presented.

3.1 Capacitively Coupled Input Network

As discussed in Section 2.4.2, large board-mount and small on-chip capacitive coupling are utilized in varying applications. The area and parasitics imposed by board-

mount capacitors were not practical nor feasible for the targeted micron spacing packaging solutions of this work. While on-chip capacitors alleviated these constrains and enabled the fully integrate nature of the proposed receiver, the small time constant of the coupled input nodes requires detailed modeling of the high-pass input network in order to maximize the peak coupled amplitude (V_P) while minimizing any voltage error (V_E) for a given bit period (T_B). Figure 19 depicts an NRZ input signal (V_{IN}) and the effects of coupling through both large board-mount and small on-chip coupling capacitors over two CIDS.

In the large C_C coupling case, the coupled signal (V_C) signal exhibits a V_P almost equal to the input peak value (V_{in_pk}) and slowly decays apart from V_{IN} during the subsequent CID. Alternatively, the small C_C cases experience decreased V_P values and decay rapidly towards the receiver common-mode bias (V_{CMRX}). In both scenarios, the coupled waveform experience a departure from the intended NRZ signaling and therefore can exhibit a V_E, however the dissimilar V_Es measurement reference differ. In the large C_c case V_E is measured between the coupled signal and the input signal, while in the small C_c cases V_E is measured between the coupled signal and V_{CMRX}. Both V_E measurements are taken at time T_B. This difference in V_E measurements drives the opposing design methodologies of receivers. Both methodologies share the design objective to minimize V_E, however the relationship between capacitance value and V_E value are dissimilar. In

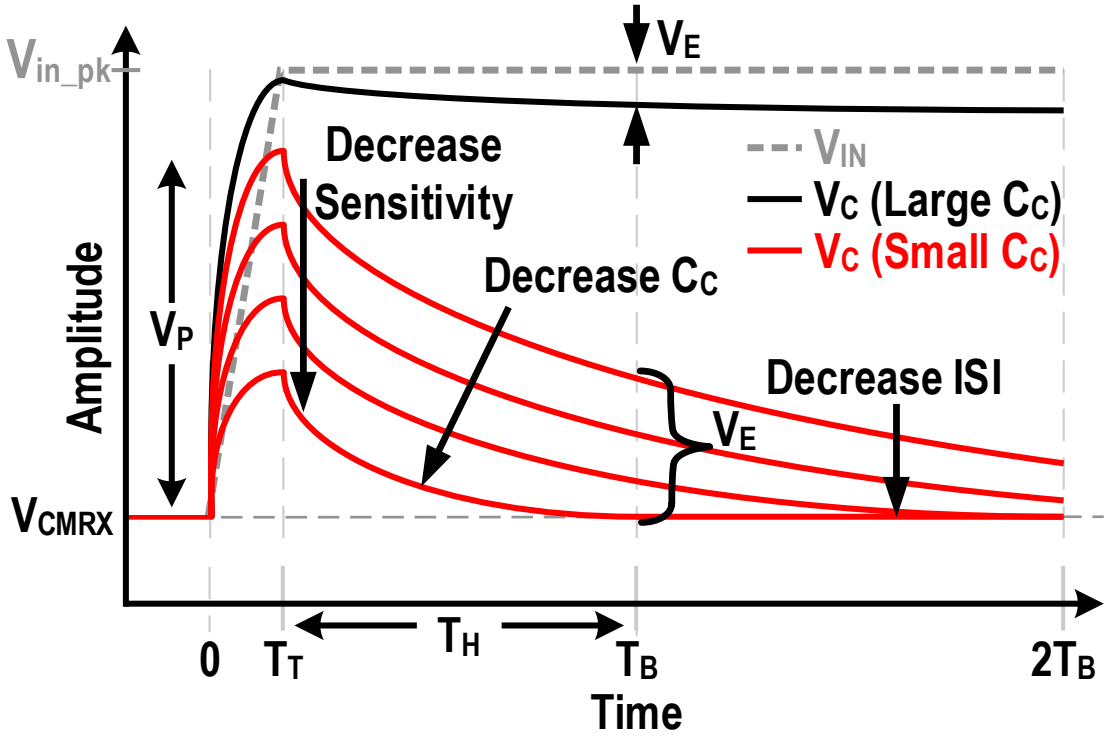

Figure 19 – RZ (red) and PRZ (black) pulse characteristics comparison

large C_C receivers this is an inverse relationship, while in small C_C receivers it is a direct relationship. The differing relationships gives small C_C receivers an inherent advantage over large C_C receivers as data rates and pin density increase. The direct relationship allows continual area and parasitic reduction in advanced technology nodes as smaller C_C are desired.

The size of the C_C not only effects V_E but also V_P. To explore the C_C design space, the high pass input network given in Figure 7, is modeled by (3.1) [28].

$$\frac{V_C}{V_{IN}} = \frac{sR_TC_C}{sR_T(C_C+C_P)+1} \tag{3.1}$$

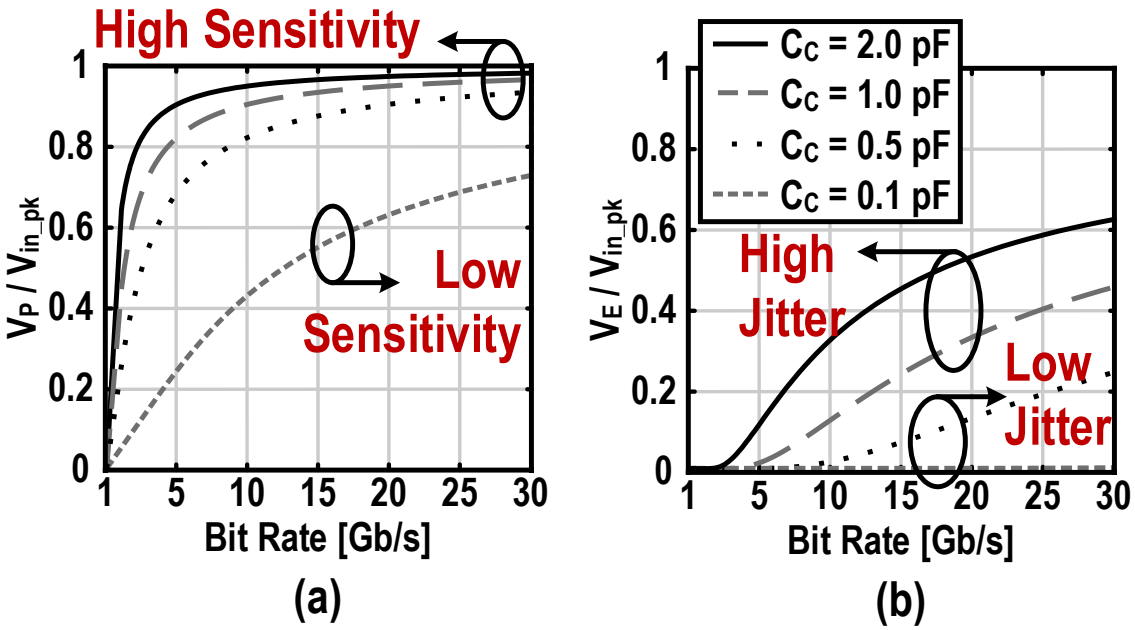

Figure 20 – Normalized coupled signal (a) peak coupled voltage, and (b) residual voltage error, with T_T set to $0.1T_B$

Ignoring the parasitic capacitance (C_P), the coupled input signal is expressed by (3.2) [28] with, *m* being the slope of the input transition ($m = V_{in\_pk}/T_T$), transition time (T_T) being the rise/fall time of the input signal, and time constant ($\tau=R_TC_C$) of the coupled nodes.

$$V_C(t) = \mathrm{u}(t) \cdot m\tau\left(1 - e^{\frac{-t}{\tau}}\right) - u(t - T_T) \cdot m\tau\left(1 - e^{\frac{-(t-T_T)}{\tau}}\right) \qquad (3.2)$$

By evaluating (3.2) at time T_T and T_B, V_P and V_E can be found, respectively [9]. When normalized to V_{in_pk}, the effect of C_C value (assuming $R_T = 50\Omega$) on receiver sensitivity and output jitter is found. As Figure 20 depicts, when C_C is increased, both V_P and the V_E rise, increasing the receiver sensitivity at the expense of ISI jitter. Alternately, decreasing C_C decreases the receiver sensitivity while improving ISI performance. This design trade-off is further exacerbated at higher speeds where a shrinking T_B increases V_E, which ultimately limits the achievable data rate of a given capacitance value due to accumulation

of voltage error and the resulting ISI. Note that this analysis is assuming a T_T equal to 10% T_B. This assumption associates the transitions' frequency content to T_B of the signal. This is typical when transmitters are operated at or near the peak data rate. However, if a transmitter is operated at data rates much less than the peak data a technology can support, a large T_B supports larger pulse widths and this trade-off is relaxed. If the T_T is held constant across data rates, the sensitivity curves become flat and the C_C value can be chosen based on achievable sensitivity and acceptable jitter performance for the desired peak data rate.

In order to maximize peak data rate and minimize BER, the sources of jitter must be minimized. Jitter can be broken down into random jitter (RJ) and deterministic jitter (DJ). RJ is typically the result of noise from resistors and transistors. However, DJ is the result of circuit architecture and chosen components. DJ is measured by collecting the variation in transition timing due to variation in data pattern. In clock-less receivers, once DJ is added to a node it is challenging to reverse. DJ can be significantly decreased, if not eliminated, by re-clocking data streams, increasing area and power consumption. Non-zero V_E values are a measureable value of added DJ. Any V_E value on the coupled nodes will be passed along to the next component and typically amplified. Any amplitude error and will be converted into DJ when converted to rail-to-rail output.

3.2 Input Bias Latching

With an appropriate sized C_C, the bi-polar RZ pulse train generated from the NRZ transitions still requires data manipulation to recover CIDs, as discussed in Section 2.5.4. Data latching is employed to avoid the latency, complexity, power and area penalties

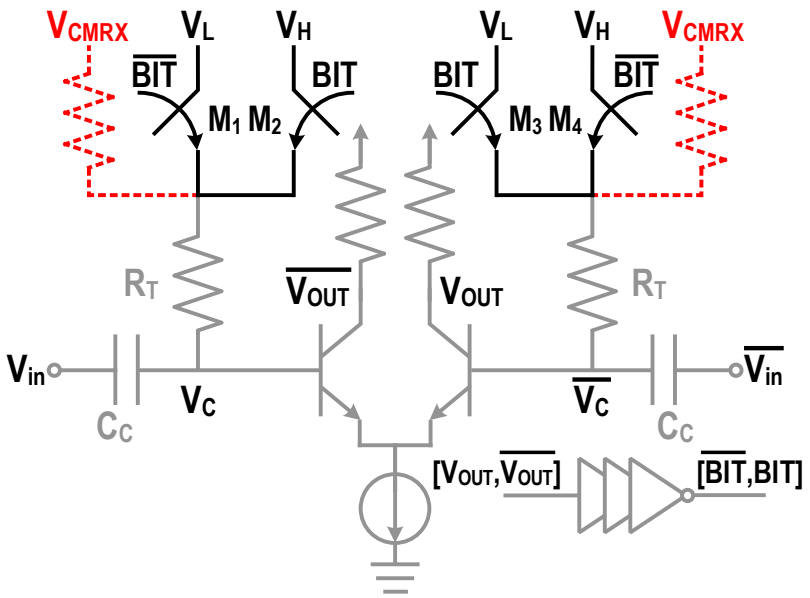

Figure 21 – Capacitively-coupled differential pair with fixed (red) or latched (black) bias schemes.

associated with data manipulation, the data latching is employed. Since the widths of the coupled pulses are constrained to T_B, each bit period can be viewed independently on a bit-by-bit biases. This viewpoint limits the interaction between bit periods to either two cases: equal (CIDs) or unequal (transition). Equal adjacent bit periods contain no frequency content and input is essentially a DC signal, while unequal adjacent bits periods contain high frequency based on the T_T and amplitude of the input signal. Only when sufficient energy is coupled into the receiver to surpass the sensitivity threshold should the output toggle, elsewise the output should hold the previous bit period's value. This is the behavior of the input bias latching implemented.

Figure 21 overlays both a fixed (dashed, red) and latched bias (solid, black) scheme on a capacitively-coupled differential amplifier. The fixed bias scheme applies equal and

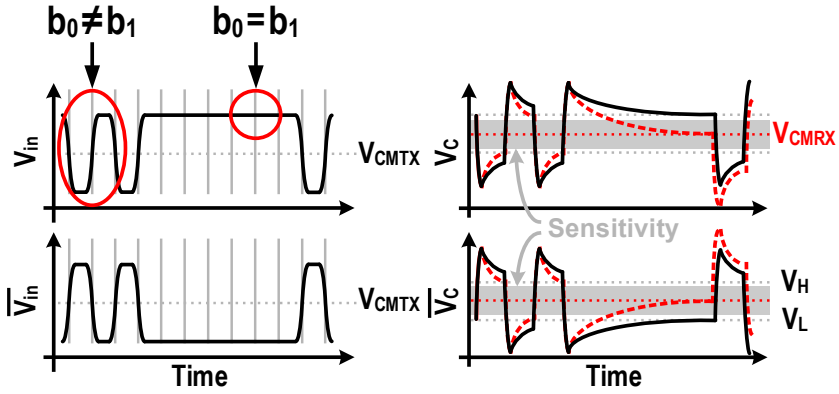

Figure 22 – Waveforms of the input (V_{in}, $\overline{V_{in}}$) and capacitive-coupled nodes (V_C, $\overline{V_C}$) in the presence of a toggling data stream and CIDs

constant voltage biases. The latched bias scheme applies dynamic data dependent biases via two switch pairs (M1-M4). An offset is maintained by digital selection of two bias levels (V_H and V_L). This generates a level of hysteresis in the receiver determined by the bias offset magnitude ($\Delta V = V_H - V_L$) and value of C_C. The switch pair control signals are created by digitally amplifying the differential output, and when combined with inherent connectivity logic creates a balance between positive and negative feedback loops. These digital feedback loops introduce a feedback delay (T_{FB}) equal to the time between an incoming bit transition and application of a new bias state at the coupled input. The result is a self-timed, high-speed, toggled bias latching receiver capable of recovering an indefinite number of CIDs without data manipulation

Figure 22 depicts the input waveforms (V_{in}, $\overline{V_{in}}$) and compares the coupled waveforms (V_C, $\overline{V_C}$) of the fixed and latched input bias schemes. Under both biasing schemes transition bit periods are coupled as pulses and remain outside the receiver's sensitivity region. However, during CID bit periods the fixed bias scheme experiences

rapid signal decay back towards V_{CMRX} and into the sensitivity region. This places the receiver into an ambiguous indeterminate state, which can result in bit errors based on noise and PVT variation. On the contrary, the latched bias scheme ensures the amplifier inputs decays to distinct potentials outside of the receiver's sensitivity region during CID bit periods, assuming ΔV is greater than the receiver's sensitivity. The difference between the biases serves as intrinsic 1-bit memory of the previous bit polarity and eliminates the need of data manipulation circuitry in both transmitter and receiver.

3.3 Pseudo Return-to-Zero Waveform Characteristics

The latched bias scheme in combination with the small C_C coupling on an NRZ data stream signal generates a unique waveform on the differential amplifier input nodes. As discussed in Section 2.5.5, an input network with a small C_C generates a bi-polar pulse train from NRZ data transitions. When the input bias latching is added to the coupled node, a pulse no longer decays to the same potential but to a data dependent potential. This transforms the bi-polar RZ pulse train into a bi-polar PRZ pulse train. A detailed comparison of a RZ and PRZ pulse is shown in Figure 23.

Though different, the original RZ and new PRZ waveforms share fundamental characteristics. The addition of the latched bias switches has minimal impact on the coupled node's RC time constant. Therefore assuming the same coupling network, the RZ and PRZ signal share the same V_P and decay rate values. Figure 23 shows this commonality in addition to highlighting distinct effective settling times. The difference in settling time stems from the digital latching of the incoming signal after digital feedback delay. As Figure 23 depicts, at $t < T_{FB}$ the node is biased to V_L, while at $t > T_{FB}$ is biased to V_H. The

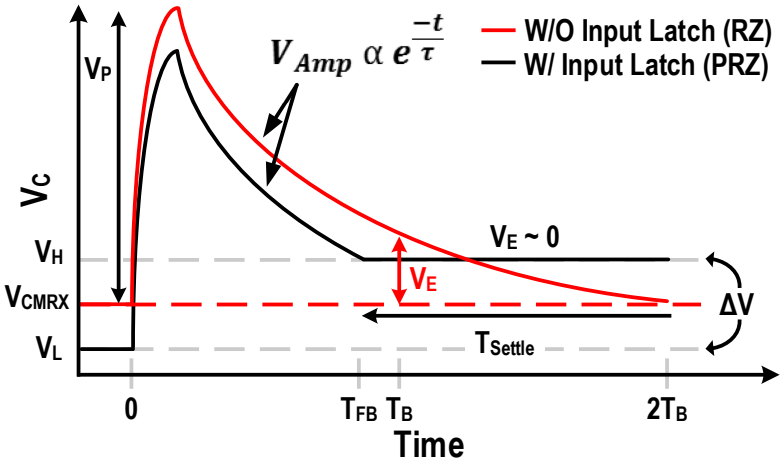

Figure 23 – Comparison of RZ and PRZ pulse characteristics

feedback delay the through digital amplification stages leverages the PRZ pulse exponential decays towards the original bias point (V_L) between time T_T and T_{FB} then receives the new bias at time T_{FB}. The new bias reduces the total charge required to decay from the coupled nodes by the value of ΔV. This can reduce the effective settling time and V_E value by breaking the tradeoff presented in Figure 20, while maintaining the same V_P. Even through V_E is not necessary eliminated, the upper limit of V_E is reduced to $V_P - V_H$. If ΔV is increased, the upper limit of V_E is decreased equally, therefore reducing maximum DJ. This direct tradeoff must be taken into consideration for the specified application's signal swing and jitter requirements.

Figure 24 depicts the output eye diagrams when the RZ and PRZ waveforms are amplified to rail-to-rail digital CMOS levels. The large RZ V_E results in timing jitter and formation of separate overlaid eyes, while the PRZ results in a singular eye. The number of separate eyes is dependent on the number of bit periods a V_E is present for a single pulse. The PRZ eye has only one distinct eye opening due to the inherent V_E reduction enabled

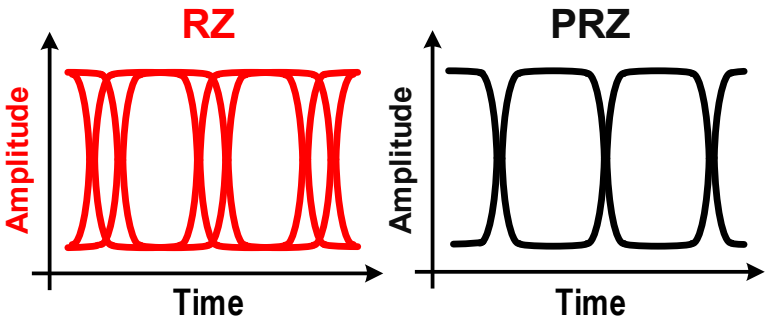

Figure 24 – RZ and PRZ rail-to-rail eye diagrams

by the latched input bias PRZ receiver. This allows the support of higher data rates than RZ input receivers for an acceptable V_E value.

To model this benefit, (3.2) must be modified to include an exponential charge of ΔV starting at time T_{FB}. This addition represents the new latched bias timeframe ($t > T_{FB}$). The PRZ coupled waveform is described by (3.3) with parameterized model provided in Appendix A.

$$V_{C\_PRZ}(t) = V_C(t) + u(t - T_{FB}) \cdot \Delta V\left(1 - e^{\frac{-(t-T_{FB})}{\tau}}\right) \qquad (3.3)$$

The latch biasing has added the ΔV and T_{FB} variables to input coupling network design considerations. Originally, the input coupling network was only a one degree of freedom C_C, which forces the V_P and V_E tradeoff to be navigated. Now with three variable (C_C, ΔV, and T_{FB}) the design space is inflated. To simplify further analysis, $R_T = 50\ \Omega$ is assumed, in order to match coupling channel characteristic impedance. With this assumption, C_C and V_P can be interchanged due to their direct relationship. The latched input bias architecture can achieve functionality with a variety of V_P, ΔV, and T_{FB} values. However, for optimal performance a balance between these three design variables must be achieved. In order to explore the input coupling and bias latching network design space,

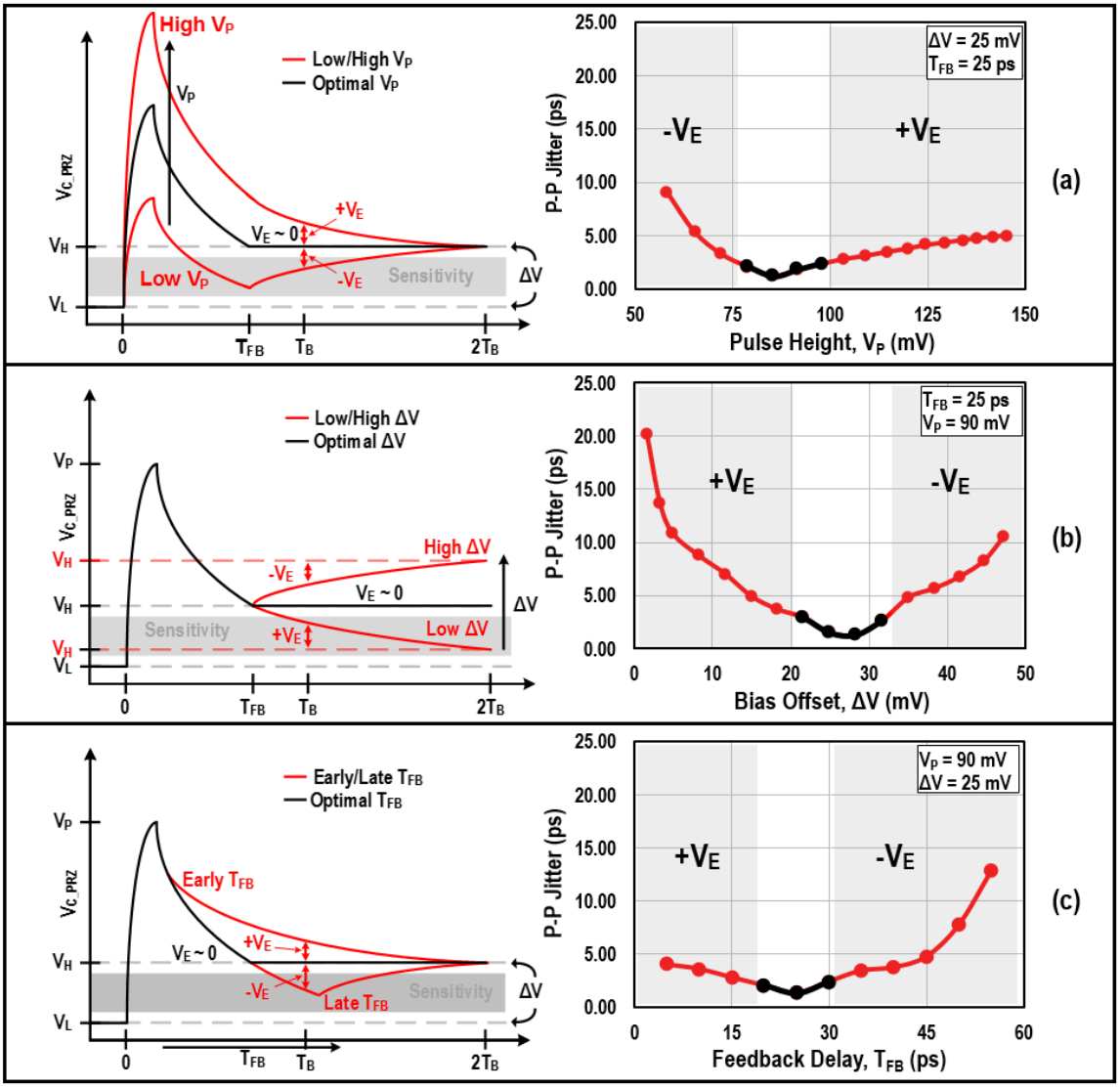

Figure 25 – Coupled PRZ waveforms highlighting the induced V_E and associated simulated jitter

three set of waveforms and simulated data of the receiver presented in Chapter 5 are depicted in Figure 25. The simulations are carried out at 28 Gb/s with (a) varying V_P, (b) varying ΔV, and (c) varying T_{FB}. The input signal is a 100 mV differential (V_P of 90 mV) PRBS15 signal. The p-p jitter performance is used as an analogue for V_E.

The three waveform-data sets portray the effects of individually varying V_P, ΔV, or T_{FB} while holding two variables constant. Due to the addition of offset bias, PRZ waveforms can experience positive, zero and negative values of V_E. Similar to Figure 19, Figure 25 waveforms portray a single transition from a settled low value to indefinite number of high value CIDs. This eliminates the effects of previous bits' ISI and allows isolation of single PRZ pulse behavior. The near optimal (± 20%) region is represented by the black waveform, while the red waveforms represent settling times greater than T_B and respective positive and negative V_E values.

Across all three Figure 25 waveform-data sets, V_E values of near zero are achieved when $V_{C\_PRZ} = \Delta V$ and T_{FB} are coincident with T_{FB} greater than T_T. In order to maximize V_P, $T_{FB} = T_B$ must fulfilled. With these two conditions meet, the three parameters' interdependencies are balanced and high sensitivity with minimal jitter at a given data rate is achieved. While any variation in the three parameters will derogate performance, only large variations will cripple the receiver.

Figure 25 (a) illustrates the effects of varying V_P. Small values of V_P result in the PRZ waveform momentarily entering the sensitivity region prior to the new bias value being applied. This results in a negative V_E value, which requires the latched node to be re-charged back to V_H, increasing settling time. Similar to small V_P cases, large V_P waveforms decay quickly towards the previous bias prior to T_{FB}. Nevertheless, after the new bias is applied, the exponential decay's magnitude slows due to the decreased voltage difference and results in a settling time greater than T_B and a positive V_E. The optimal V_P for the presented data is achieved near 90 mV, representing the case where the coupled

amplitude decays to V_H just as the new bias is applied. The jitter performance trend resembles an exponential curve that is inverted near 90mV. This inversion highlights the PRZ pulse's capability to alter traditional exponential charge limitations.

In Figure 25 (b), ΔV variation is illustrated. A high ΔV case exhibits a similar waveform to a low V_P. However, a high ΔV does not enter the sensitivity region. In a low ΔV case the signal enters and remains in the sensitivity region. The simulated jitter performance across ΔV values shows a primarily symmetric response around a minimum near 25 mV. A large spike in jitter is seen in low ΔV values due to a weak latching effect which can result in bit errors.

Finally, Figure 25 (c) varies T_{FB} from near zero to nearly two T_B. A large T_{FB} case can be associated with both small V_P and a large ΔV due to their comparable waveform profiles. However, a large T_{FB} enters the sensitivity region similar to the small V_P case with resembling performance derogation. A small T_{FB} case mimics the large V_P and small ΔV cases' waveforms, while imitating the large V_P jitter trend as it deviates from optimal.

These likenesses highlight the relationships between the three design parameters. For a given variation in one, a combination of the other two parameters can rebalance the configuration to achieve near minimal jitter performance. However, the given input coupling and bias latching network analysis assumes correct bias latch control signals generation. In the cases that enter the sensitivity region, this assumption may not be valid. This stems from the introduction of glitches into the receiver output and therefore the feedback control signals. The bias feedback loop utilizes digital inverters as high gain stages and has a maximum gain. This maximum gain limits the minimum ΔV needed to

generate a glitch free rail-to-rail operation bias latch control signal. If the pulse decays below this level, an incorrect bias state can be temporarily applied, due to increased switch resistance, introducing excessive amounts of jitter and inevitably bit errors. The ΔV dependence on a fixed feedback loop gain is the reason for Figure 25 (b) peculiar jitter performance trend.

3.4 Enhanced Bandwidth Digital Buffer

Most systems utilizing a high-speed digital data receiver require on-chip digital signal processing of the incoming data streams. CMOS is by far the most popular technology for digital circuitry due availability of highly advanced nodes and ultra-low power consumption. Traditionally this processing is designed and instantiated via standard digital logic cell libraries. While the PRZ latched input bias architecture is capable of receiving NRZ data streams containing indefinite strings of CIDs without data encoding or scrambling, it is not capable of directly interfacing with CMOS standard digital logic cell libraries. Standard libraries require rail-to-rail signals to ensure high signal-to-noise ratio, proper logic, and clocking operation. Unfortunately, the differential amplifier output are not compatible with full-scale CMOS standard cell and resemble current mode logic (CML) signaling. While CML circuitry offer high bandwidths and are compatible with the latched bias architecture, power and area penalties will negate the benefits of the receiver. In addition, CML cells are not readily available like CMOS libraries and require custom design.

To transform the receiver output into rail-to-rail digital signals, pseudo differential digital buffers are utilized. Dependent on the technology and differential amplifier

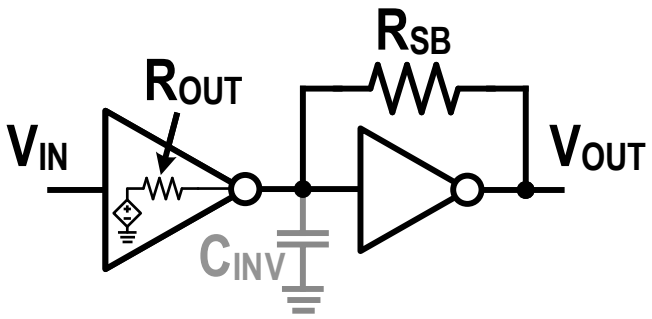

Figure 26 – Enhanced bandwidth digital amplifier block diagram

component sizing, a common mode alignment stage may be required between the differential amplifier and first digital amplifier. Digital inverters are utilized as high gain amplifiers although typically a single inverter does not provide sufficient gain to achieve full-scale operation at high frequencies. Multiple cascaded stages are utilized to achieve required gain to ensure rail-to-rail operation at peak data rate.

Like any amplifier, digital inverters have a limited bandwidth due to technology confines and parasitics. Digital inverters can have gain values in excess of 30 dB at lower frequency, however 3dB bandwidths typically are in the low gigahertz for submicron CMOS technologies. Cascading multiple stages of equal bandwidth amplifiers increases the chain's gain at the cost of bandwidth due to the super imposed non-flat frequency responses of each stage. To combat the decreased cascaded bandwidth, an enhanced bandwidth digital inverter is implemented. The enhanced bandwidth inverter is a combination of a standard digital inverter in series with self-biased inverter, as shown in Figure 26. The addition of a self-biased resistor (R_{SB}) to the second inverter extends the pole of the previous inverter from $\frac{1}{(R_{OUT})C_{INV}}$ to $\frac{1}{(R_{OUT} \,||\, R_{SB})C_{INV}}$. The trade of low frequency gain for increased bandwidth is confirmed by the simulated small signal gain curves, as

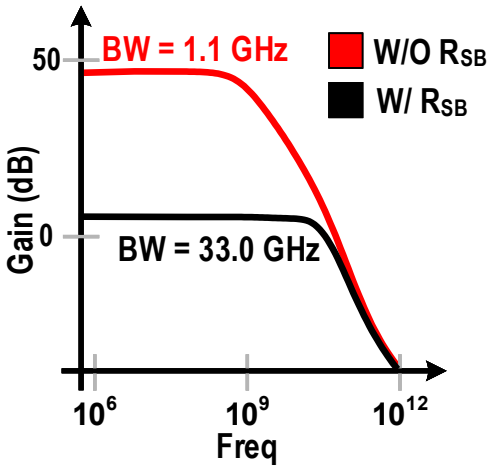

Figure 27 – Enhanced bandwidth digital amplifier small signal response

shown in Figure 27. The decrease in the inverter's gain increases the number of required stages in the pseudo differential output buffers to reliably achieve rail-to-rail operation. The additional stages increase power and area consumption, however without the flat gain of the enhanced bandwidth inverters, standard digital inverters would add excessive jitter and limiting peak data rates.

Non-linear gain is another non-ideal characteristic of digital inverters that limits performance when used as an amplifier. Figure 28 illustrates the linear and non-linear regions of a typical digital inverter's transfer function. The added R_{SB} linearizes the inverter transfer curve by limiting the range of both the input and output nodes. A R_{SB} is only added to the even stages of the output buffer chain in order to avoid multiple feedback paths that can result in instability. In addition, each inverter stage component sizes and layout are mirrored in order to minimize any variation throughout and between the pseudo differential paths. The alternating self-biased stages assist with minimizing mismatch effects by

biasing all the inverter stages in the center of the transfer function curve. This center point, provides the highest most balanced and linear gain of the transfer curve.

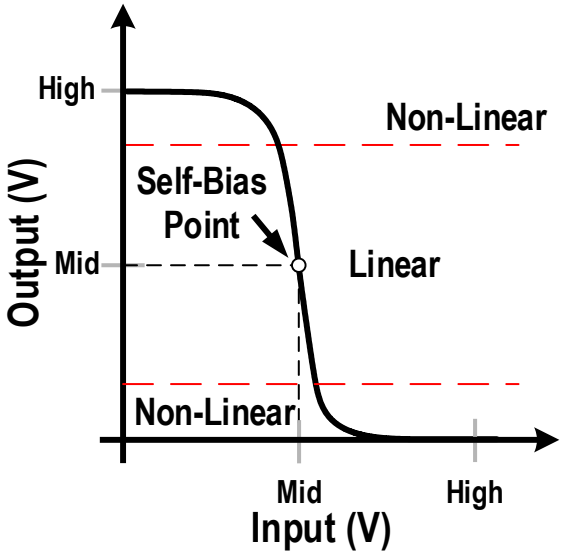

Figure 28 – Standard digital invert transfer function

Chapter 4: Preliminary Work

An existing implementation of the latched bias receiver was realized in a 130 nm silicon germanium (SiGe) BiCMOS technology [9]. This process enables fast (F_t = 200 GHz) SiGe bi-polar junction transistors (BJTs) with low power consumption CMOS on the same substrate.

4.1 130nm SiGe Bi-CMOS Design

This implementation was constructed as a building block for interfacing to high-speed data converters. Data converters are data-error sensitive applications as bit errors would be evident in spurious free dynamic range (SFDR) measurements. It has been implemented in multiple instances [29] [30] [31]. In [29], six parallel data channels (2 Gb/s) employed this architecture, while fourteen parallel data channels (4 Gb/s) were implemented in [30]. In [31], ten data channels (3.35 Gb/s) were utilized. The systems in [29] and [30] were driven by FPGAs, while [31] was driven from test equipment. The dynamic performance measurements of all three converters agreed well with simulation results, demonstrating SFDR > 65 dB from 1-2.25 GHz in [30] and SFDR of > 48 dB from 5-20 GHz in [31]. These levels of performance mathematically confirms the data streams were received error-free.

A standalone implementation of the design was tested operational up to 10 Gb/s. Even though the architecture is proven functional, opportunity for enhancement and

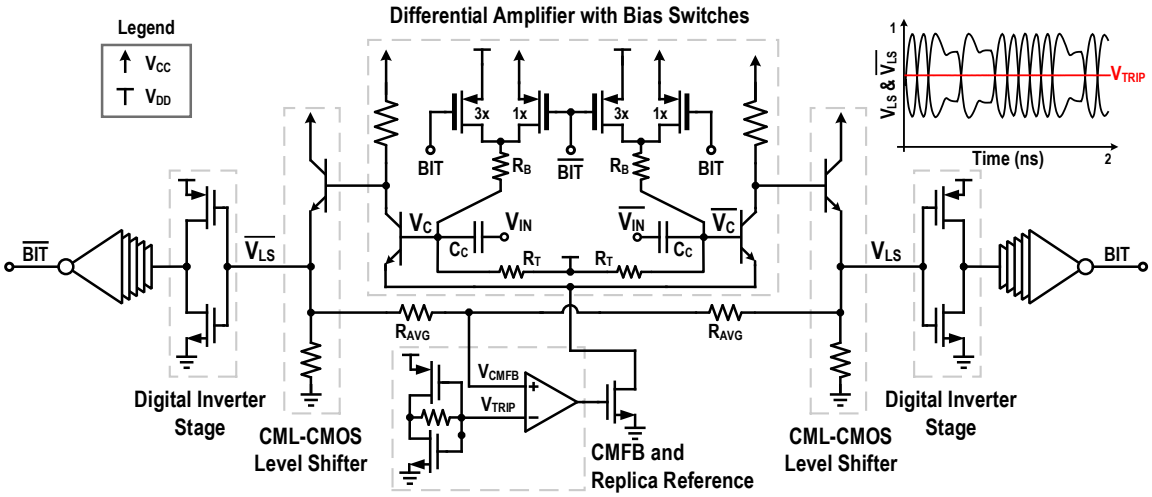

Figure 29 – SiGe BiCMOS latched bias receiver schematic

optimization is present. A schematic of the SiGe BiCMOS design is shown in Figure 29. The following sections describes the receiver's components.

4.1.1 Input Network & Latched Data Biasing

The input stage of the receiver consists of coupling capacitors (C_C), termination resistance (R_T) and latched biasing switches. Metal-insulator-metal (MIM) capacitors of value 1.3 pF was utilized as the coupling capacitors. 50 Ω input termination, per low-voltage differential signaling (LVDS) standard, was implemented via resistive matching network on the coupled input nodes. The bias latching was implemented with two pairs of PMOS transistors, one of minimum and second of three time's minimum width. The pseudo differential digital feedback paths generate the control signals of the bias latches. The bias latch pairs share a drain node that serves as the dynamic bias point while their sources are tied to separate off-chip voltages.

4.1.2 Amplifier and Level Shifter

The core of the receiver is an input amplifier implemented as a common emitter differential pair amplifier. Resistively loaded SiGe BJTs were employed due to the superior F_t and gain compared to the available CMOS transistors. A CMOS transistor was utilized as the tail current source. A compact layout of the amplifier mitigates any mismatches between the differential branches.

The BJT amplifier operates at an elevated voltage rail (1.8V) compared to digital CMOS (1.2V). The difference in voltage rail and amplifier architecture offsets the output common mode outside CMOS compatible levels. For this reason, emitter follower are implemented as CML to CMOS level shifters from the elevated SiGe voltage levels into CMOS compatible levels.

4.1.3 Common Mode Feedback

A common mode feedback mechanism ensures proper biasing across PVT variations. Relatively high (kOhm) resistors (R_{AVG}) average the output of the level shifters with one another. A high gain, low bandwidth differential-to single ended CMOS amplifier compares the averaged node to a self-biased replica of the output buffer's first inverter stage. The self-bias replica inverter establishes the ideal input bias point of the inverter chains. This comparison regulates the amplifier current source and consequently adjusts the amplifier's and level shifters' common-modes to be centered at the first stage inverter trip point. This centering mitigates duty-cycle distortion, therefore reducing receiver jitter as discussed in section 3.4.

4.1.4 Inverter Chain & Digital Feedback

The output of the receiver is designed to achieve full-scale CMOS digital levels. This eases power consumption and increases ease of integration compared to a CML implementation. A digital inverter chain is placed at the output of the common emitter source follower with the purpose of amplifying the low swing signal into a rail-to-rail waveform. The inverter chains are tapped-off after six inverters to create the pseudo differential digital feedback signals. A final inverter is placed between the tapped inverter chains and PMOS bias switches to provide required gain and current drive to toggle the latched bias switches.

4.1.5 Loopback Transmitter

An integrated loopback transmitter enabled independent testing of the receiver. The transmitter was not the focus of the work and therefore power and area consumption were not a concern. However, the receiver's jitter performance needed to be maintained through the transmitter. A CML architecture was utilized due to its high bandwidth, low jitter capability and supporting a multi-stage implementation to step-down a high impedance drive to 50-Ω impedance. The 50-Ω driver is needed to cross PCB transmission lines, test cables and interface with laboratory test equipment.

4.2 Optimization

An investigation of the implemented design uncovered multiple opportunities for refinement. The placement of the termination resistors, number of feedback inverters, output buffers design and coupling capacitance value were analyzed.

The placement of R_T on the input coupled nodes is non-ideal due to the absence of low frequency termination. The impulse response of the channel includes reflections and amplitude jitter without any low frequency termination. A reduction in the number of feedback loop inverters reduces excess gain and delay, while increasing power and area efficiencies. A reduced feedback delay would increase the latching bandwidth and improve peak data rate. The bandwidth of standard CMOS inverters is inferior to the bandwidth of the input amplifier. Substituting the enhanced digital inverters discussed in Section 3.4 would extend these bandwidths and support increased peak data rates.

The large coupling capacitor value was chosen to enhance sensitivity and promote low frequency termination. However, the large size limited peak operational speed of the receiver due to the presence of ISI. To characterize this limitation, Figure 30 presents the simulated eye diagrams of a 2 Gb/s data stream coupled onto a 50 Ω termination resistor through various coupling capacitors (2 pF to 100 fF). Capacitors greater than 1 pF generate enough ISI that the eyes begin to separate, which leads directly to jitter. The standalone design achieved a peak data of 10 Gb/s while implementing a 1.3 pF MIM capacitor. With a 100 ps bit period, V_E values greater than 50% V_P are generated at the coupled nodes, leading to substantial amounts of deterministic jitter at the output. A capacitor value of less than 500 fF would severely reduce the V_E while largely retaining V_P. Unfortunately the optimizations discussed require die manipulation or re-manufacturing the design.

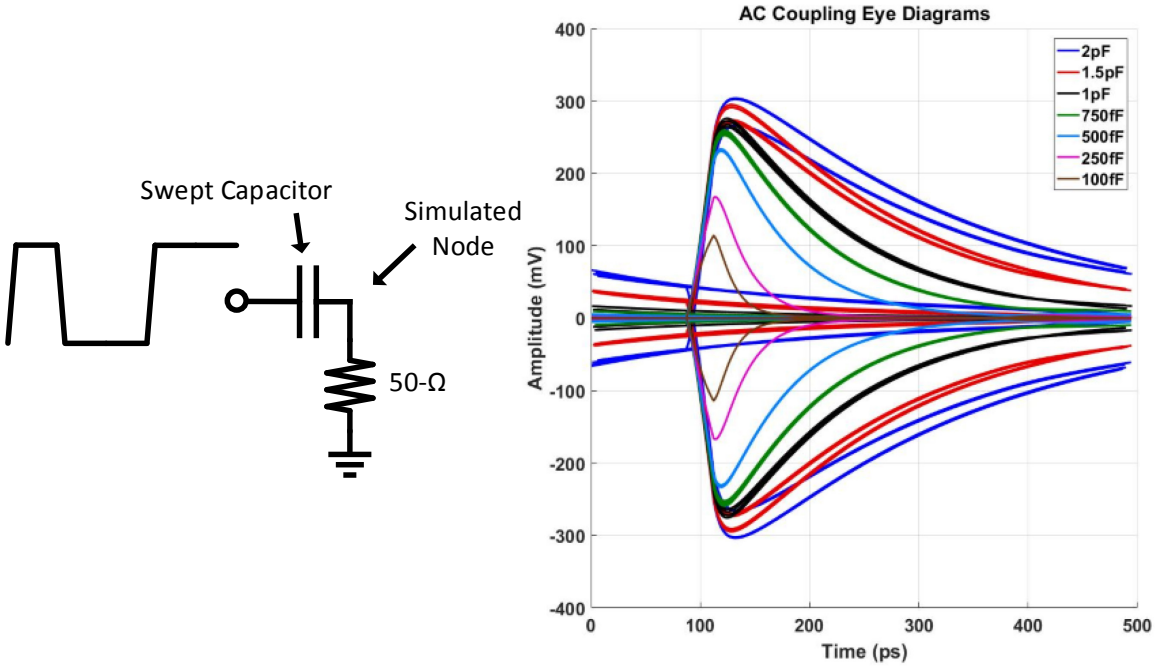

Figure 30 – Eye diagrams of coupled input at 2 Gb/s

4.3 Stud-Bump Repacking and Enhanced Testing

Upon further analysis, the employment of wire-bond packaging was discovered as a possible re-work to improve performance. While wire-bonding provides a fast, reliable packaging method, the addition of a series inductance on all of the pads can limit performance. On the high-speed data pins a series inductance can decrease eye openings via high frequency attenuation. In addition, inductance on bias, power and ground pins can cause voltage droop and ripple on the connected nodes.

In order to decrease the wire-bond inductance, stud bump and flip-chip die attachment were selected as a replacement packing method. Stud bumps mimics controlled collapse chip connection (C4) bumps by replacing long wire bonds with short vertical

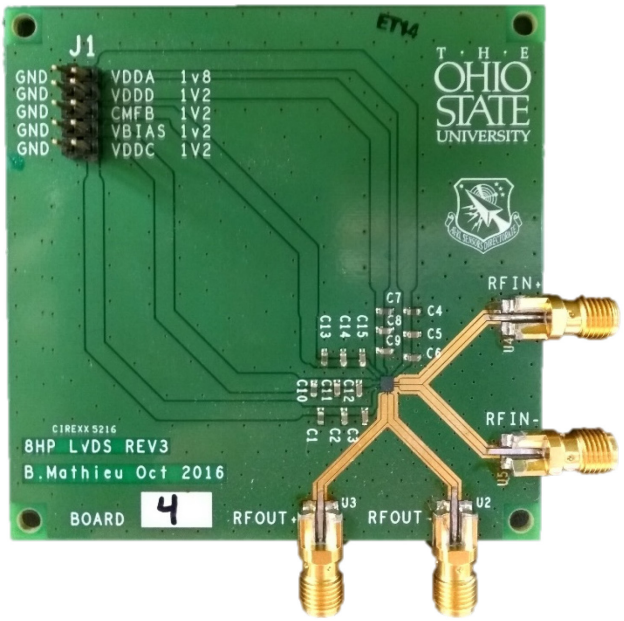

Figure 31 – SiGe BiCMOS stud-bump and flip-chip board

connections. The PCB designed to support stud-bump packing is shown in Figure 31. The 2 mil pad spacing on the existing chip proved to be a challenge in design and fabrication of the board. While wire bonds can fan out between pads on a die to PCB traces, flip chip connections do not have this flexibility. The stud bump PCB designed required 2 mil traces on 2 mil spacing. With the capabilities and expertise of the Air Force Research Lab, Sensor Directorate Microelectronics Packing Laboratory, the stud bump placement and die attachment was successful.

To test the stud-bumped design, phase matched 50 Ω cables connected a Keysight 8195A arbitrary waveform generator (AWG) to the input, while the output was monitored with a Keysight Infiniium Z204A digital signal analyzer (DSA). The use of an AWG allowed the addition of pre-emphases to a PRBS15 data stream in order to compensate for input cable loss. The input and output 2.5cm PCB traces and output cables were not

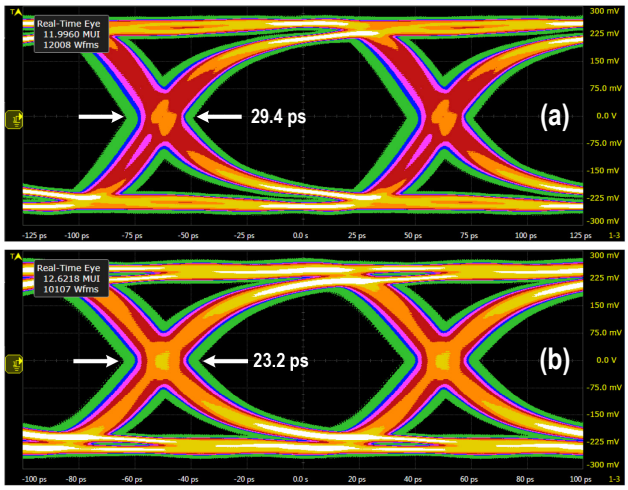

Figure 32 – SiGe BiCMOS measured eye diagrams

included in calibration. Figure 32 shows the measured eye diagrams of the stud-bump board tested under two supply conditions for $V_{CC}/V_{DD:}$ (a) nominal supply 1.8/1.2 V and (b) elevated supply 1.9/1.3 V. Under the nominal supply condition a peak efficiency of 0.46 mW/Gb/s at 8 Gb/s with 29.4 ps p-p jitter was recorded, Figure 32 (a). While under the elevated supply condition a peak data rate of 10 Gb/s with 5.1 mW power consumption and 23.2 ps p-p jitter, Figure 32 (b). The DSA software reported statistical BERs less than 10^{-12} in both modes with bathtub curves shown in Figure 33.

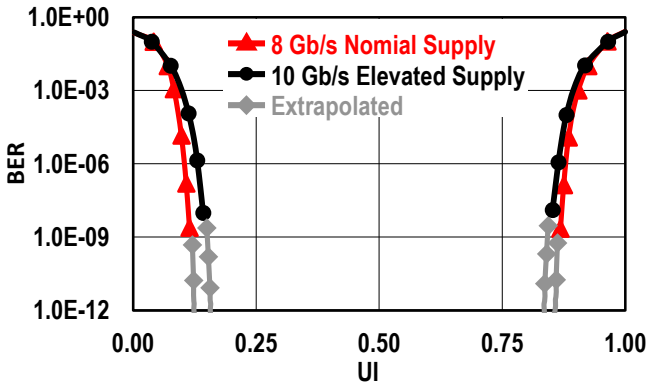

Figure 33 – SiGe BiCMOS measured BER curves

Chapter 5: 45nm SOI CMOS Receiver Design

An implementation of the capacitively-couple PRZ input latched bias receiver architecture is demonstrated in a 45 nm silicon on insulator (SOI) CMOS technology. The shortcomings of the SiGe BiCMOS design are addressed and a CMOS only implementation is established. This instantiation includes broad-band termination, reduced feedback delay, decreased coupling capacitance, elimination of CML-to-CMOS level shifting, and utilization of enhanced bandwidth inverters. The design's block diagram highlighting the included enhancements is shown in Figure 34.

5.1 Circuit Design

The technology chosen for the design is a digital targeted process, with a nominal voltage rail of 1V. This SOI technology provides transistors with and without body

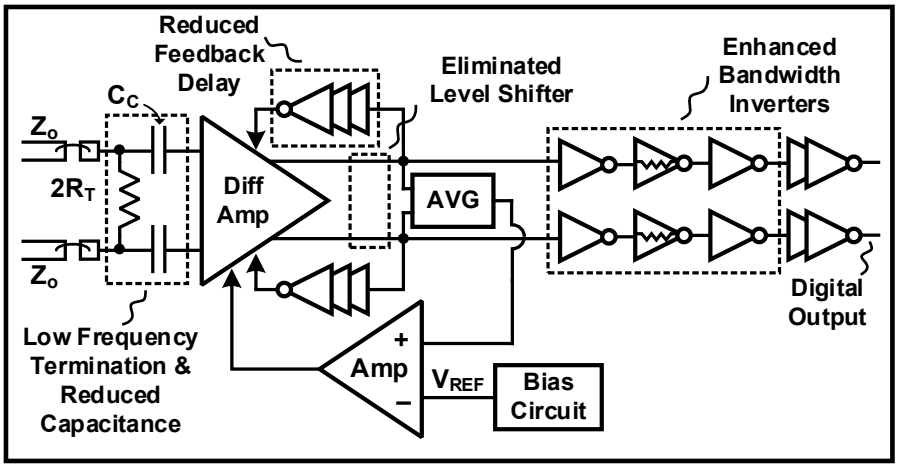

Figure 34 – SOI CMOS receiver block diagram

connections. While the non-connected body transistors have higher F_T and smaller footprint, the V_T of these transistors can be dynamic based on operating conditions. In order to control V_T of all the transistors, the entire receiver design utilizes the body-connected devices. This mitigates jitter as fluctuations in V_T can add deterministic jitter to the signal. By capacitively coupling, the receiver is able to meet and exceed the LVDS common-mode range requirement of over 2-volts, while implementing only 1-volt upper rail. A sensitivity of 100 mV p-p differential was targeted to allow maximum interoperability with existing standards. The following sections describe the design's components.

5.1.1 Input Network & Data Biasing Latching

The input network of the receiver includes resistive termination and 125 fF interdigitated vertical natural coupling capacitors, as shown in Figure 35. The resistive termination is placed on the input nodes as nominal 100 Ω differential configuration. This maintains a large acceptable input common-mode range and provides broad impedance matching to the transmitter and channel, reducing reflections and amplitude modulations of the input signal. With the separation of the termination impedance (R_T) and biasing impedance ($R_H \parallel R_L$), the coupled nodes' time constant ($\tau = (R_H \parallel R_L)\ C_C$) is now independent of termination requirements, allowing greater flexibility and increasing the design space. One opportunity created by this agility is reduction in area via smaller C_C values with larger R_H & R_L values, while maintains the same τ.

The bias latching is implemented using two pairs of bias switches and independent off-chip biases. The PMOS bias switches are sized separately in order to generate the two dynamic bias potentials from the static bias voltages (V_H & V_L). The independent off-chip

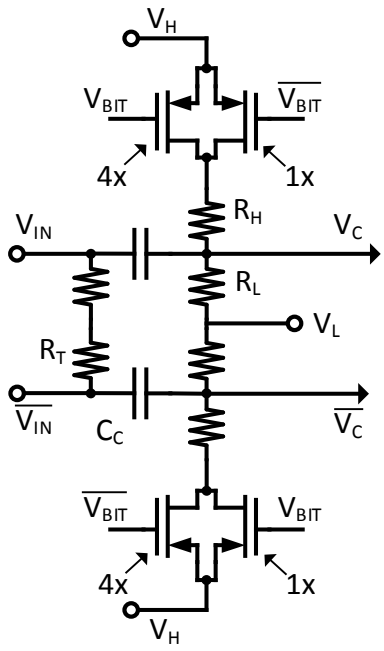

Figure 35 – Input coupling and latched bias schematic

biases provide flexibility in adjusting the latched states' absolute and delta magnitudes during testing and performance optimization.

5.1.2 Differential Amplifier with Common Mode Feedback

A resistively loaded NMOS differential pair with NMOS current source is utilized as the design's core differential amplifier. In the 45nm process, the F_T of a NMOS transistor is over 20% higher than equally sized PMOS. Similar to the SiGe implementation, common-mode feedback is utilized to automatically adjust the current source bias. The differential amplifier with common-mode feedback schematic is shown in Figure 36.

The nominal voltage rail of 1V is used for both the differential amplifier and digital inverters. In addition, the deep sub-micron CMOS limited operating voltages allows the design of a differential amplifier with input and output biases that are similar and even

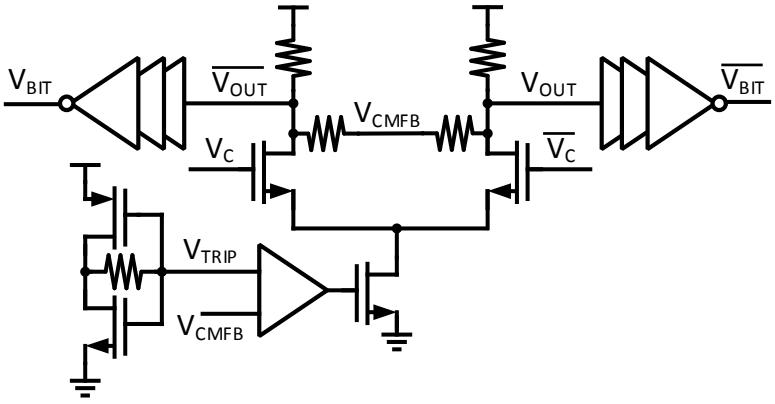

Figure 36 – Input amplifier, digital feedback, and common mode feedback schematic

equal. This also enables the alignment of the differential amplifier nominal output common-mode to mirror the output buffer's first inverter stage trip voltage and eliminates the need for level shifters and associated latency. The CMFB circuit leverages resistive averaging, a self-biased replica reference and a differential to single-ended amplifier. The CMFB compares and automatically aligns the differential amplifier output common-mode with the ideal trip point output buffer's first inverter stage across PVT.

The digital feedback loops are multi-stage digital inverter chains. The three-stages inverts the amplifier output, increases current drive and provides sufficient gain to ensure rail-to-rail bias switch control signals. The amplifier output direct interface to the pseudo differential feedback chains minimize feedback delay with simulation exhibiting a nominal feedback delay of 30 ps.

5.1.3 Digital Output Buffer

A full-scale pseudo differential digital output signal is achieved via the enhanced bandwidth inverters discussed in Section 3.4. Unlike the feedback loop, the delay through the output buffers is not critical in the receiver's performance. For this reason, 3 stages of

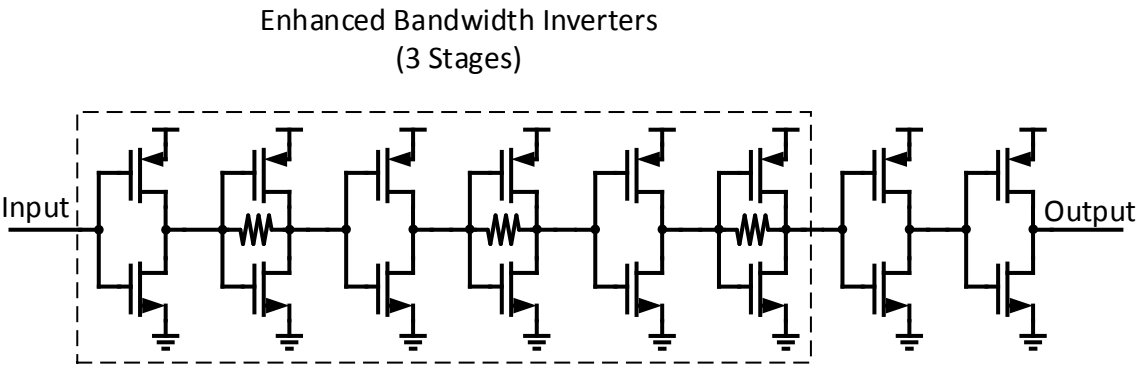

Figure 37 – Enhanced bandwidth digital inverter chain

the enhanced bandwidth inverters followed by two traditional inverter stages construct the pseudo differential output buffers, Figure 37. This construct achieves a flat high bandwidth and high gain frequency response while ensuring rail-to-rail operation at peak data rate. In addition to bandwidth extension, the every other self-biasing method includes duty-cycle mitigation by DC biasing all of the inverters at their ideal trip point.

5.2 Testing & Results

To enable testing of the receiver design, a loopback CML driver was included in the design. The loopback transmitter's power consumption and area is excluded from any measurement due to not being part of the receiver core. The total area of receiver core is less than 0.013 mm^2 and active area less than 0.070 mm^2. A micrograph of the fabricated die is presented in Figure 38.

Custom RF/DC probes are used to characterize the standalone die with a modelled channel loss of 2 dB at 15 GHz. A 200 mV p-p PRBS15 differential bit stream is provided as the input by a Keysight 8195A arbitrary waveform generator (AWG), while the output is monitored by a Keysight Infiniium Z204A digital signal analyzer (DSA). Data receivers are typically tested with PRBS31 data streams to replicate the probable conditions

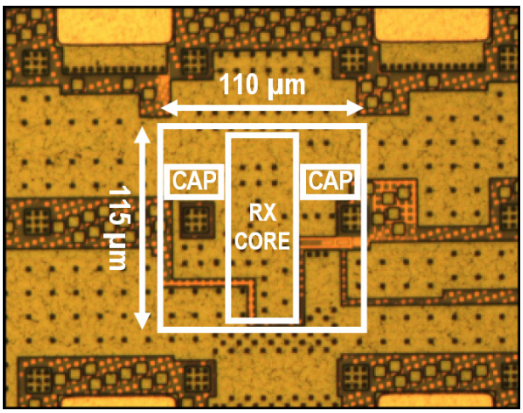

Figure 38 – SOI CMOS die micrograph

encoding and scrambling generate. This verifies performance under a wide variety of conditions from toggling bits to large numbers of CID. Unfortunately the AWG utilized bounded testing to PRBS15 due to memory limitations. However, simulation shows PRBS15 data sufficiently stresses the proposed architecture due to the rapid PRZ signal decay and latching. This results in minimal added ISI when the receiver is presented with CID lengths greater than 15. Figure 39 illustrates the simulated p-p jitter trend approaches an asymptote near 7 ps as the PRBS length increases.

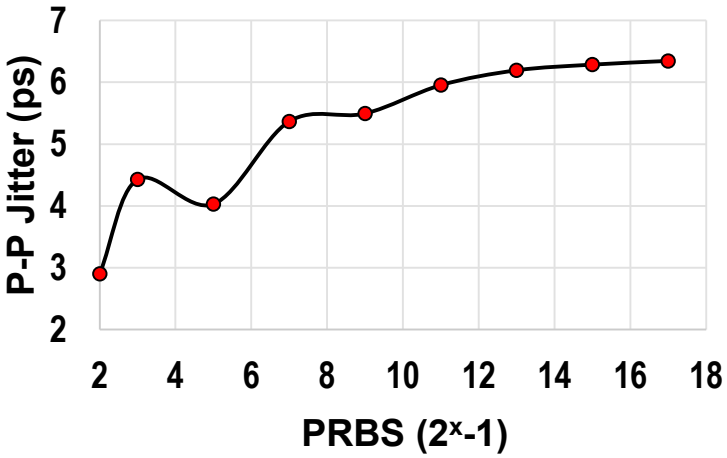

Figure 39 – Simulated p-p jitter verses PRBS length

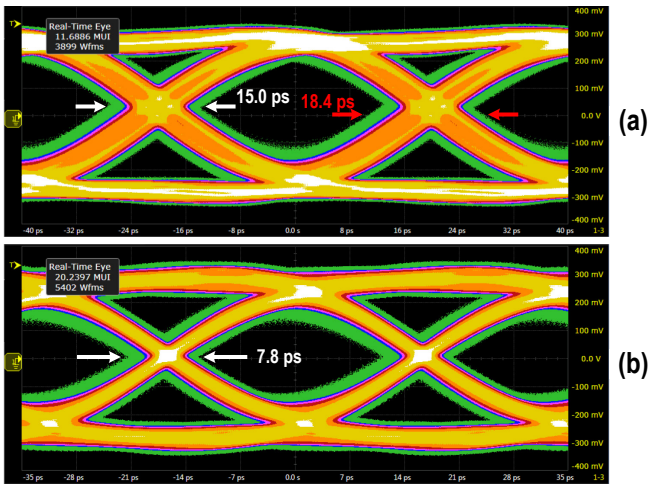

Figure 40 – SOI CMOS measured eye diagrams

Performance is measured under both the nominal- (1.0V V_{DD}) and an elevated-supply (1.3V V_{DD}) conditions. In the nominal-supply condition, the design achieves 15.0 ps p-p jitter at 24 Gb/s with a peak efficiency of 0.25 mW/Gb/s. An eye diagram from this test condition is shown in Figure 40 (a). In the elevated-supply condition, the maximum bit rate is extended to 30 Gb/s while generating only 7.83 ps p-p jitter and consuming 12.0 mW; the corresponding eye diagram is given in Figure 40 (b). Figure 42 depicts the close agreement between simulated p-p jitter data with measured peak efficiency and data rate

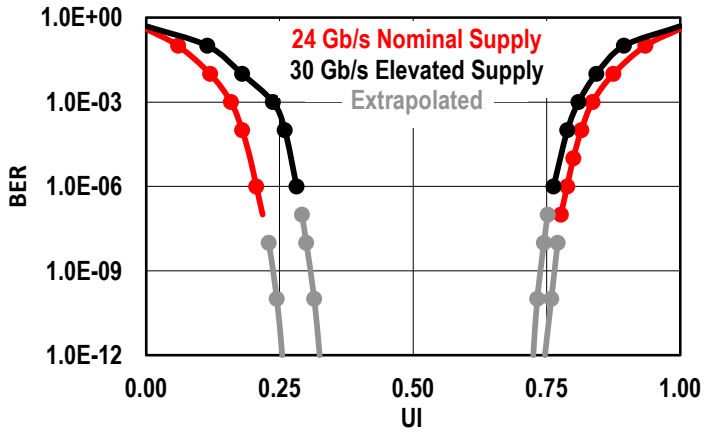

Figure 41 – CMOS SOI measured BER curves

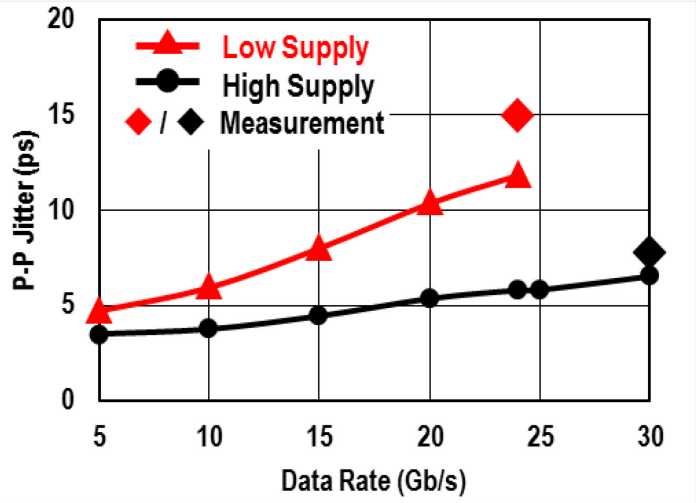

Figure 42 – Simulated p-p jitter of the CMOS SOI receiver vs. data rate with peak power efficiency and data rate measurements comparison

points. The bit-error-rate (BER) curve for both supply modes is given in Figure 42, with the DSA reporting a statistical BER of less than 10^{-12}. It should be noted, in the nominal-supply condition at 24 Gb/s, the output signal includes a differential offset which increases the p-p jitter at the zero-crossing to 18.4 ps, as shown in Figure 40 (a). With this adjustment, the eye diagram and BER bathtub curve are in close agreement. Additionally, the measured

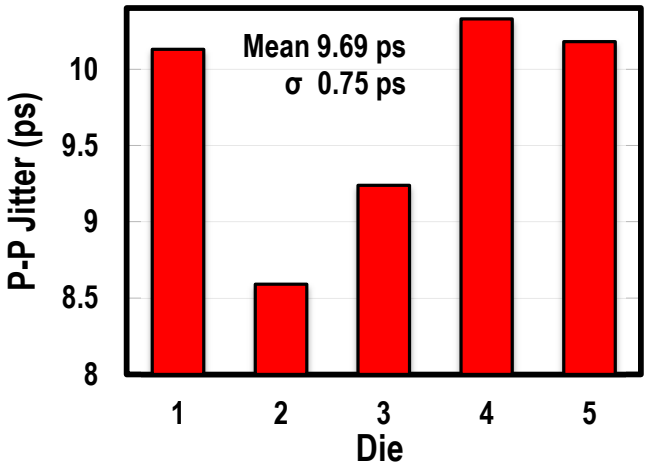

Figure 43 – P-P jitter measurements of five separate CMOS SOI die at 28 Gb/s

p-p jitter five die tested at 28 Gb/s is depreciated in Figure 43. The receivers' p-p jitter ranges from 8.6 ps to 10.4 ps with a mean of 9.69 ps, $\sigma = 0.75$ps.

5.3 Comparison

Table I summarizes the receiver performance and compares it to other high-speed receivers that utilize on-chip capacitive coupling. For full transceiver designs, only the receiver values are cited, where possible. The SiGe BiCMOS version of the architecture, compares favourably in efficiency and area despite the data-rate lagging recent works. Its lower speed performance primarily owing to the slower switching speed of full swing 130 nm CMOS inverters available in the SiGe BiCMOS technology. With the move to the CMOS SOI technology and the improvements listed in Section 5, the proposed architecture achieves comparable data-rates to the cited works while having the smallest active area footprint. Additionally, the CMOS SOI receiver achieves the highest power efficiency among all receivers that do not require data encoding. Normalizing for differential signalling, the design achieves the best-reported power and area efficiency. This work is the only effort preforming the latching at the coupled input node of the receiver and maintains a truly AC coupled interface.

Table 1 – Comparison of AC-Coupled Data Receivers

		This Work†				JSSC06† [13]	VLSI07† [25]	TCASII14 [27]	JSSC14 [10]	JSSC16 [32]	JSSC16 [8]
Technology		**130 nm SiGe BiCMOS**		**45 nm CMOS SOI**		180 nm CMOS	90 nm CMOS	65 nm CMOS	32 nm CMOS SOI	14 nm CMOS	28 nm CMOS SOI
Coupling	Type	**AC On-Chip**				AC On-Chip	AC On-Chip	AC On-Chip	DC / AC On-Chip	AC/ Pad-to-Pad	DC / On-Chip Cap. Term.
	Value	**1.3 pF**		**125 fF**		150 fF	80 fF	1 pF	105 kΩ / 2 pF	N/A	30 pF
Signaling		**Differential**									Single-Ended
Encoding Req.		**No**									Yes
Die Area [mm^2]		**0.012[1]**		**0.007[1]**		0.043[1]	0.045[1]	0.20[1]*	0.7[2]	0.045[1]	0.011[1]
Supply Condition		**Low**	**High**	**Low**	**High**	3	14	32 (4 Ch.)	32	32 (4 Ch.)	20
Aggregate Data Rate [Gb/s]		**8**	**10**	**24**	**30**						
Power Eff. [mW/Gb/s]		**0.46[1]**	**0.51[1]**	**0.25[1]**	**0.40[1]**	3.33[1]	2.29[1]	0.58[1A]	21.1[2]	1.05[1B]	0.17[1BC]

† Clockless RX [1] RX Only [2] RX & TX * Estimated
[A] EQ (Analog) & Clocked Sampler
[B] Excludes Clocking Power
[C] Req. DC balanced data, includes deserializer

Chapter 6: Conclusion

6.1 Work Summary

In this work, a fully integrated, low power, high-speed, area efficient capacitively-coupled, pseudo return-to-zero input, latched-bias data receiver is presented. The architecture is capable of receiving arbitrary NRZ data streams including an indefinite number of CIDs without encoding or scrambling while minimizing deterministic ISI and baseline wander. The on-chip strictly capacitive coupling scheme eliminates the need for board mounted components while enabling a large acceptable input common-mode range limited only by the capacitor breakdown voltage. The placement of bias latches on the coupled input nodes generate PRZ signals that intrinsically include a 1-bit memory of the previous bit's polarity. The PRZ waveform characteristics and model is conveyed and establishing only a balance of design parameters offers optimal performance. The self-generated, full-scale, bias switch control signals enable area and power efficient high-bandwidth data latching while multi-stage enhanced bandwidth digital output buffers offer direct interfacing with standard digital cells.

Two implementations of the architecture and respective testing are given. The first in a 130 nm SiGe BiCMOS process which attained a maximum data rate of 10 Gb/s, while a peak efficiency of 0.46 mW/Gb/s is achieved at 8 Gb/s. The other in a 45 nm SOI CMOS technology that is capable of sustained data rates up to 30 Gb/s, with peak efficiency of

0.25 mW/Gb/s is obtained at 24 Gb/s. Both the implementations exhibit BERs of $< 10^{-12}$ with PRBS15 data with peak-to-peak amplitudes as small as 100 mV. The active areas, including on-chip coupling capacitances, occupy 0.012 mm^2 and 0.007 mm^2, respectively. This architecture is suitable for short, localized board-level, stacked-die, and heterogamous integration applications and benefits from technology scaling.

6.2 Future Work

As the digital age matures, communication and computation demands will continue to push digital chip-to-chip links to new technologies and standards. One evident change to support increased data rates is the emergence of four (4) level pulse-amplitude modulation (PAM-4). PAM-4 signaling doubles the bit rate of NRZ while maintaining the same baud rate and therefore signal bandwidth. While NRZ signals exhibit three bit-to-bit relationships, a PAM-4 signal exhibits seven bit-to-bit relationships and due to this increase in complexity many current PAM-4 receivers are multi-bit ADC and digital signal processing based. The demonstrated PRZ receiver could be expanded to support PAM-4 by arraying the receiver core threefold and the addition of digital logic to decode the bias latch control signals. Possible solutions that would enable decoding the tri-level bi-polar pulses are varied sensitivity per each core, via fixed or dynamically sized capacitors or gain, or an intrinsic logic state machine that tracks data output values based on received pulse height and polarity. In addition, possible state mismatches between transmitter and receiver could result in large number of bit errors. To avoid these mismatches, the transmission of a training sequence could exercise all seven transitions to ensure

coordination between transmitter and receiver. Furthermore, signal-to-noise ratio reduction inherent to PAM-4 signals makes the expansion to an AC coupled PAM-4 non-trivial.

The burden of PAM-4 may be needed to avoid additional signal bandwidth over lossy channels, however short low-loss chip-to-chip interconnects can support continual increases in data rates. As the presented implementations demonstrate, a realization of the PRZ receiver architecture in even more advanced CMOS technology could increase peak data rates. However, the shrinking bit periods would further test the feedback loop optimization. One direction that would expand latching bandwidth is the removal of the digital inverters and bias switches latencies. With these eliminations, the feedback would loss digital characteristics and assume an analog behavior. This analog feedback would remove the analog-to-digital and digital-to-analog conversion and accompanying quantization noise. Less injected noise would increase suitability for PAM-4 applications and support increased data rates.

Another emerging trend in high density chip-to-chip links are single-ended interconnects. Modest transmitters and receivers footprints can dwarf minimum pad area resulting in low utilization near I/O pads. In the presented form, both PRZ receiver implementations utilize differential signaling and benefit from the readily available dual polarization of the signal. Single-ended operation is inherently supported by the architecture where low common-mode noise and high signal-to-noise ratio can be guaranteed. However, an exclusively single-ended design could reduce area to support placement directly under a single pad and enable high density I/O limited only by pad density.

Additional developments that would increase the level of integration and expand the application space of the PRZ receiver architecture include on-chip regulation of the static bias voltages and tunable equalization. Instantiation of small on-chip DACs or automatic regulation, similar to the CMFB already employed, could replace the off-chip biases while minimally impacting power and area. The addition of tunable, high frequency peaking to the core differential amplifier would expand the architecture to applications with lossy channels. The addition of high frequency CTLE behavior to the high-speed latching operation would allow a data's full bandwidth to be recovered over a variety of channel responses.

6.3 Final Remarks

AC coupling of digital signals is an enabling methodology for the future of high-speed, high-density chip-to-chip digital communications. The availability of robust and scalable transceiver designs will expedite the development of future highly integrated microsystems leveraging specialized substrates. Flexible interfaces between these dissimilar technologies will reduce risk and allow rapid prototyping with both new and legacy designs. The scope of this effort should not be an indication the capacitively-coupled, PRZ input, latched-bias data receiver architecture is fully matured. As the demand and application space continues to grow, the number of challenging hurdles and innovative solutions will be sure to follow.

Bibliography

[1] Cisco. (2017) The zettabyte era: Trends and analysis. [Online]. Available: Available: https://-www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/vni-hyperconnectivity-wp.pdf

[2] B. Zhang, K. Khanoyan, H. Hatamkhani, H. Tong, K. Hu, S. Fallahi, M. Abdul-Latif, K. Vakilian, I. Fujimori, and A. Brewster, "A 28 gb/s multistandard serial link transceiver for backplane applications in 28 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3089–3100, Dec 2015.

[3] R. Navid, E. H. Chen, M. Hossain, B. Leibowitz, J. Ren, C. h. A. Chou, B. Daly, M. AleksiÄ‡, B. Su, S. Li, M. Shirasgaonkar, F. Heaton, J. Zerbe, and J. Eble, "A 40 gb/s serial link transceiver in 28 nm cmos technology," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 814–827, April 2015.

[4] P. A. Francese, T. Toifl, M. BrÃ¤ndli, P. Buchmann, T. Morf, M. Kossel, C. Menolfi, L. Kull, T. M. Andersen, and H. Yueksel, "A 16 gb/s receiver with dc wander compensated rail-to-rail ac coupling and passive linear-equalizer in 22 nm cmos," in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, Sept 2014, pp. 435–438.

[5] A. Chien, S. H. Hung, K. I. Wu, C. Y. Liu, M. H. Hsieh, and C. C. P. Chen, "A 8.1/5.4/2.7/1.62 gb/s receiver for displayport version 1.3 with automatic bit-rate tracking scheme," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2393–2396.

[6] S. Kimura, "10-gbit/s tdm-pon and over-40-gbit/s wdm/tdm-pon systems with opex-effective burst-mode technologies," in *2009 Conference on Optical Fiber Communication - incudes post deadline papers*, March 2009, pp. 1–3.

[7] Y. S. Wang, M. H. Hsieh, Y. C. Wu, C. M. Liu, H. C. Chiu, B. F. Lin, and C. C. P. Chen, "A 12 gb/s chip-to-chip ac coupled transceiver," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, May 2011, pp. 1692–1695.

[8] B. Dehlaghi and A. C. Carusone, "A 0.3 pj/bit 20 gb/s/wire parallel interface for die-to-die communication," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2690–2701, Nov 2016.

[9] J. J. McCue, "An interleaved multi-mode δσ rf-dac with fully integrated, ac coupled digital input," Ph.D. dissertation, The Ohio State Univeristy, 2015.

[10] G. R. Gangasani, C. M. Hsu, J. F. Bulzacchelli, T. Beukema, W. Kelly, H. H. Xu, D. Freitas, A. Prati, D. Gardellini, R. Reutemann, G. Cervelli, J. Hertle, M. Baecher, J. Garlett, P. A. Francese, J. F. Ewen, D. Hanson, D. W. Storaska, and M. Meghelli, "A 32 gb/s backplane transceiver with on-chip ac-coupling and low latency cdr in 32 nm soi cmos technology," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2474–2489, Nov 2014.

[11] Maxim Integrated, "Spectral content of nrz test patterns." [Online]. Available: http://pdfserv.maximintegrated.com/en/an/AN3455.pdf

[12] D. Friedman. (2016) Subcommittee wireline-2016 trends. [Online]. Available: http://isscc.org/wp-content/uploads/2017/07/ISSCC2016_Trends.pdf

[13] L. Luo, J. M. Wilson, S. E. Mick, J. Xu, L. Zhang, and P. D. Franzon, "3 gb/s ac coupled chip-to-chip communication using a low swing pulse receiver," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 287–296, Jan 2006.

[14] L. Luo, J. Wilson, S. Mick, J. Xu, L. Zhang, E. Erickson, and P. Franzon, "A 36gb/s acci multi-channel bus using a fully differential pulse receiver," in *IEEE Custom Integrated Circuits Conference 2006*, Sept 2006, pp. 773–776.

[15] C. W. Huang, K. J. Liu, Y. J. Huang, M. K. Chen, Y. L. Lin, and M. D. Ker, "Design of ac-coupled circuit for high-speed interconnects," in *2012 IEEE Global High Tech Congress on Electronics*, Nov 2012, pp. 87–90.

[16] O. Viitala and J. Ryynanen, "Chip-to-chip communications using capacitive interconnects," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, May 2010, pp. 2888–2891.

[17] S. Mick, J. Wilson, and P. Franzon, "4 gbps high-density ac coupled interconnection," in *Proceedings of the IEEE 2002 Custom Integrated Circuits Conference (Cat. No.02CH37285)*, 2002, pp. 133–140.

[18] Y. Dong, S. Howard, F. Zhong, S. Lowrie, K. Paradis, J. Kolnik, and J. Burleson, "Ac-coupling strategy for high-speed transceivers of 10gbps and beyond," in *2007 IFIP International Conference on Very Large Scale Integration*, Oct 2007, pp. 84–87.

[19] J. Wilson, S. Mick, J. Xu, L. Luo, S. Bonafede, A. Huffman, R. LaBennett, and P. D. Franzon, "Fully integrated ac coupled interconnect using buried bumps," *IEEE Transactions on Advanced Packaging*, vol. 30, no. 2, pp. 191–199, May 2007.

[20] J. Kim, I. Verbauwhede, and M. C. F. Chang, "A 5.6-mw 1-gb/s/pair pulsed signaling transceiver for a fully ac coupled bus," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1331–1340, June 2005.

[21] P. L. Zador, "Error probabilities in data system pulse regenerator with dc restoration," *The Bell System Technical Journal*, vol. 45, no. 6, pp. 979–984, July 1966.

[22] N. Miura, T. Shidei, Y. Yuan, S. Kawai, K. Takatsu, Y. Kiyota, Y. Asano, and T. Kuroda, "A 0.55 v 10 fj/bit inductive-coupling data link and 0.7 v 135 fj/cycle clock link with dual-coil transmission scheme," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 965–973, April 2011.

[23] M. Kandlikar and I. Jacobs, "Analysis of quantized feedback low-frequency restoration in digital regenerators," *IEEE Transactions on Communications*, vol. 38, no. 8, pp. 1118–1120, Aug 1990.

[24] E. Fang, G. Asada, R. Kumar, S. Hale, and M. Leary, "A 5.2gbps hypertransport integrated ac coupled receiver with dfr dc restore," in *2007 IEEE Symposium on VLSI Circuits*, June 2007, pp. 34–35.

[25] M. Hossain and A. C. Carusone, “A 14-gb/s 32 mw ac coupled receiver in 90-nm cmos,” in *2007 IEEE Symposium on VLSI Circuits*, June 2007, pp. 32–33.

[26] M. Hossain and A. Chan Carusone, “5-10 gb/s 70 mw burst mode ac coupled receiver in 90-nm cmos,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 524–537, March 2010.

[27] T. Kim, S. Jang, S. Kim, S. H. Chu, J. Park, and D. K. Jeong, “A four-channel 32-gb/s transceiver with current-recycling output driver and on-chip ac coupling in 65-nm cmos process,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 5, pp. 304–308, May 2014.

[28] B. L. Mathieu, J. J. McCue, L. Duncan, B. Dupaix, H. M. Lavasani, and W. Khalil, “A capacitively coupled, pseudo return-to-zero input, latched-bias data receiver,” *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2500–2511, Sept 2018.

[29] J. J. McCue, B. Dupaix, L. Duncan, V. J. Patel, T. Quach, and W. Khalil, “A time-interleaved multi-mode ΔΣ rf-dac for direct digital-to-rf synthesis,” in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2015, pp. 103–106.

[30] J. J. McCue, B. Dupaix, L. Duncan, B. Mathieu, S. McDonnell, V. J. Patel, T. Quach, and W. Khalil, “A time-interleaved multimode ΔΣ rf-dac for direct digital-to-rf synthesis,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1109–1124, May 2016.

[31] L. Duncan, B. Dupaix, J. McCue, B. Mathieu, M. LaRue, M. Teshome, M. J. Choe, and W. Khalil, “16.6 a 10b dc-to-20ghz multiple-return-to-zero dac with >48db sfdr,” in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 286–287.

[32] C. Thakkar, S. Sen, J. Jaussi, and B. Casper, “A 32 Gb/s bidirectional 4-channel 4 pJ/b capacitively coupled link in 14 nm CMOS for proximity communication,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 3231–3245, Dec 2016.

Appendix A. MATLAB Pseudo-Return-to-Zero Waveform Model

```
clc; clear; close all; %Reset Enviroment

coupling_caps = [2 1 0.5 0.250 0.125].*1e-12; %Farads
data_rate = [logspace(0,1) [11:1:30]]*1e9; %b/s

vin = 0.2; %input amplitude, volts (normalized=1)
tfb = 30e-12; %feedback delay, seconds
deltav = 0.025; %bias offset, volts
= 85; %bias resistance low bias, ohms
%rb = 79; bias resistance high bias, ohms
time_start = 0; %seconds
time_step = 0.125e-13; %seconds
time_stop = 1e-9+.25e-13; %seconds

t=time_start:time_step:time_stop; %time array

for y=1:1:length(coupling_caps) %loop across coupling cap sizes
for x=1:1:length(data_rate) %loop across data rates

tb = 1./data_rate(x); %calculate bit period
tr = 0.1 .* tb; %calculate rise/fall time
cc = coupling_caps(y); %get coupling capacitor size
m = vin./tr; %calculate transition slope

Vinc_trans = m .* rb .* cc .* (1 - exp(-t./(rb.*cc)));%Coupled input
transistion timeframe (0>t>Tt)
Vinc_decay = -(t>tr).* m .* rb .* cc .* (1 - exp(-(t-tr)./(rb.*cc)))
; %
Coupled input decay timeframe(t>Tt)
Vinc_RZ = Vinc_trans + Vinc_decay; %Fixed bias RZ responce

Vinc_biaslatch = -(t>tfb).* deltav .* (1 - exp(-(t-tfb)./(rb.*cc)));
%
Coupled input latched bias timeframe (t>Tfb)
Vinc_PRZ = Vinc_RZ - Vinc_biaslatch; %Latched bias PRZ responce

Vinc_RZ_data(:,x,y) = Vinc_RZ; %Cumulate RZ pulses
Vinc_PRZ_data(:,x,y) = Vinc_PRZ; %Cumulate PRZ pulses

Vp_RZ(x,y)=max(Vinc_RZ); %Peak coupled amplitude (VP)
Ve_RZ(x,y)=Vinc_RZ(find(t>tb,1)-1); %Voltage error at time TB
(Verror=VE)

Vp_PRZ(x,y)=max(Vinc_PRZ); %Peak coupled amplitude (VP)
```

```
39 Ve_PRZ(x,y)=Vinc_PRZ(find(t>tb,1)-1)-deltav; %Voltage error at time
TB
(Verror=VE)
40 end
41 legend_text(y) = strcat({'C_C = '},num2str(coupling_caps(y)*1e12),
{' pF'}); %
Legend text array
42
43 end
44
45 figure(1) %Plot Normalized VP/Vin
46 hold on;
47 title('Vp/Vi');
48 plot(data_rate./1e9,Vp_RZ);
49 legend(legend_text, 'Location', 'Northeast'); xlabel('Bit Rate
(Gb/s)'); ylabel
('Vp/Vi');
50 hold off;
```

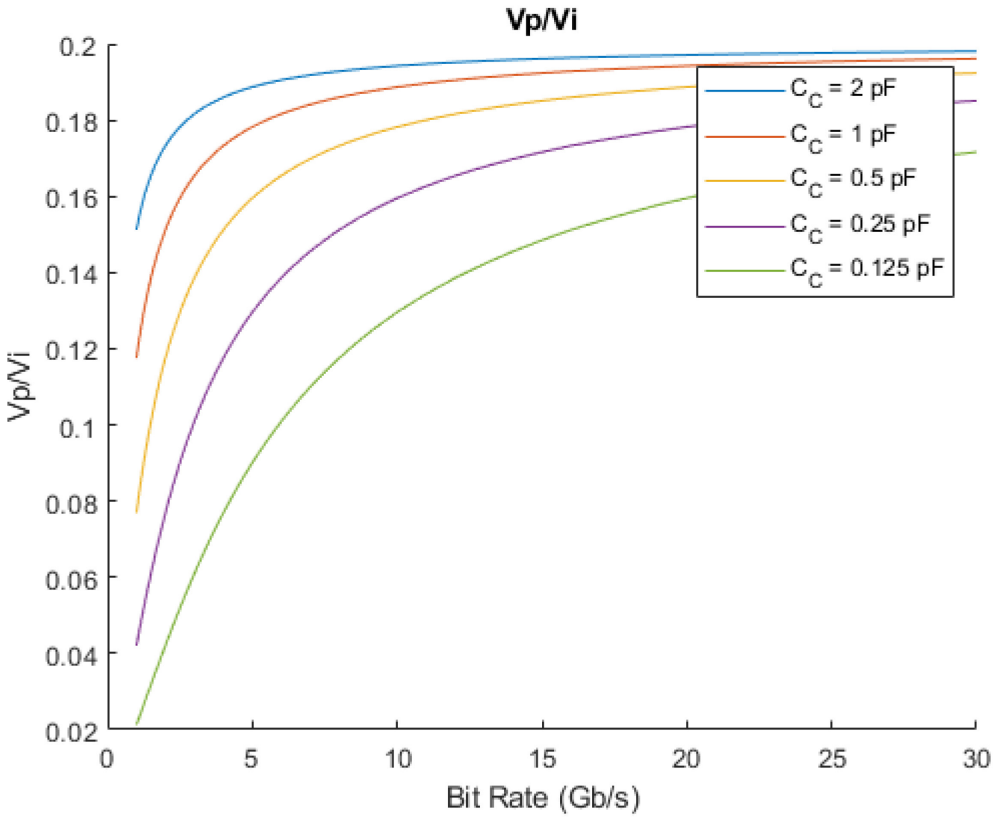

Figure 44 – MATLAB Model Output: Vp/Vi

```
51 figure(2) %Plot Normalized Ve/Vin
52 hold on;
53 title('Ve/Vi');
54 plot(data_rate./1e9,Ve_RZ);
```

```
55 legend(legend_text, 'Location', 'Northwest'); xlabel('Time');
ylabel('Ve/Vi');
56 hold off;
```

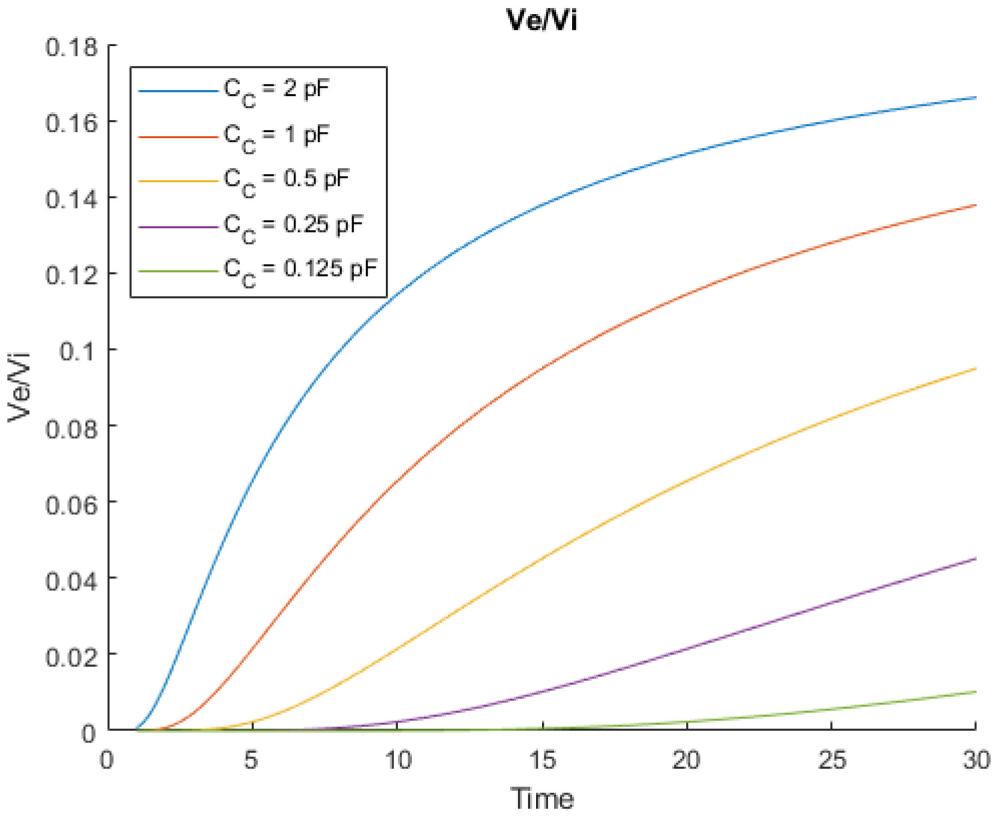

Figure 45 – MATLAB Model Output: V_E/V_i

```
57 figure(3) %Plot RZ Pulses
58 hold on;
59 title('RZ pulses');
60 for i=1:1:size(Vinc_RZ_data,3)
61 plot(t, Vinc_RZ_data(:,size(Vinc_RZ_data,2),i));
62 end
63 legend(legend_text, 'Location', 'Northeast'); xlabel('Time');
ylabel('Magnitude');
64 hold off;
```

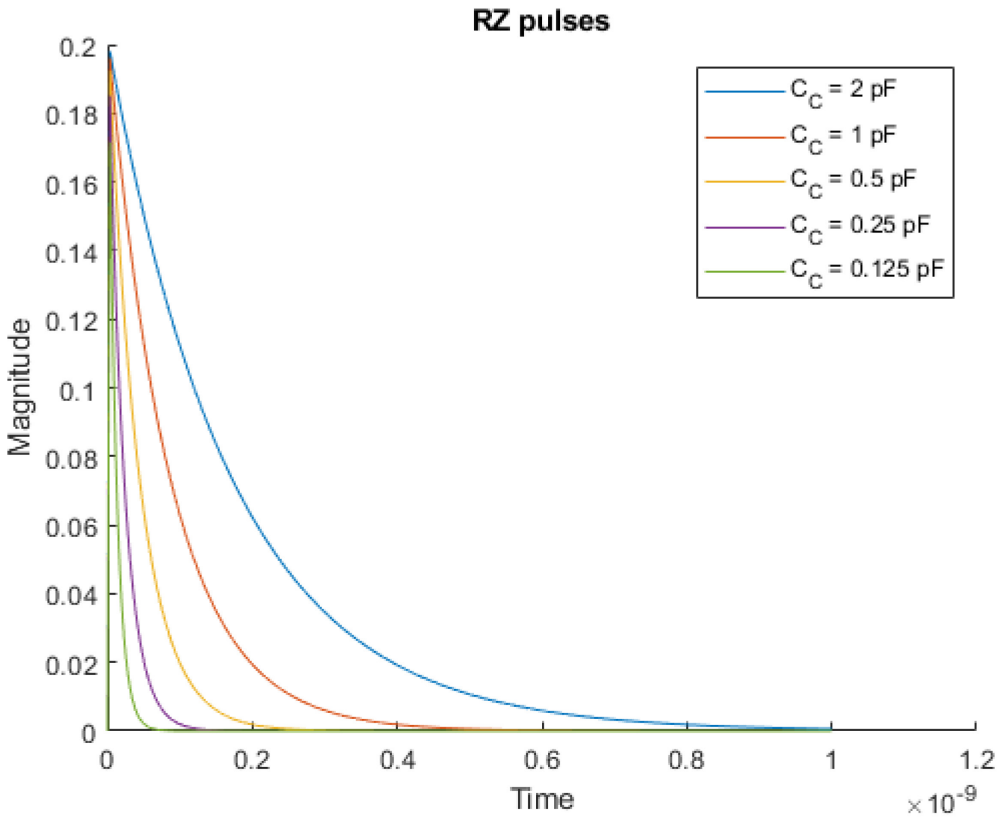

Figure 46 – MATLAB Model Output: Time Domain RZ Pulses

```
figure(4) %Plot PRZ Pulses
hold on;
title('PRZ pulses');
for i=1:1:size(Vinc_PRZ_data,3)
plot(t, Vinc_PRZ_data(:,size(Vinc_PRZ_data,2),i));
end
legend(legend_text, 'Location', 'Northeast'); xlabel('Time');
ylabel('Magnitude');
hold off;
```

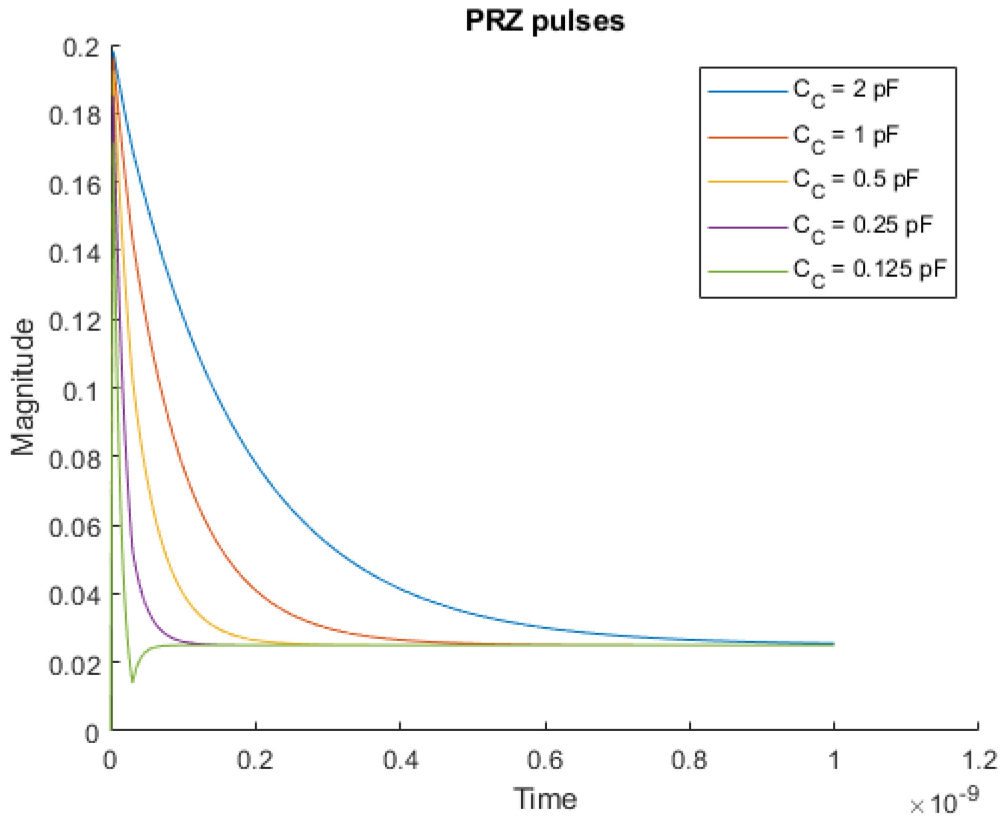

Figure 47 – MATLAB Model Output: Time Domain PRZ Pulses

```
73 figure(5) %Plot PRZ Error
74 hold on;
75 title('PRZ Verror');
76 for i=1:1:size(Vinc_PRZ_data,3)
77 plot(t, Vinc_PRZ_data(:,size(Vinc_PRZ_data,2),i)-deltav);
78 end
79 legend(legend_text, 'Location', 'Northeast'); xlabel('Time');
ylabel('Magnitude');
80 hold off;
```

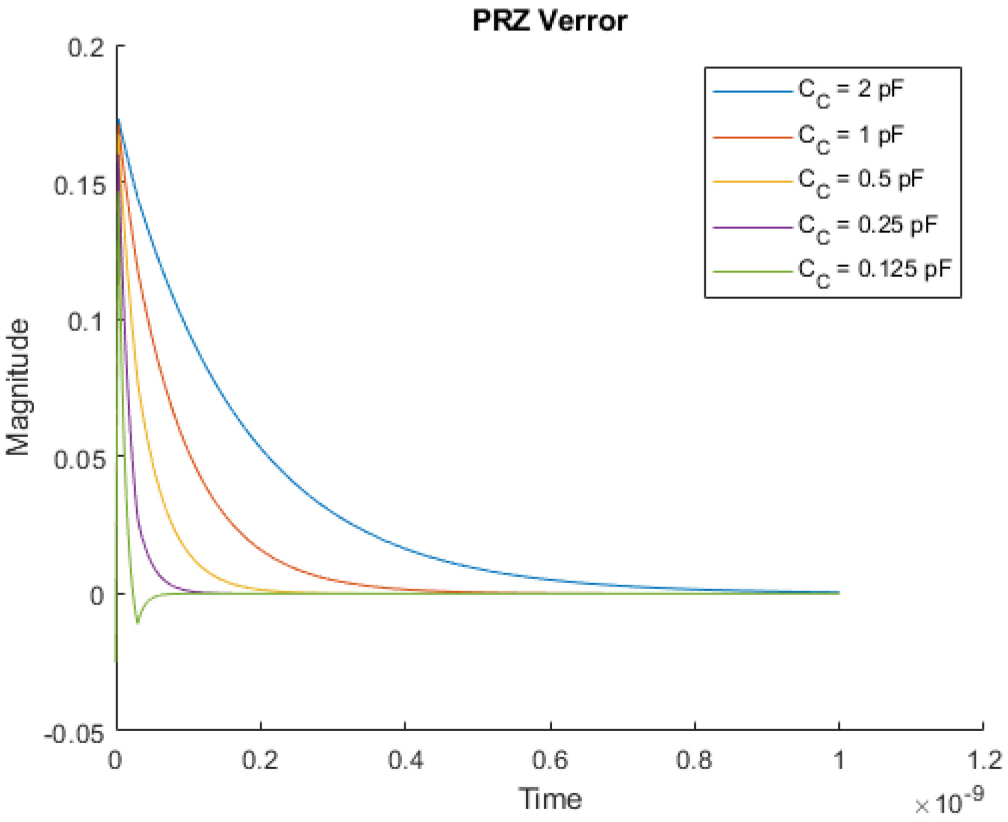

Figure 48 – MATLAB Model Output: PRZ V_E

```
figure(6) %Plot PRZ Error reduction
hold on;
title('PRZ to RZ Error Reduction');
for i=1:1:size(Vinc_PRZ_data,3)
plot(t, Vinc_RZ_data(:,size(Vinc_RZ_data,2),i)-(Vinc_PRZ_data(:,size
(Vinc_PRZ_data,2),i)-deltav));
end
legend(legend_text, 'Location', 'Northeast'); xlabel('Time');
ylabel('Magnitude');
hold off;
```

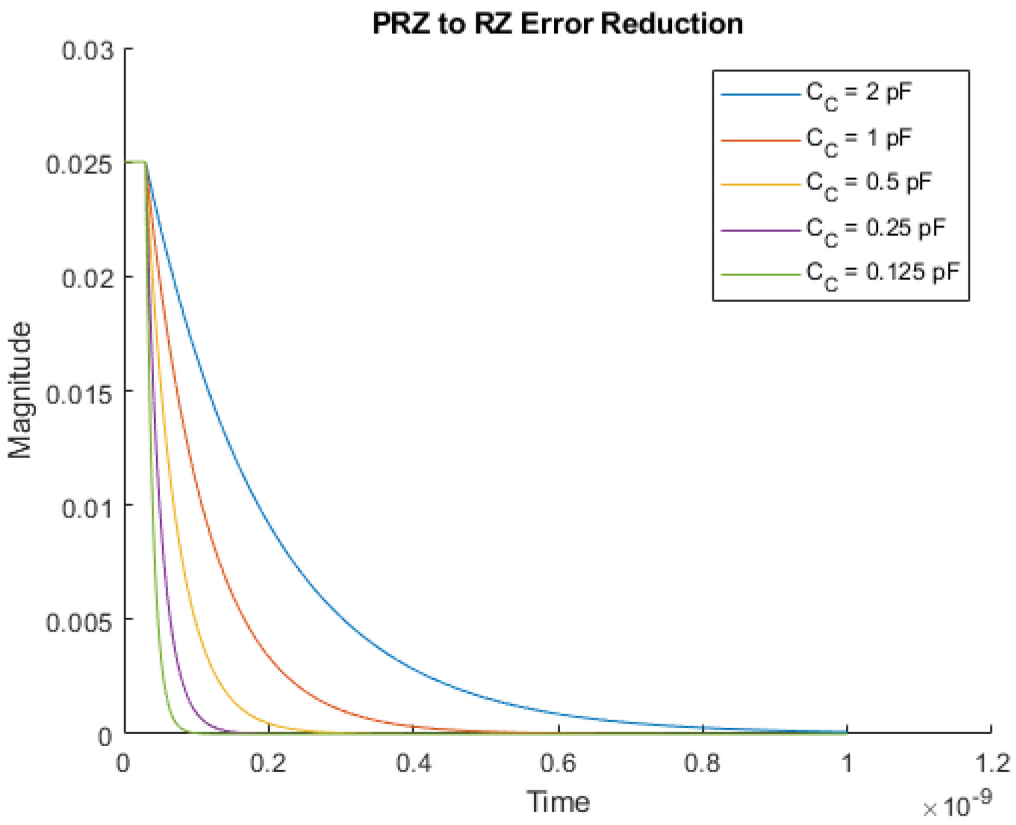

Figure 49 – MATLAB Model Output: PRZ to Rz Error Reduction Magnitude

```
89 figure(7) %Plot PRZ Error reduction %
90 hold on;
91 title('PRZ to RZ Error Reduction');
92 plot(data_rate./1e9,((1-(Ve_PRZ./Ve_RZ))*100));
93 legend(legend_text, 'Location', 'Northwest'); xlabel('Bit Rate
(Gb/s)'); ylabel
('Verror Reduction (%)');
94 hold off;
```

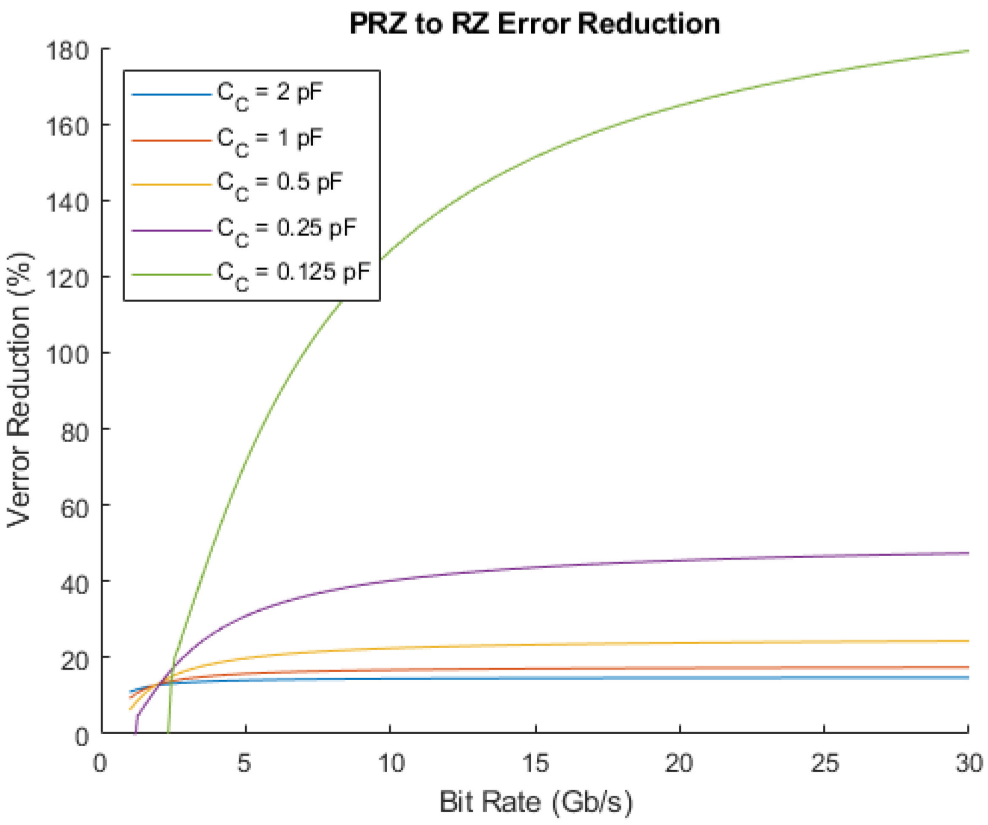

Figure 50 – MATLAB Model Output: PRZ to RZ Error Reduction Percentage