A Self-Oscillating Boosting Amplifier With Adaptive Soft Switching Control for Piezoelectric Transducers

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***Abstract*— This paper describes the design of a high-voltage amplifier for a piezoelectric transducer used in underwater communication applications, which incorporates boosting and signal generation within a single boost converter stage improving the total efficiency of the system. The proposed architecture combines hysteretic ripple current-mode control with an adaptive soft switching technique to achieve improved power efficiency over the full output power range. This is achieved by dynamically controlling the inductor current ripple to keep the converter running in soft switching. The feedback control and the soft switching regulation are implemented in a 0.25 μm 60-V TSMC process with an external power stage. The system achieves a peak efficiency of 85% at 20 W of output power up to 30-kHz signal frequency.**

***Index Terms*— Boost converter, continuous-conduction mode, hysteretic current-mode control (HCMC), minimum power-loss tracking, piezo driver, power efficiency, soft switching.**

I. Introduction

UNDERWATER sensor networks (USNs) have countless detection applications, such as pollution monitoring, seismic activity detection, environmental, and harbour monitoring. However, the development of reliable low power, low cost, and high data rate sensor nodes is a major challenge in the practical implementation of such applications [1]. A typical USN consists of several network nodes spread across an area of interest, where each network node is capable of receiving and transmitting data to the neighbouring network node, as shown in Fig. 1. Apart from problems such as multi-path effects, localization, and propagation delays, limited battery power is also one of the major issues in such systems. Therefore, USN nodes must be energy efficient as battery power is limited and recharging/replacing batteries is usually not practical.

Unlike electromagnetic and optical waves, acoustic waves have relatively low absorption in water and can be generated by using underwater piezoelectric transducers. However, for effective actuation of such transducers, high driving voltages are required (in the order of 10's to 100's of volts). With these battery-powered nodes having limited supply voltage, the requirement of the high voltage for piezoelectric transducers necessitates the use of supply boosting techniques.

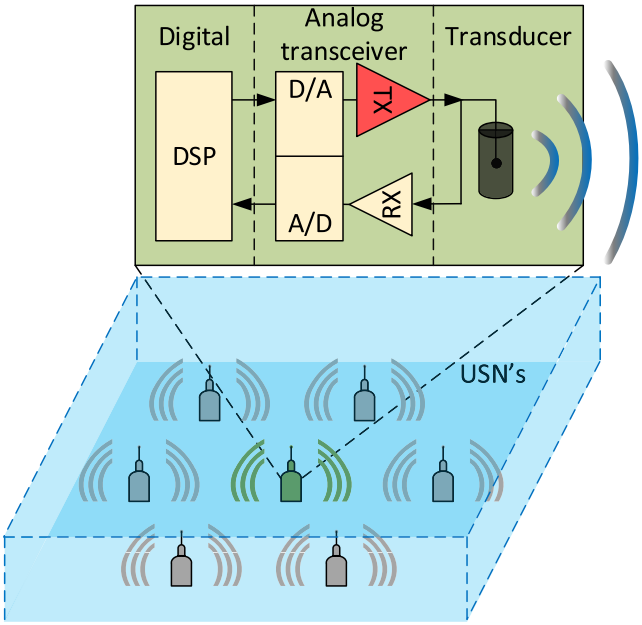

Fig. 1. Typical illustration of USN's with a single sensor.

As compared to some other architectures (like resonant amplifiers), the major requirement for the target application is to achieve a wide bandwidth of 0–30 kHz and high signal swing at the output [2]. Linear amplifiers including class A, B, and class AB can be used to generate the ac signal for actuation of the piezoelectric transducer. However, the inherently low efficiency of these topologies make them unsuitable for battery powered applications.

Over the years, class-D amplifiers (a buck-type converter) have slowly taken over the area of sound generation because of their high efficiency [3], [4]. Despite these advantages, the class-D topology has its own limitations. The maximum signal swing in a class-D amplifier is limited to the supply voltage, and hence cannot effectively drive the piezoelectric transducer with the limited battery voltage. This task is usually achieved by a two-stage solution, normally with a class-D amplifier for generation of dynamic signal and a dc–dc boost converter to increase the supply voltage of the class-D stage. Hence the total efficiency of the complete amplifier is lowered by the boost converter efficiency. Therefore, if the signal generation and the boosting could be performed in a single stage,

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the overall efficiency could be improved with a lower number of components, achieving a low cost solution.

Despite the efficiency advantage, boost converters have not gained significant popularity in direct signal generation in audio applications. This is because of the highly non-linear control-to-output transfer characteristic and the risk of instability due to the presence of a right-half plane zero (RHPZ) for resistive loads, which results in limited bandwidth and high distortion at the output.

In applications involving underwater communication, the maximum distortion requirement of the amplifier depends on the application and the used modulation scheme. Often, the spectral efficiency of modulation schemes for underwater communication is limited because of high noise from ships and waves, as well as time varying channel characteristics that include frequency dependent attenuation, dispersion, Doppler effects, and severe multi-path caused by the seabed and temperature gradients. Compared to audio applications the resulting linearity requirements are less critical. In addition, the presence of the RHPZ at much higher frequencies in capacitive loads such as piezo-electric transducers used for acoustic communication [5], makes the use of a boost converter as a single stage solution an interesting option.

Piezoelectric actuators are available in a wide variety of frequencies and sizes. They are primarily capacitive, with a resistive component that is only present at frequencies where there is good coupling with the water and power transfer occurs. In this paper, we use a general model of the transducer impedance consisting of a parallel RC combination and a decoupling capacitor to block the dc path. The exact values are not specific for a particular transducer, but the operation and performance of the circuit are not dependent on the exact values either.

Several techniques have been developed in the literature to use non-linear converters for direct dc–ac conversion and audio reproduction [6]–[15]. In [6]–[8], a boosting amplifier is proposed, that uses two complementary boost converters with the load connected differentially. Although the cancellation of the second harmonic improves distortion, total harmonic distortion (THD) still remains relatively high.

The concept of pre-distortion, which works by compensating the non-linear parts of the transfer function in such a way that the complete signal transfer becomes linear, has also been reported in [10]–[13]. As the effectiveness of pre-distortion is dependent on the cancellation of the non-linear parts of the control-to-output transfer function, dynamic cancellation becomes challenging and often may require periodic calibration leading to more complexity. A recent approach described in [16], uses a bi-directional boost converter in combination with full bridge to achieve high output voltage swing for a piezo actuator. The system is designed for very low bandwidth and output power, however.

The other technique for reducing distortion is by using feedback. The choice of feedback scheme determines the transient behaviour of the converter. Compared to traditional voltage-mode control (VMC), hysteretic voltage mode control is popular in buck-based converters due to its fast transient response and simplicity [17]. However, this technique cannot be directly applied in boost converters due to the inherent phase difference between the output voltage and inductor current [18]. In comparison to VMC, peak current-mode control (PCMC) as shown in Fig. 2, uses an additional current feedback loop. This makes the system dominantly first order, and thus results in simpler compensation, more bandwidth and cycle-by-cycle current monitoring [19]. However, one of the major problem with peak or valley CMC is the unstable sub-harmonic oscillations occurring when the duty ratio $D > 0.5$. In order to reduce this effect, a fixed artificial slope M_a can be subtracted from the control signal. Fixed slope compensation makes the system stable within a limited range of duty cycles, as less slope compensation can lead to instability and excessive slope compensation reduces the loop gain and makes the system approach VMC operation. Hence, to achieve the good performance over wide duty cycle operation, complex adaptive slope compensation techniques depending on circuit components are required [20], [21]. In addition to linearity, power efficiency is of crucial importance for developing low cost and low power USN's. In high-voltage applications, soft switching can considerably reduce dissipation [22]–[24]. Traditional PCMC does not provide an easy way to keep the converter running in soft switching.

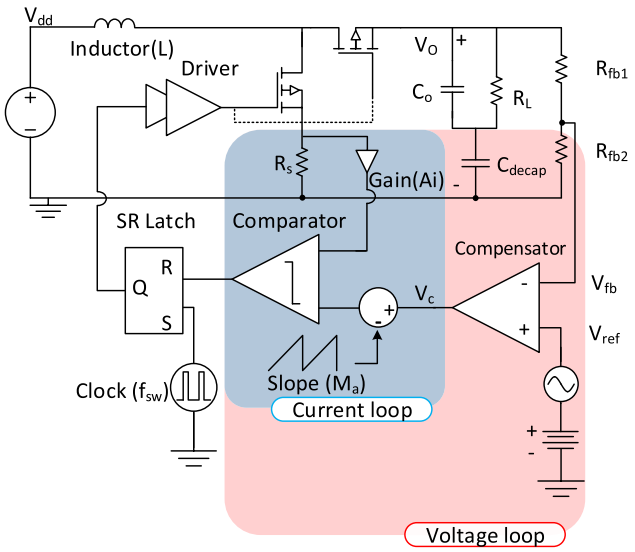

Fig. 2. Peak current mode control scheme.

Therefore in this paper, the key idea is to use a boost converter for direct signal generation in a power efficient way. This is achieved by integrating hysteretic current-mode control (HCMC) (that achieves wide bandwidth and much greater stability) with fast cycle-by-cycle soft switching operation. Section II discusses in detail the proposed control scheme that improves the efficiency and bandwidth. In Section III, the system and circuit realizations are discussed. The proposed strategy is verified by measurement results in Section IV, and finally, the conclusion is described in Section V.

II. Ripple HCMC and Soft Switching Regulation Scheme

In this section, ripple HCMC and the associated soft switching regulation scheme are proposed. The implementation and

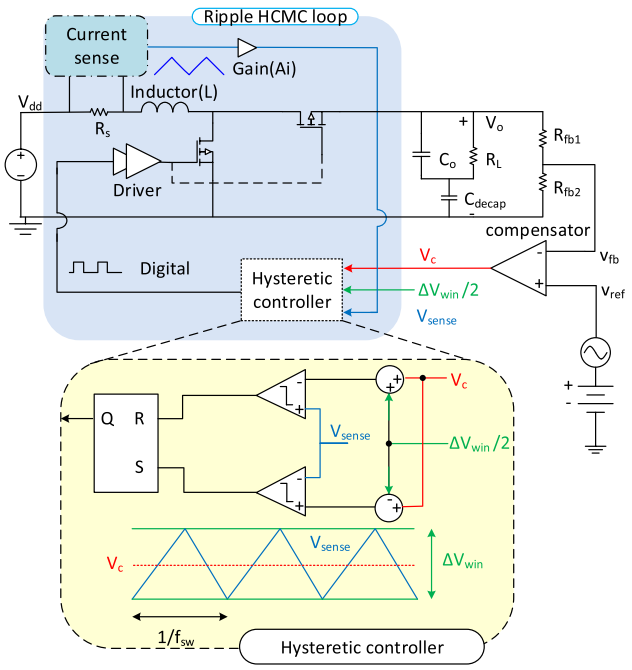

Fig. 3. Ripple HCMC scheme.

advantage of ripple HCMC is described and compared to traditional PCMC in Section II-A. The mechanism of achieving minimum dissipation is discussed in Section II-B and the adaptive soft switching regulation scheme that improves the efficiency is explained in Section II-C.

A. Ripple HCMC

Traditional current mode control schemes have gained more popularity in recent years due to the advantages stated earlier. However, most of the fixed frequency solutions suffer from sub-harmonic stability issues resulting in limited loop gain and bandwidth. The HCMC technique as explained in [25], provides fast transient response, higher loop gain, and better stability than traditional current mode control schemes, as will be shown later. Fig. 3 shows a simple implementation of a ripple HCMC-based self-oscillating boost converter. In ripple HCMC, a fixed voltage $1/2\Delta V_{\text{win}}$ is added and subtracted to the control signal V_c to generate the hysteretic window in which the inductor current oscillates. The sensed inductor current is fed into the controller and the peak and valley crossing points are dependent on the hysteretic window to generate the pulse width modulated (PWM) signal. Compared to a hysteretic comparator implementation as described in [26], a separate error amplifier based structure is chosen here because it helps to control the average current that results in better frequency and voltage regulation [27]. In addition, the noise immunity of the proposed structure with error amplifier is far superior to that of a comparator-based scheme.

Contrary to peak or valley CMC, the switching frequency f_{sw} is not fixed and is given by

$$f_{\text{sw}} = \frac{m_1 * D}{\Delta V_{\text{win}}} * R_s, \quad \{D = 0..1\} \tag{1}$$

where R_s is the sense resistance, m_1 is the rising inductor current slope, D is the duty ratio, and V_{dd} is the supply voltage.

TABLE I
CIRCUIT PARAMETERS

Parameters	Values
Duty ratio (D)	0.5
Inductor (L)	2 µH
Current sense gain for PCMC($R_s \cdot A_i$)	25mΩ∗15
Current sense gain for HCMC($R_s \cdot A_i$)	25mΩ∗1
Supply voltage (V_{dd})	9V
Switching frequency (f_{sw})	1 MHz
Slope compensation (peak-peak)(PCMC)	150 mV
Compensator gain (PCMC)	12
Compensator gain (HCMC)	1
Output capacitance (C_o)	0.47 µF
Resistance (R_L)	1 kΩ
Decoupling capacitance (C_{decap})	50 µF

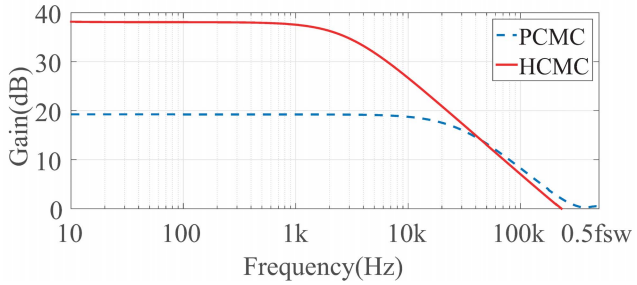

Fig. 4. Loop gain comparison of PCMC and HCMC.

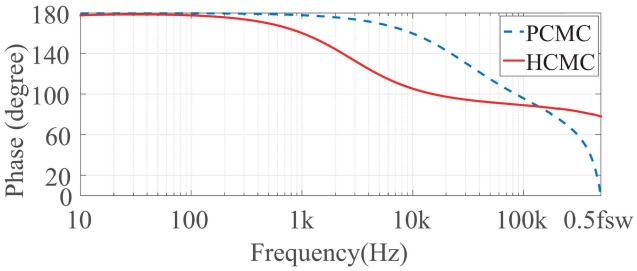

Fig. 5. Phase comparison of PCMC and HCMC.

The variable switching frequency is a drawback of HCMC as it depends on several factors including input voltage, output voltage, and hysteretic window. This creates some uncertainty with respect to electromagnetic interference (EMI), though the frequency band can roughly be controlled.

To determine the loop stability, the PCMC circuit in Fig. 2 and the HCMC circuit in Fig. 3 are modelled in SIMPLIS. In this way, the inherent loop gain of both control schemes can be compared and validated. The circuit parameters are summarized in Table I. The values are chosen such that the systems display identical loop gain at higher frequencies.

The voltage loop gain and phase of both PCMC and HCMC are compared in Figs. 4 and 5, respectively. HCMC provides more loop gain, even having a compensator gain of one. In PCMC, the dc gain is reduced by the amount of slope compensation, while HCMC has no slope compensation. The advantage can be seen at the higher frequencies because the

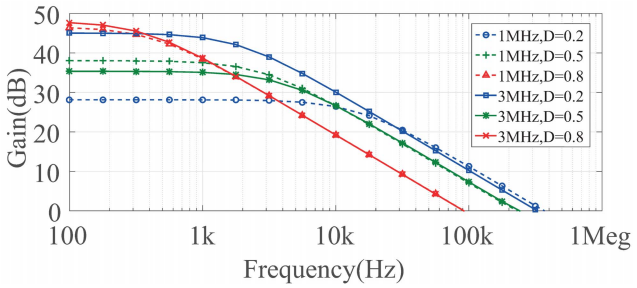

Fig. 6. Loop gain of HCMC for different duty ratios and switching frequencies.

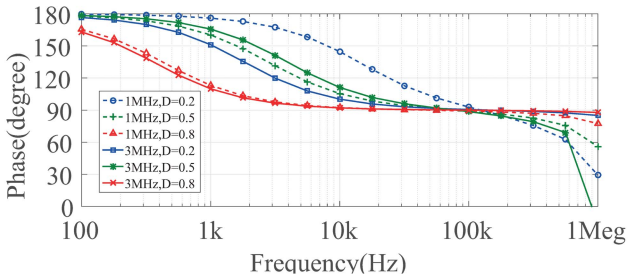

Fig. 7. Phase of HCMC for different duty ratios and switching frequencies.

phase shift is much lower for HCMC. It can also be seen that the PCMC operates at the edge of instability (to achieve the same unity gain frequency); any more loop gain in the compensator makes the system oscillate. Therefore, in order to make the system sufficiently stable and increase the loop gain, a relatively complex compensation network and dynamic slope compensation are required.

To test HCMC for varying operating conditions, the topology in Fig. 3 with the circuit parameters in Table I is simulated in SIMPLIS for a range of duty ratios and switching frequencies. The results of loop gain and phase are shown in Figs. 6 and 7, respectively. It can be seen that the phase margin stays sufficient for a wide range of operating conditions.

Apart from the inherent stability and higher bandwidth, ripple HCMC provides an extra degree of freedom: changing the current ripple. This property is exploited here by adaptively adjusting the ripple to keep the converter in soft switching and thus increase efficiency.

B. Minimum Dissipation

In an application involving battery-powered USN nodes, the requirement of output power can change drastically from low to high power levels and vice versa. Therefore, in order to improve battery life, the boost converter must be power efficient over a wide range of output power levels. A complete characterization of different power dissipation mechanisms in a class-D amplifier is given in [23]. The results show that for a high-voltage class-D amplifier, minimum dissipation can be achieved by keeping the amplifier running near the soft switching boundary, where the inductor current is just enough to charge and discharge the output switching node. Therefore in order to verify the same conclusion for a boost converter, the boost converter with power stage shown in Fig. 8 is

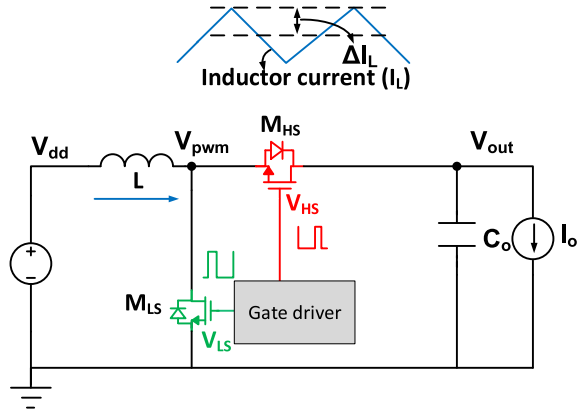

Fig. 8. Bidirectional boost converter power stage.

analyzed here. The output voltage of a boost converter can be expressed as

$$V_{\text{out}} = \frac{V_{dd}}{1-D}. \tag{2}$$

The root-mean-squared inductor current $I_{L,\text{RMS}}$ is composed of a dc component I_L and a triangle ripple component ΔI_L. This can be expressed as [23]

$$I_{L,\text{RMS}} = \sqrt{{I_L}^2 + \frac{\Delta {I_L}^2}{12}}. \tag{3}$$

The dc component of the inductor current I_L depends on the output current I_o and duty ratio (D)

$$I_L = \frac{I_o}{1-D} \tag{4}$$

the ripple of the inductor current ΔI_L, is given by

$$\Delta I_L = \frac{V_{dd} * D}{2 * L * f_{\text{sw}}}. \tag{5}$$

The total dissipation (P_d) in a boost converter can be categorized into three major loss mechanisms: conduction loss (P_{cond}) due to the inductor current ($I_{L,\text{RMS}}$), gate-driver loss (P_g) caused by charging and discharging the gate capacitance of the power transistors and switching loss (P_{sw}) associated with charging and discharging of the output parasitic capacitances of the power transistors at the PWM node. For high-voltage applications, the dominant losses are the switching losses. As shown in Fig. 9, the switching loss (P_{sw}) based on falling switching transition (also valid for rising transitions) can be categorized into one of the following categories.

1) *Hard Switching Loss:* The inductor current cannot discharge the PWM node, as shown in Fig. 9(a).
2) *Partial Soft Switching:* The inductor current is not large enough to completely discharge the PWM node during dead time, as shown in Fig. 9(b).
3) *Complete Soft Switching:* The inductor current is enough to completely discharge the PWM node, as shown in Fig. 9(c).

In order to verify, if the minimum dissipation can be achieved at the soft switching boundary, a comparison of the transistor-level power dissipation simulation with the

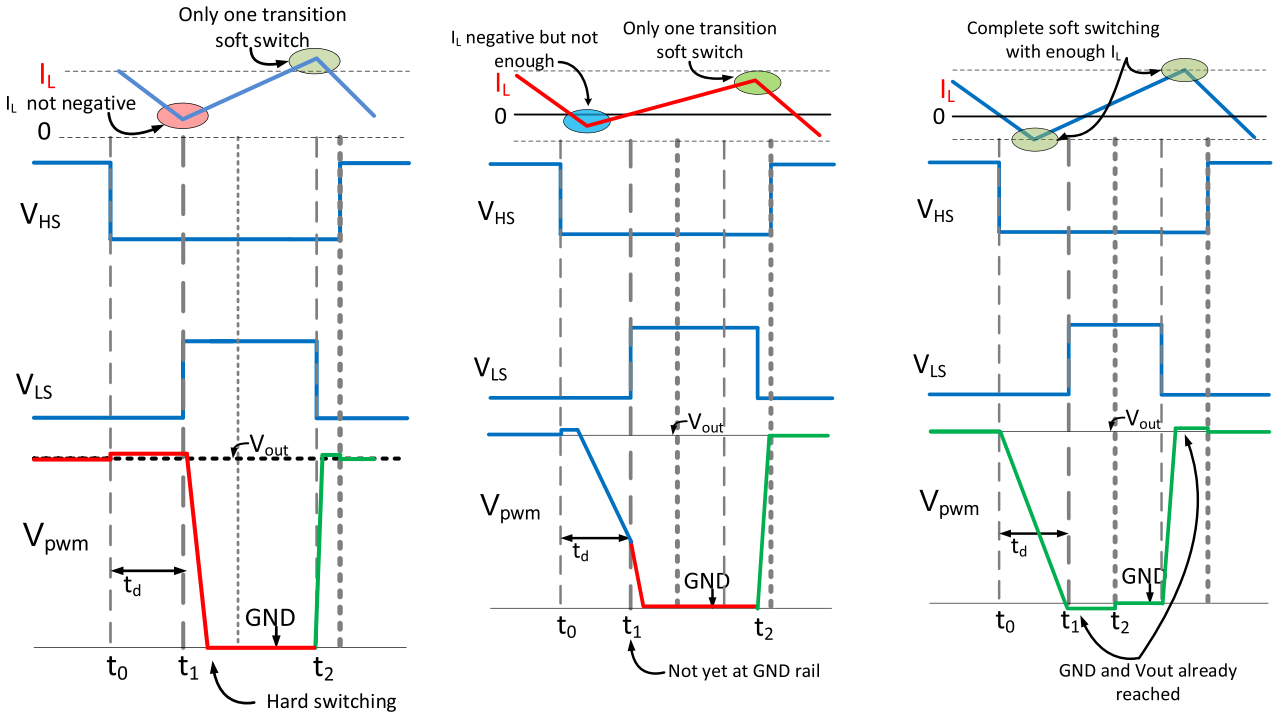

Fig. 9. Illustration of different switching conditions from hard switching to complete soft switching. (a) One hard-switching transition. (b) Partial soft switching transition. (c) Complete soft switching transition.

TABLE II
CIRCUIT PARAMETERS FOR DISSIPATION ANALYSIS

Parameters	Values
Power mosfet model	IRFL014
Gate driver model	LTC4446
Diode model (D)	1N5819
Boot strap capacitance (C_{boot})	0.1 µF
Duty ratio (D)	0.5
Inductor (L)	2 µH
Supply voltage (V_{dd})	9 V
Driver voltage (V_{cc})	9 V
On resistance(r_{on})	250 mΩ
Gate charge (Q_{iss})	8nC
Output charge (Q_{oss})	6nC
Output capacitance (Co)	10 µF
Dead time (t_d)	80nsec
Load current(I_{o1})	50mA
Load current(I_{o2})	400mA

analytical model presented in [23] can be made. Therefore, the output power stage shown in Fig. 8 with circuit parameters in Table II is simulated with two different output power conditions for a range of switching frequencies (to vary the inductor current ripple).

The comparison of the analytical model and circuit simulation is shown in Figs. 10 and 11 for an output current (I_{out}) of 50 and 400 mA, respectively.

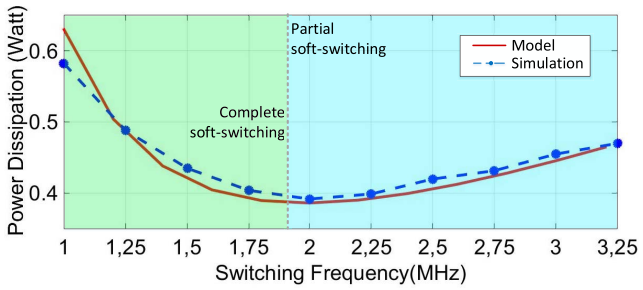

Fig. 10. Minimum power loss versus switching frequency for fixed $V_o = 24$ V and $I_o = 50$ mA.

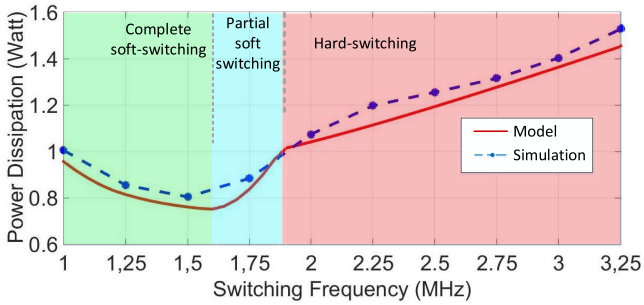

Fig. 11. Minimum power loss versus switching frequency for fixed $V_o = 24$ V and $I_o = 400$ mA.

For low output power as shown in Fig. 10, the dissipation is mainly due to conduction losses at low switching frequency, due to the large current ripple. As the switching frequency

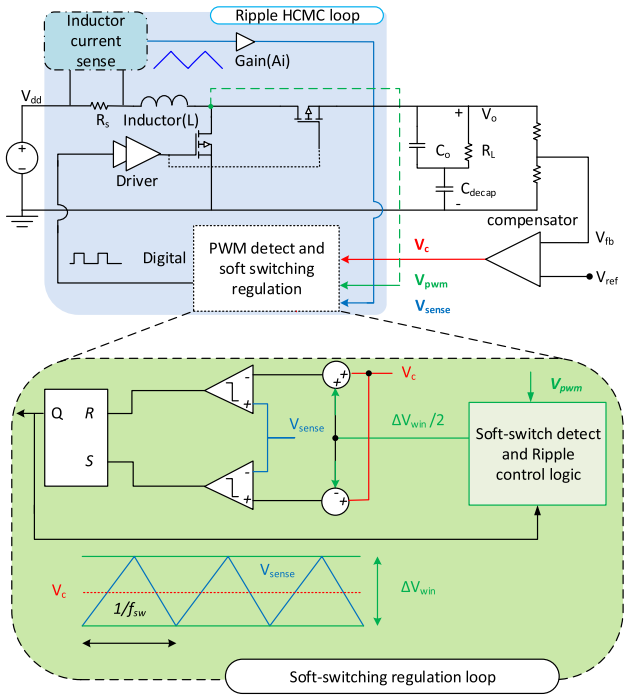

Fig. 12. HCMC-based boost converter with soft switch regulation loop.

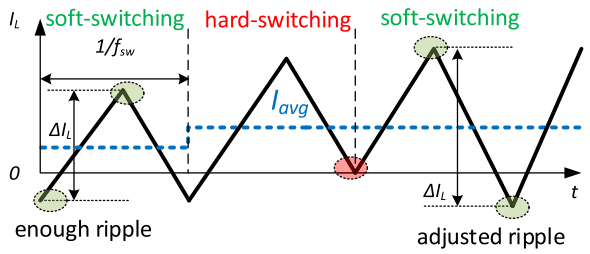

Fig. 13. Regulation of soft switching transitions.

is increased, the conduction losses reduce, the converter stays fully soft switching and a minimum dissipation point is achieved. Further increasing the switching frequency results in partial soft switching transitions making switching loss starts to increase. For high output power as in Fig. 11, the trend is similar. The minimum dissipation point is achieved at a lower switching frequency because a larger inductor current ripple is necessary to keep I_L bidirectional at the switching instants.

Compared to hard switching, complete soft switching requires a reverse inductor current that can be considered an extra loss. However, in high-voltage applications, the CV^2 losses of charging parasitic capacitances are higher than the extra loss as a result of the reverse inductor current, as can be seen in Fig. 11.

These results show that also for a high-voltage boost converter power stage, the minimum dissipation occurs at the boundary of soft switching and partial soft switching. For the case of simplicity the inductor core loss is ignored in the comparison above. Inductor core loss increases the total dissipation; however, as shown in [23], the minimum dissipation still occurs very close to the soft switching boundary. Therefore, by changing the hysteretic window in HCMC as function of I_o, the current ripple can directly be controlled and the switching frequency can be brought to this point of minimum dissipation.

C. Soft Switching Regulation Loop

Based on the results in Section II-B, our proposed scheme uses a soft switching regulation loop as shown in Fig. 12 to reduce power dissipation, by adaptively changing the magnitude of the current ripple. This results in optimum power efficiency over wide range of output power levels for the HCMC-based boost converter.

In order to make the converter run in soft switching, detection of the switching transitions is a first step. Depending on the magnitude and direction of the inductor current at the switching instant, switching of the V_{pwm} node can be made lossless. As shown in Fig. 9(c), complete soft switching can occur when the inductor current is bi-directional and can charge/discharge the parasitics at V_{pwm} to V_{out} and GND respectively, making both the rising and falling transitions soft switching. By observing the V_{pwm} node during t_d it can be detected if a transition is soft switching: if the PWM node reaches the opposite supply rail within the dead time, the transition is lossless.

The soft switching regulation loop that we use can be best understood with the help of Fig. 13 which shows a step increase of the average inductor current. The moment the average inductor current is increased, one of the transitions becomes hard switching; this triggers the soft switching regulation loop to increase the hysteretic window, causing the inductor current ripple (ΔI_L) to increase and move the converter back to soft switching transitions. This way it can track the highest efficiency over a wide range of output power levels.

Although the HCMC loop and the soft switching loop together determine the PWM signal, the loops are basically independent. Fig. 12 shows that the hysteretic window is determined by adding and subtracting $1/2\Delta V_{\text{win}}$ from the error voltage V_c, generating the inductor current switching points V_{peak} and V_{valley}. Therefore, these are symmetric around the error voltage V_c. So when the ripple (represented by ΔV_{win}) changes, V_{peak} and V_{valley} change, but the average stays the same. Although the gain and phase of the HCMC loop change somewhat due to the changing switching frequency (as illustrated in Figs. 6 and 7), the duty cycle and the average inductor current stay the same and the output voltage regulation is (in first order) not disturbed. Hence the HCMC loop and f_{sw} regulation loop are largely independent, preventing instability [27].

III. System and Circuit Implementation

The proposed implementation of the topology is shown in Fig. 14. The system is realized on a printed circuit board (PCB) using an external power stage and the control is realized on chip. The non-overlapping gate driver signals are generated internally for the external gate driver IC. The chip circuitry is mainly divided into the ripple HCMC loop and the soft switching regulation loop. Due to the ease of adding and subtracting currents, the HCMC loop implementation is realized in the current domain.

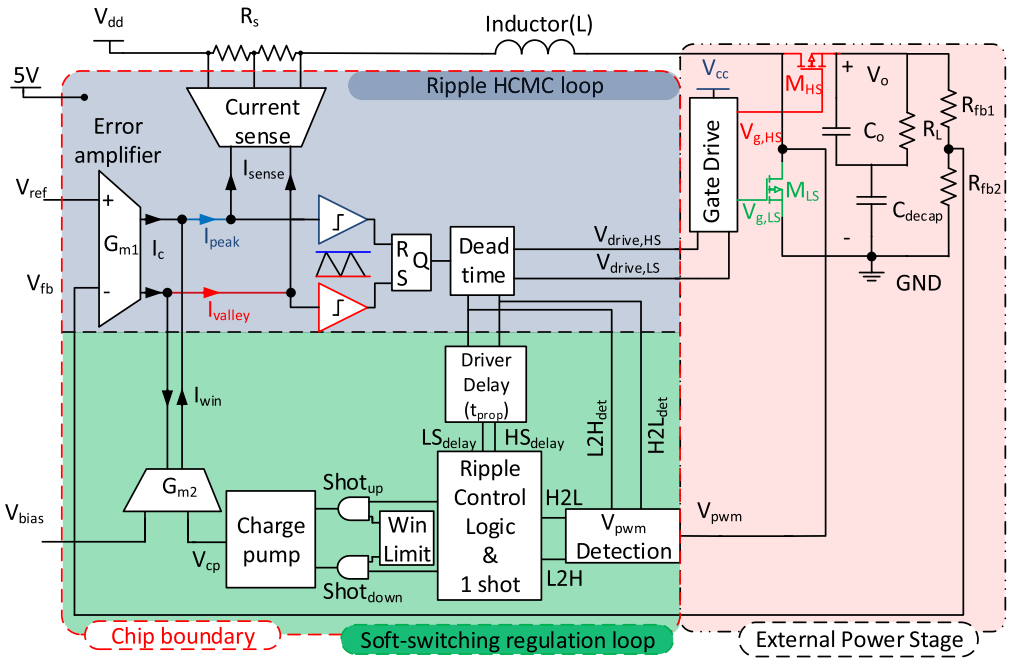

Fig. 14. System overview of HCMC-based boost converter with soft switching regulation.

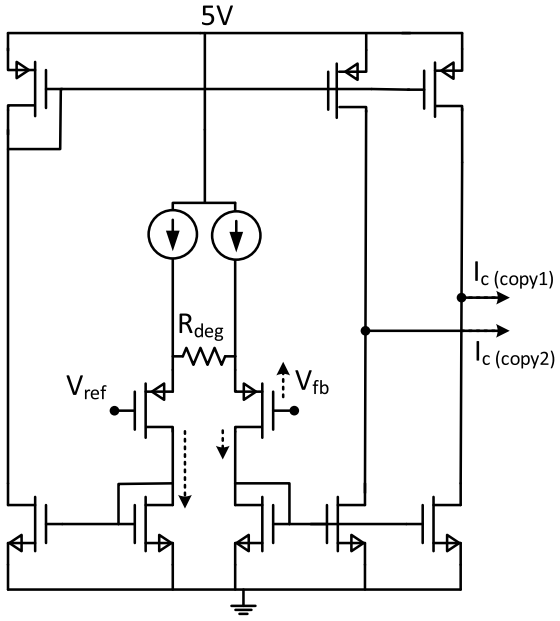

Fig. 15. Implementation of transconductor G_{m1}.

A. HCMC Regulation

The HCMC loop is responsible for making sure the output voltage V_o signal tracks the external reference signal V_{ref} using a negative feedback loop. The actual implementation of the transconductor is shown in Fig. 15. The on-chip current-sense (CS) transconductor produces two copies of I_{sense}, a scaled version of I_L, by translating the voltage across the sensing resistor R_s.

The transconductor G_{m1} generates two copies of the desired control current I_c (current representation of V_c in Fig. 12), whereas the transconductor G_{m2} produces the relevant window current I_{win} (current representation of V_{win} in Fig. 12) to set the desired f_{sw}. The implementation of both transconductors is identical using source degeneration for better linearity, only the degeneration resistors are different and one of the output currents of G_{m2} is reversed because it must be subtracted from I_c. To avoid a negative window the charge pump voltage V_{cp} is always greater than V_{bias}. The peak and valley current comparators are implemented as inverters.

B. Current Sensing

In all current mode control based topologies, current sensing is a fundamental step. Several techniques have been reported in the literature to implement on-chip current sensors [28]–[31]. For HCMC, the complete inductor current needs to be sensed, therefore for maintaining simplicity and accuracy, the choice of an off-chip sense resistor R_s is made. The value of R_s is chosen to be four times smaller than R_{on} of the external power transistor to keep conduction losses low.

To reduce distortion in V_o, a linear current sensing scheme is proposed in Fig. 16. The circuit is designed to handle common-mode voltages near V_{dd} and is implemented differentially. The gate voltage of the input transistors M_{1-4} is set by bias transistor M_b. The cascode transistor M_{cascode} helps to improve current matching. The $M_{\text{HVprotect}}$ transistors clamp the LVNMOS gate voltage during an over-current situation.

During an increase in I_L as shown in Fig. 16, the gate–source voltage of both M_1 and M_2 increase, while the gate–source voltage of M_3 and M_4 decreases. Hence, the current I_1 increases and I_3 decreases. The difference current I_{sense} is thus equal to the inductor current I_L scaled by R_s and the transconductance (gm) of M_1 and M_3. The advantage comes from the fact that while gm is non-linear, the difference of currents cancels the (dominant) second-order

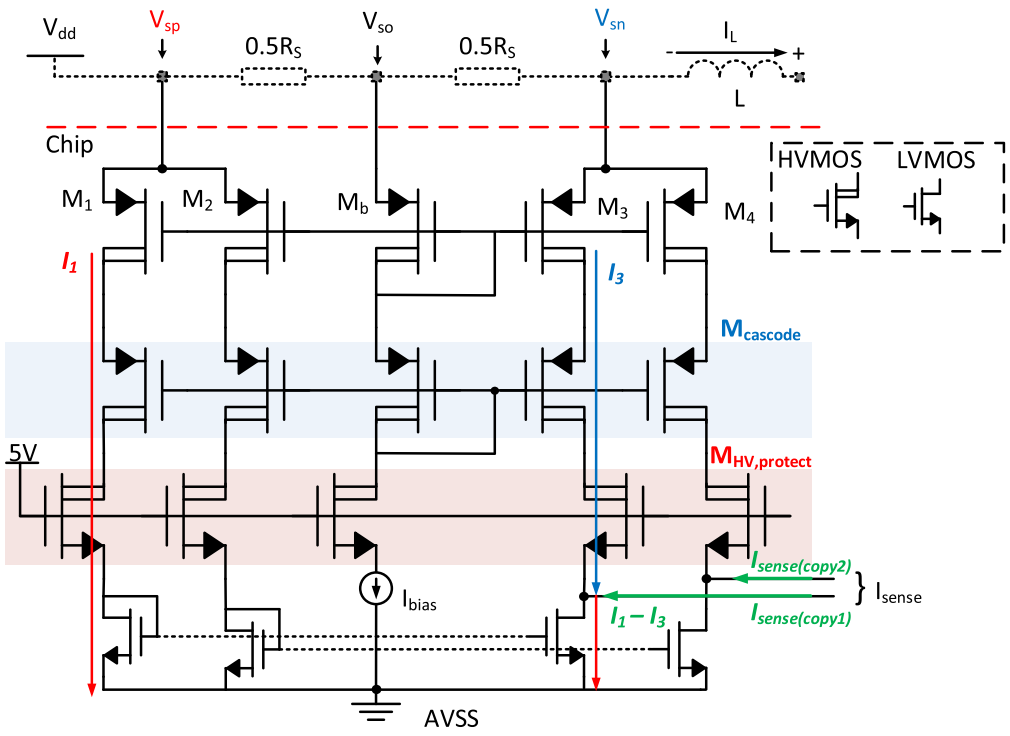

Fig. 16. High side current sense circuit.

non-linearity of gm. Therefore, linearity is better compared to a differential pair, where the sum I_1 and I_3 would be constant. The maximum non-linearity of the simulated current sense is 2.6% of full scale. Small deviations in the sensed inductor current are no problem because the external loop tracks the average current and adjusts it until the average current is correct. In total two replica currents are generated for peak and valley level detection as explained in Fig. 15 earlier.

C. Soft Switching Regulation

The soft switching regulation loop shown in Fig. 14 works by observing V_{pwm} at the end of the dead time t_d. This information is passed to the ripple control logic to determine if the ripple needs to be increased or decreased in order to keep the converter running in soft switching. Based on this decision, the ripple control logic drives the charge pump/loop filter with an up/down single shot pulse. If the ripple needs to be increased, the charge pump increase V_{cp} with a step ΔV_{cp} and vice versa.

Due to the fact that we use an external power stage, the signals $V_{g,\text{HS}}$ and $V_{g,\text{LS}}$ generated by the chip suffer from propagation delay introduced by the external driver IC. Hence to satisfy the timing requirements for internal logic, a replica delay t_{prop} is added to the internal signals in the ripple control logic block and must be set to match the external driver delay.

Depending on the output power level, the regulation loop adjusts f_{sw} in order to maintain soft switching. The minimum f_{sw} is chosen to be 1 MHz dictated by inductor size, distortion, and point of hard switching. Similarly the maximum f_{sw} must be limited to approximately 3.2 MHz due to the external power stage propagation delay, distortion caused by dead time, and gate driver dissipation. The f_{sw} limits are externally set by specifying the window limits; the window limit block monitors I_{win} and disables the ripple control logic if needed.

In normal operation during steady state, the regulation loop oscillates around soft and partial soft switching transitions every alternate switching cycle. The main time constant in the loop, however, is set by the loop filter, ensuring a dominant first order behaviour of the loop gain. Therefore, in response to sudden increase/decrease in output power, the regulation loop does not abruptly change the ripple.

The step size ΔV_{cp} of the charge pump is set to 20 mV, equivalent to a 110 mA change in inductor current, which is based on the required tracking speed of the loop. In the proposed design, the tuning window of the charge pump voltage is 350 mV, meaning the loop can adapt from minimum to maximum inductor current in 18 switching periods. With an average switching frequency of 2 MHz, this results in a 30 kHz full-power bandwidth.

D. V_{pwm} Detect and Ripple Control

The V_{pwm} detection circuit is shown in Fig. 17. When $H2L_{\text{det}}$ or $L2H_{\text{det}}$ is high, it detects if V_{pwm} has reached the corresponding supply rail within the dead time t_d. Since the $V_{g,HS}$ driver signal is level shifted by the driver IC for proper operation, $L2H_{\text{det}}$ must also be level shifted to turn on $M_{\text{shield}}HS$ transistor, as shown in Fig. 17. The H2L detection is communicated via a current mirror near V_{dd} to isolate the severe ground bounce on the power ground. The detection information is passed to the ripple control logic shown in Fig. 18. The ripple control logic checks if both rising and falling transitions of the V_{pwm} node are

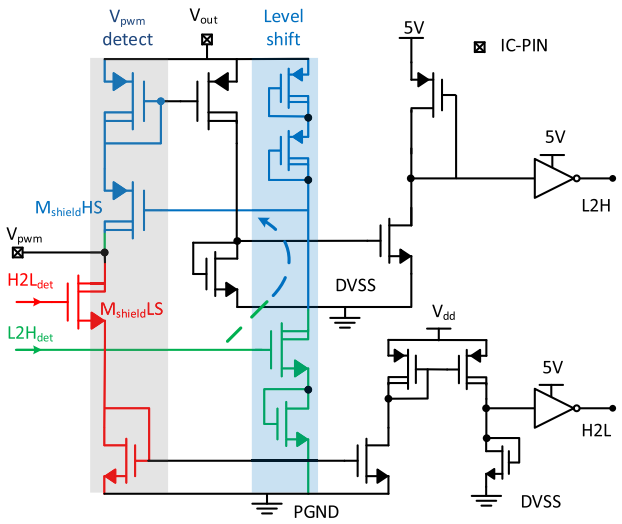

Fig. 17. Soft switching detection circuit.

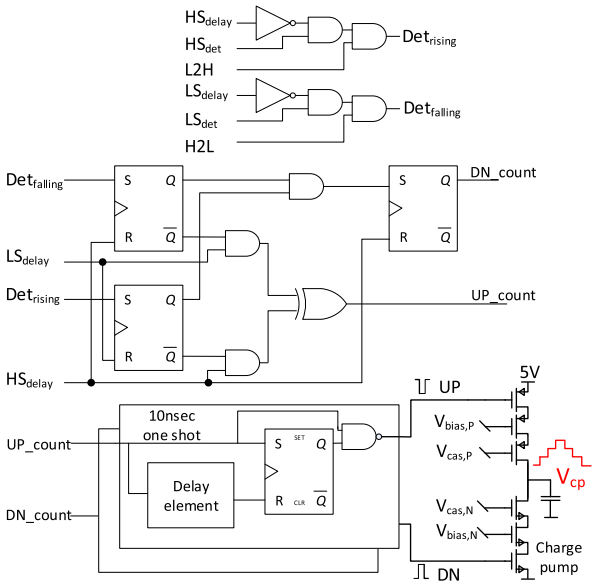

Fig. 18. Ripple control logic.

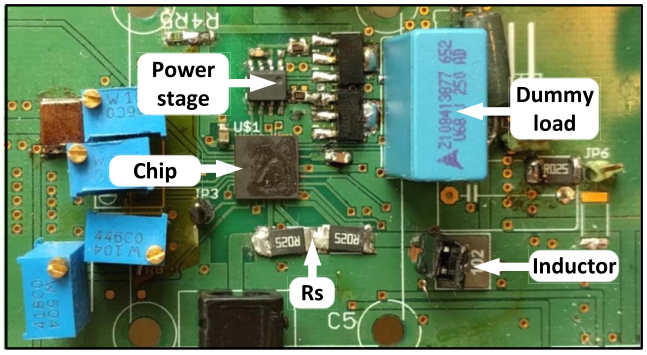

Fig. 19. Implemented PCB for the amplifier.

TABLE III
PERFORMANCE AND COMPONENTS SUMMARY

Parameters	Values
Technology	0.25 µm HVCMOS
Driver IC	LM5101C
Power transistors	NDT3055
C_{boot}	0.1 µF
Inductor (L)	2 µH
Supply voltage (V_{dd})	9V
Driver voltage (V_{cc})	9V
IC voltage	5V
On resistance(r_{on})	100 mΩ
Output capacitance (Co)	0.47 µF
Decoupling capacitor (C_{decap})	50 µF
Switching Freq (f_{sw})	1MHz-3.2MHz
Signal Freq (f_{sig})	30 kHz
*R_L	1kΩ
Dead time (t_d)	80nsec
Maximum Power Efficiency(η)	85% @ 20VA
Die Size	3 mm × 3 mm
*R_L models the water coupling	

soft switching, triggering the corresponding DN pulse. If any one of the V_{pwm} transitions is not finished within t_d, the UP pulse is triggered. These UP/DN pulses are passed on to the charge pump at the end of each switching cycle resulting in increase/decrease in the current ripple. The charge pump is timed by a one shot circuit to increase and decrease the voltage in steps at the input of the transconductor.

IV. MEASUREMENTS

The proposed HCMC-based boosting amplifier with soft switching regulation is implemented on a PCB as shown in Fig. 19, combining an external power stage and the proposed chip. The chip is implemented in a 60 V 0.25 μm high-voltage CMOS process with a size of 3 mm × 3 mm and is shown in Fig. 20. The performance and component parameters are summarized in Table III. For the chip implementation, the analog and digital sections are separated in the layout to avoid switching noise. Similarly, the external power stage switching current loop is separated from the analog signal path, to reduce the effect of ground bounce. For start-up operation, the soft switching loop is initially disabled by an enable/disable pin and an initial charge pump voltage of $V_{\text{cp}} = 1.55$ V is applied externally. After the amplifier reaches steady-state operation, the soft switching loop is enabled.

Fig. 21 shows the boosted output voltage, measured across the load for a 30-kHz sine wave. The output shows a 38 Vpp signal with a supply voltage of 9 V. Although the technology supports 60 V, the maximum output voltage is limited to 50 V because at high switching frequencies the dead time limits the maximum boosting ratio. Also, some of this headroom is used for r_{on} losses.

Figs. 22 and 23 present a comparison between the operation of the amplifier at two output powers. For the first case, where the amplifier is driven by a high swing input signal, the inductor current ripple is increased to make the converter run near the soft switching boundary. When the input voltage

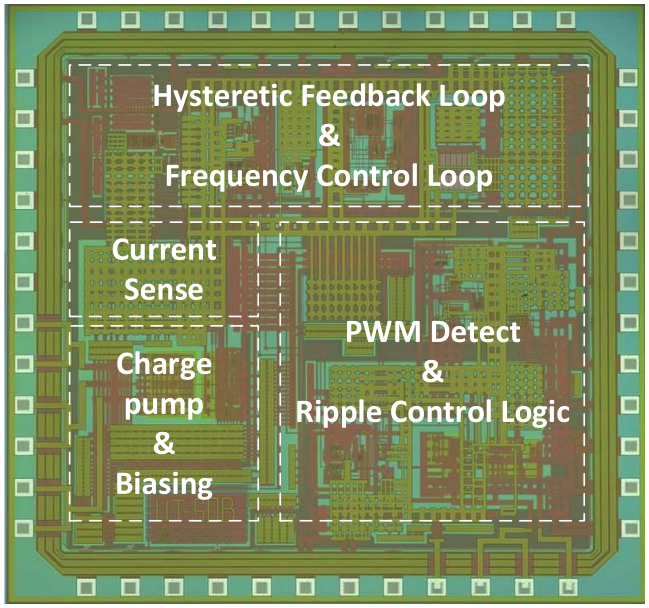

Fig. 20. Chip micrograph.

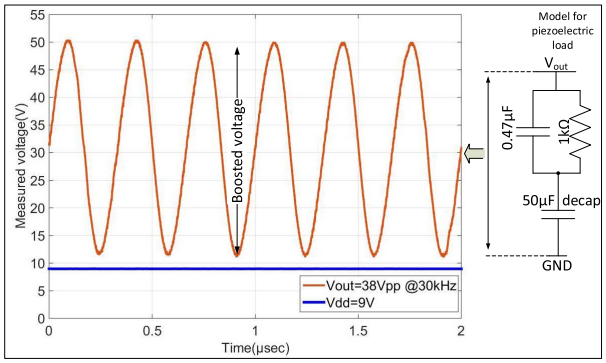

Fig. 21. Time-domain waveform of boosted output signal (red) generated at 30 kHz across V_{out} and GND with an input supply of 9 V.

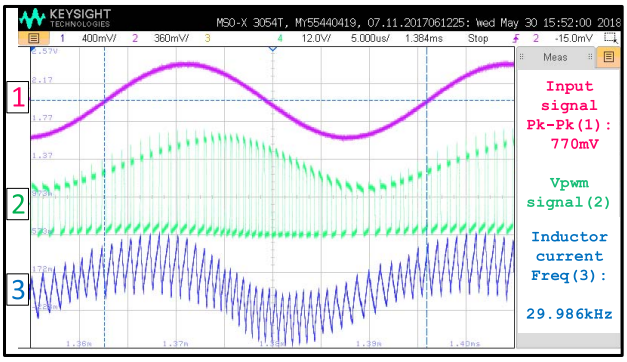

Fig. 22. Time-domain waveform of PWM (green) signal generated at 30 kHz across V_{pwm} and GND with inductor current I_L (blue).

signal decreases, the inductor current ripple decreases resulting in optimum operation.

As the load is dominantly capacitive at the desired signal frequency of 30 kHz, the processed output power (P_{out}) is

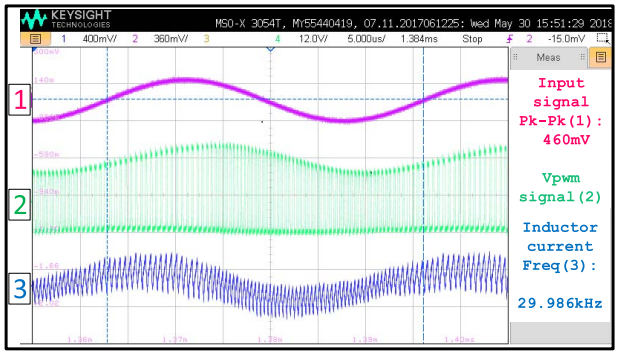

Fig. 23. Time-domain waveform of PWM (green) signal generated at 30 kHz across V_{pwm} and GND with inductor current I_L (blue).

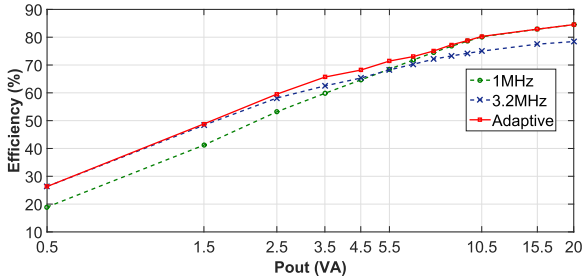

Fig. 24. Efficiency measurements for adaptive and fixed f_{sw} as a function of output power at 30-kHz input signal.

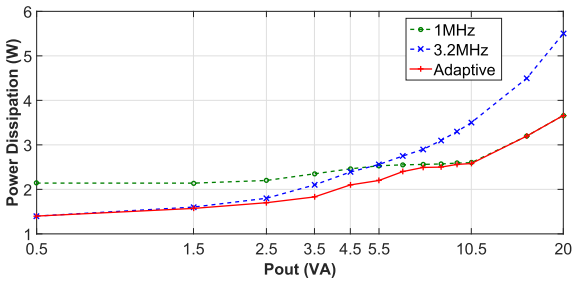

Fig. 25. Power dissipation measurements for adaptive and fixed f_{sw} as a function of output power at 30-kHz input signal.

apparent power. Hence the measured efficiency is calculated as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_d} \tag{6}$$

where P_{out} is measured as $V_{\text{out,rms}} * I_{\text{out,rms}}$ (VA) and P_d is the total amplifier power dissipation, including external power stage and control circuits. The measured efficiency of the boosting amplifier for a 30-kHz sine wave as a function of P_{out} is shown in Fig. 24 for both fixed and adaptive f_{sw}. P_{out} is varied by changing the amplitude of the output signal. Since the proposed scheme tunes itself to achieve minimum power loss, the effectiveness of the scheme is compared to two fixed 1 MHz and 3.2 MHz f_{sw} modes. Fig. 24 clearly shows that the scheme tracks the best efficiency across the whole output power range as compared to the low and high switching modes.

Fig. 25 shows a comparison of the power dissipation P_d of the adaptive f_{sw} regulation with fixed f_{sw} conditions. At low

TABLE IV
COMPARISON WITH OTHER HIGH-VOLTAGE PIEZO-DRIVER TOPOLOGIES

Parameters	This work	[16]	[32]	[23]	[33]
Technology	0.25 µm	0.18 µm	-	0.14 µm	-
Topology	boosted	boosted	boosted	class-D	linear
Load	470 nF	330 nF	330 nF	23 µF	10 µF
Bandwidth (BW)	30kHz	150Hz	150Hz	300Hz	200Hz
Inductor (L)	2 µH	100 µH	4.7 µH	100 µH	N/A
$V_o$pp	40V	100V	100V	80V	220V
Supply(V_{dd})	9V	3.6V	3.6V	80V	220V
f_{sw}	1-3.2MHz	kHz range	-	230-530kHz	N/A
Efficiency	85%	*82%	*32%	**83%	-
($P_{out,max}$)	20VA	0.39VA	0.39VA	45VA	1VA
THD+N	0.6%-5%	0.56%	1.2%	0.94%	0.62%
	1kHz-30kHz	150Hz	150Hz	500Hz	200Hz

'-'=not available, N/A=not applicable
(*) Derived efficiency based on given load and dissipation conditions
(**) Derived efficiency based on class-D+boost($\eta = 90\%$)with same boosting ratio

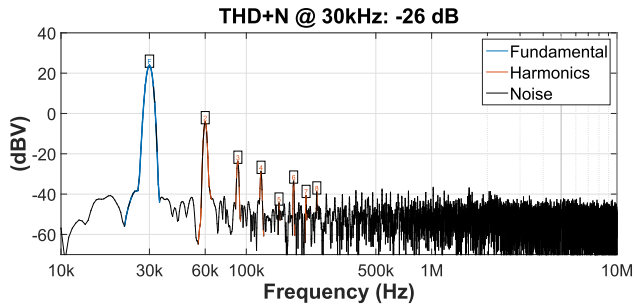

Fig. 26. Spectrum plot of 30 kHz 40 V_{pp} sine generated across the load with 9-V input voltage.

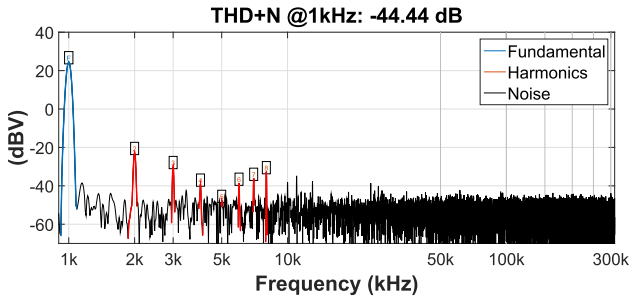

Fig. 27. Spectrum plot of 1 kHz 40 V_{pp} sine generated across the load with 9-V input voltage.

output power, the amplifier regulates itself to 3.2-MHz switching frequency and at high power it regulates itself to 1-MHz switching frequency.

For the case of minimum output power, the soft switching regulation improves the efficiency from 18.9% to 27% by dissipating 35% less power compared to switching at a fixed 1 MHz. The dissipation at low output power is mainly dominated by fixed dissipation sources independent of load current, like static currents, gate driver losses, and other capacitive losses. In case of peak output power, the efficiency is improved from 78% to 84% by dissipating 33% less power compared to switching at a fixed 3.2 MHz. This improvement is largely independent of the signal frequency as the soft switching loop is fast enough to track a 30 kHz signal, so lower frequency signals will be quasi static in comparison.

The system achieves a THD + N of 0.6% at 1 kHz and 5% at 30 kHz with a 40 V_{pp} sinusoidal output signal as shown in Figs. 26 and 27, respectively.

THD + N of the amplifier is also examined as a function of output voltage swing in Fig. 28. In addition, the amplifier's distortion is compared with adaptive and fixed f_{sw}. THD + N of a hysteretic-based boost converter depends on several factors. Apart from the inherent boost converter non-linearity, contributing effects are noise, the influence of f_{sw} on the loop

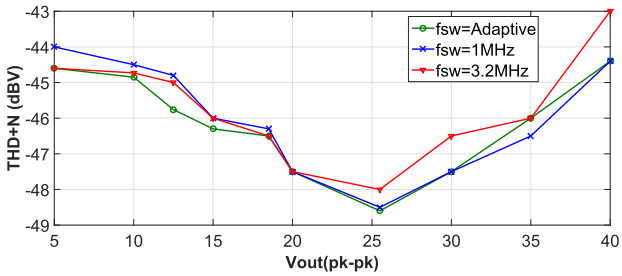

Fig. 28. THD + N measurement results comparison with $f_{sig} = 1$ kHz, $V_{dd} = 9$ V, for adaptive f_{sw} and fixed f_{sw} of 1 and 3.2 MHz.

gain [34], asymmetric rise and fall time of the V_{pwm} node [23] and the effect of fixed dead time at high f_{sw} [35]. The exact contribution of each effect to THD + N, however, is difficult to predict.

The proposed amplifier is compared in Table IV with previously reported state-of-the-art piezoelectric driver topologies. Although the topology in [16] uses a boost converter for direct signal generation, the operating bandwidth and output power are very low. The topology in [32] shows much lower efficiency with even higher distortion. The work in [23] is based on a class-D amplifier which uses a fixed supply voltage. In this case for the purpose of comparison, the real efficiency

of the system is calculated based on that class-D amplifier combined with a hypothetical dc–dc boost converter with an efficiency of 90%. In [33], a linear amplifier is proposed; the efficiency figures are not available but bandwidth is lower and distortion is higher. Overall, the proposed system shows higher efficiency and much higher bandwidth than previous works.

V. Conclusion

This paper proposes an efficient method of generating high-voltage signals for piezoelectric transducers from a single boost converter stage. By using ripple HCMC, the boost converter can achieve high bandwidth without stability problems. Furthermore, by combining the hysteretic loop with soft switching regulation, the inductor current ripple is automatically tuned to achieve soft switching regulation over a wide range of output power. The control circuits are realized on chip and measurements show that the performance improves the state of the art by featuring higher efficiency and considerably higher bandwidth.

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