High-Linearity Bottom-Plate Mixing Technique With Switch Sharing for *N*-path Filters/Mixers

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***Abstract*— A four-path filter/mixer for surface acoustic wave (SAW)-less frequency division duplex (FDD) radio receivers is proposed, targeting high linearity and compression requirements. A bottom-plate mixing technique improves linearity by reducing the gate-source voltage modulation of the MOSFET switches. Differential bottom-plate mixing allows for switch sharing which halves the effective switch resistance to reduce drain-source voltage modulation. The first four-path switch-RC filter stage with bottom-plate mixing and a shared switch renders 2nd-order voltage-domain RF-bandpass filtering around the LO frequency. Extra out-of-band rejection is implemented combined with *V–I* conversion and zero-IF frequency down-conversion in the second cross-coupled switch-RC four-path stage, which offers a low-ohmic high-linearity current path for out-of-band interferers. A prototype chip fabricated in a 28-nm CMOS technology achieves an out-of-band IIP3 of +44 dBm, IIP2 of +90 dBm and blocker 1-dB gain-compression point of +13 dBm for a blocker frequency offset of 80 MHz. At this offset frequency, the measured desensitization is only 0.6 dB for a 0-dBm blocker, and 3.5 dB for a 10-dBm blocker at 0.7-GHz LO (i.e., 6- and 9-dB blocker noise figure). The chip consumes 38–96 mW for LO-frequencies of 0.1–2 GHz and occupies an active area of 0.49 mm^2.**

***Index Terms*— Bandpass, blocker rejection, CMOS, compression point, filter, frequency division duplex (FDD), high linearity, IIP2, IIP3, interference robustness, mixer-first receiver, *N*-path filter, notch, passive mixer, surface acoustic wave (SAW) less, tunable.**

I. Introduction

LTE-ADVANCED wireless receivers require high-linearity up-front filtering to prevent corruption of the in-band signals by strong out-of-band (OOB) signals and self-interference from the transmitter in case of frequency division duplex (FDD). Surface acoustic wave (SAW)-duplexer-filters are generally used for this purpose (see Fig. 1), but supporting the plethora of existing and new bands becomes troublesome with separate filters for each band. Wideband circulators can provide about 10–15-dB isolation from TX to RX. In this paper, we explore the possibility of combining an off-chip circulator with high-linearity on-chip *N*-path filtering and mixing. As an *N*-path bandpass filter (BPF) has a programmable RF-center frequency, one circulator and a programmable chip can replace a set of SAW filters, as shown in Fig. 2. However, even with 15-dB isolation from the circulator, the on-chip filter needs to deal with up to +4 dBm TX leakage P_{TX} (see Fig. 2), with a 15-dBm OOB continuous-wave (CW) blocker P_{cw} also present. Intermodulation P_{IIM3} will in this case deteriorate the RX sensitivity. For LTE applications, the integrated thermal noise is 101 dBm for a 20-MHz channel BW. If we assume P_{IIM3} is roughly the same as 101 dBm, the resulting required IIP3 is about 45–50 dBm, which is an extremely tough requirement. Inductor-less tunable *N*-path filters [1], [2] and mixer-first receivers in [3]–[6] achieved $>$ +10 dBm compression point and an IIP3 of 20–30 dBm, i.e., about 20 dB worse than required. Moreover, improved filtering is desired.A 2nd-order BPF is obtained with a simple switch-*RC* *N*-path filter and this high-linearity passive filtering

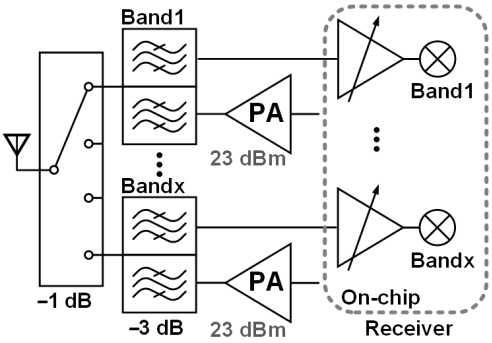

Fig. 1. Conventional LTE receiver with external SAW duplexing filters.

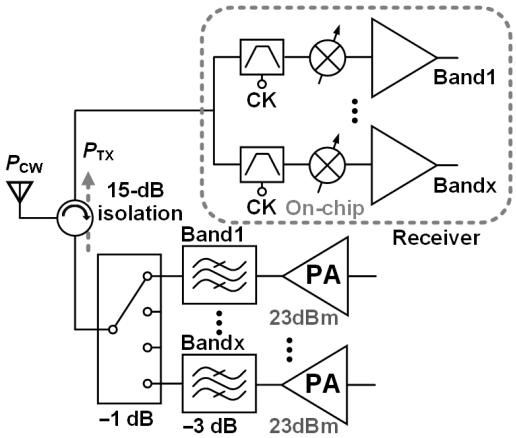

Fig. 2. Proposed LTE receiver with on-chip reconfigurable *N*-Path BPF.

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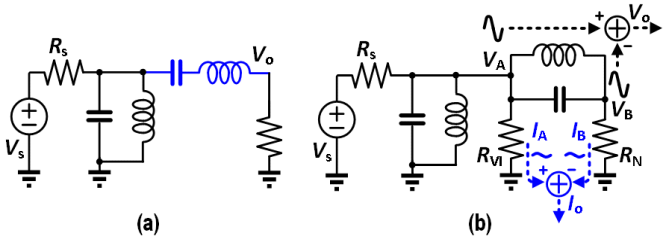


Fig. 3. (a) Conventional 4th-order BPF realization by cascading a series LC tank. (b) Proposed 4th-order BPF using V–I conversion and current subtraction.

relaxes the linearity requirement of the subsequent active amplifiers, which are much less linear. To sufficiently relax amplifier linearity, while dealing with strong blockers and TX leakage that is close to the desired RX frequency, more than 2nd-order filter roll-off may be required. Higher order N-path filtering can be realized by incorporating g_m cells [2], [7], but the active g_m circuits limit the achievable linearity. In this paper, we increase filter roll-off by cascading an N-path voltage in-voltage out (V–V) and voltage in-current out (V–I) BPF, while a bottom-plate mixing technique with switch sharing is proposed to enhance the linearity [8]. Compared to [8], this paper explains the concept in more depth, analyzes the filter transfer, noise figure and linearity, and adds simulation results and linearity benchmarks. Note that we do not target to deliver a solution ready for LTE advanced; rather, we aim for flexibility in combination with high linearity and propose a new technique that pushes flexibility and linearity. This paper is organized as follows. Section II introduces the RF BPF receiver architecture, while section III describes the receiver circuit implementation. Section IV proposes an LTI RLC model, to roughly estimate transfer function. We will propose a semi-empirical model that will be validated by measurements. Section V provides the measurement results, and the conclusion is presented in Section VI.

II. Receiver Architecture

We will now describe how we conceived the RX architecture. An N-path filter can emulate a parallel LC tank, modeled by a parallel R, L,and C [1], and perform BPF. A 4th-order BPF response could be obtained by adding a series LC tank [see Fig. 3(a) in the case of ideal LC tanks]. A series LC tank can be synthesized from a parallel LC tank via gyrator circuits [2], but these circuits limit achievable linearity. A quarter-wavelength transmission line could also be exploited [9], but this limits tuning range (0.6–0.85 GHz) while the achieved IIP3 was not sufficient (18 dBm). Fig. 3(b) shows an alternative 4th-order BPF realization by using two parallel LC tanks. As the tanks become high-ohmic in-band and low-ohmic OOB, the 1st tank attenuates OOB voltage swing bypassing OOB current, while the 2nd LC bypasses OOB current to the termination resistance R_N. If we take the output voltage across the 2nd tank, i.e., $V_o = V_A - V_B$ as in Fig. 3(b), the OOB signals become largely common mode and are attenuated. Nevertheless, a high-linearity differential amplifier that can handle large common-mode voltage swings

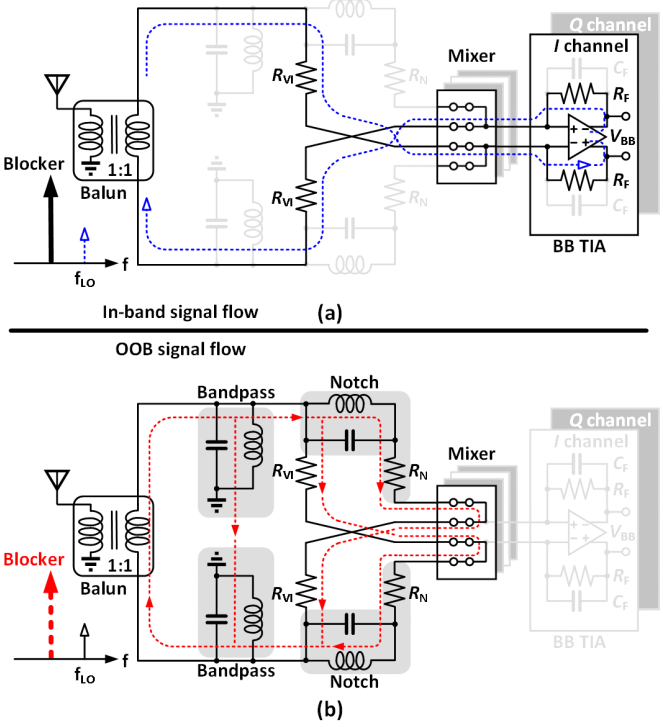


Fig. 4. (a) In-band and (b) OOB signal flow in the proposed receiver.

due to blockers is hard to implement. Instead, we propose V–I conversion by high-linearity passive resistors R_{VI} and R_N combined with current subtraction (see Fig. 3(b), output I_o). Current subtraction will be implemented by simple wire cross-coupling in the differential implementation.

Note that the BPF in Fig. 3(b) has an extra V–I conversion resistor that degrades filter-Q compared to Fig. 3(a) (i.e., Assuming $R_s = R_{VI}$ for matching, $R_s = R_{VI}$ simply halves the resistance seen by the input and hence halves Q). Although not optimal for filter selectivity, this does allow for a high-linearity implementation and this is our key target here.

Fig. 4 shows the conceptual diagram of the proposed blocker rejection receiver. The parallel LC tanks are emulated by N-path filters. The differential structure offers the possibility of high-linearity current subtraction by wire-crossing. Input voltage signals are converted to current by resistor R_{VI}, which also allows for RF-impedance matching, and this current is down-converted by the mixer switches. For in-band signals, the LC tanks are high ohmic, and the baseband (BB) current is converted to BB voltage V_{BB} by the transimpedance amplifiers (TIAs), as shown in Fig. 4(a). For OOB signals, the LC tanks become low ohmic and bypass the current as shown in Fig. 4(b). OOB signals are first attenuated by a voltage BPF and then converted to current by resistors R_{VI}. The 2nd tank acts now as notch filter, blocking in-band signals [Fig. 4(a)], but passing OOB blockers [Fig. 4(b)] which are converted to current by R_N. Due to the differential symmetry and low switch resistance, OOB blocker current will mainly circulate in the RF domain [see Fig. 4(b)], ideally without entering the BB TIA. In summary, the 1st stage gives RF blocker voltage reduction and the 2nd stage V–I

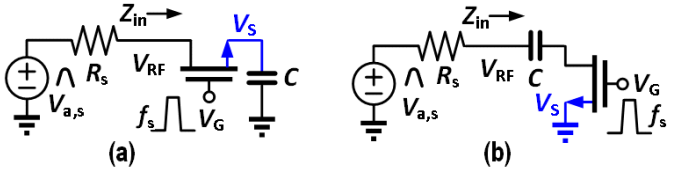


Fig. 5. Switched *RC* mixer with (a) top-plate and (b) bottom-plate mixing.

conversion with RF blocker current bypassing to improve selectivity.

III. Circuit Implementation

A. Non-Linearity Considerations

N-path filters and mixer-first receivers are switch-*RC* circuits that exploit the low-noise "mixer-region" [10], [11] or "passive mixer mode" [12], where the *RC* time constant is much larger than the on-time of the switch. In conventional (top-plate switched) mixers as shown in Fig. 5(a), the MOS switch suffers from largely varying $V_{\rm GS}$ and $V_{\rm DS}$, which modulates MOSFET channel resistance and limits linearity. To obtain some intuitive insight in the non-linearity mechanism, we will qualitatively describe the variations in channel resistance assuming the gate-voltage is switched on to a constant value (e.g., = VDD).

For simplicity, suppose the RF-voltage is a sinewave at frequency $f_{\rm RF}$ in its positive signal-half with amplitude $\hat{V}_{\rm RF}$ and average = 0 (dc value = 0), so that the RF side of the MOSFET is the drain terminal. We choose $\rho = R_{\rm sw}/R_{\rm s} \ll 1$ (e.g., $\rho = 0.1$) to achieve high OOB linearity. For in-band signals $Z_{\rm in}$ is significantly higher than source resistance R_s (e.g., $4.3R_s$ for a four-path mixer with 25% duty-cycle clocks [13]). As the switch resistance is assumed to be much smaller than R_s (e.g., $\rho = 0.1$), the BB-voltage $\hat{V}_S$ will almost reach $\hat{V}_{RF} = \hat{V}_{a,s} Z_{\rm in}/(R_s + Z_{\rm in})$ where $\hat{V}_{a,s}$ is the amplitude of the antenna signal. As a result, $V_{\rm GS}$ of the mixer switch is strongly modulated while the switch is closed, whereas the modulation of $V_{\rm DS}$ is much smaller and the non-linearity is mainly due to $V_{\rm GS}$ modulation. For OOB signals, $Z_{\rm in}$ decreases with offset frequency, reducing the $V_{\rm GS}$ modulation, while the $V_{\rm DS}$ modulation becomes slightly higher due to the increasing current. The distortion overall reduces due to the OOB filtering at V_S. When OOB signals are very far away from the LO frequency, the BB-voltage $\hat{V}_S$ becomes almost zero resulting in negligible $V_{\rm GS}$ modulation. Assuming $\hat{V}_{\rm DS} \approx \rho \hat{V}_{a,s}$, OOB IIP3 can then be estimated as [14]

$$V_{\rm IIP3} = \sqrt{\frac{4}{3} \frac{(1+\rho)^4}{\rho^3 (2g_2^2 - g_3(1+\rho))}} \tag{1}$$

where g_2 and g_3 are related to the 2nd and 3rd derivation of $I_D(V_{\rm DS})$, which can be estimated as g_2 is $(2V_{\rm OD})^{-1}$ and $g_3 = -(2V_{\rm SAT}^2)^{-1}$, where $V_{\rm OD}$ is overdrive voltage $V_{\rm GS} - V_{\rm th}$ and $V_{\rm SAT}$ is a velocity saturation parameter, respectively [14].

B. High-Linearity Bottom-Plate Mixing Technique

We will now introduce the bottom-plate mixing technique. Instead of using a switch between the RF node and the "top plate" of a grounded capacitor [Fig. 5(a)], we propose to connect the RF node to the top plate and instead switch the bottom-plate to ground as shown in Fig. 5(b). Although the name may suggest a relation with bottom-plate sampling, it is clearly different as it does not use two switches, while it also does not produce a sampled time-discrete output, but rather a continuous mixer output (for a further discussion of the difference between mixing and sampling, see also [15]). The main target for bottom-plate mixing is switch-resistance induced distortion improvement. In contrast, the deployment of bottom-plate sampling is for reducing the signal dependent charge injection and clock feedthrough.

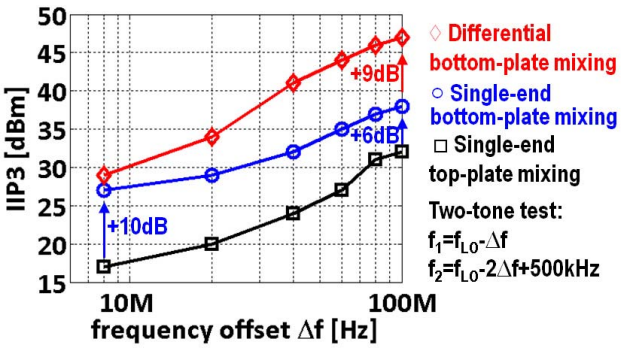


Fig. 6. Simulated IIP3 for four-path single-ended top-plate, single-ended bottom-plate, and differential bottom-plate mixing filters.

For LTE applications, the duplex frequency is <200 MHz for most of the frequency bands, while a BPF with channel BW up to 10 or 20 MHz is required. Hence not only far-OOB IIP3 matters, but also the non-linearity for OOB signals that are still rather close to the LO-frequency. To reduce the $V_{\rm GS}$ modulation and improve linearity, we proposed a bottom-plate mixing technique [8] as shown in Fig. 5(b). When the switch is turned on, the drain terminal voltage V_D of the NMOS switch will be pulled to ground, instead of being connected to a variable voltage V_S as in Fig. 5(a). Now $V_{\rm GS}$ is kept constant, i.e., the in-band $V_{\rm GS}$ modulation problem is avoided. In-band voltage signals are down-converted and mixed to capacitor C, while the signal source still sees a high impedance, i.e., very small $V_{\rm DS}$ modulation occurs. In conclusion, the bottom-plate mixing keeps $V_{\rm GS}$ constant to obtain better linearity.

Applying 1-GHz 25% duty cycle four-phase clocks with rising/falling time of 10 ps and common-mode voltage of half supply, simulations reported in Fig. 6 indeed confirm benefits. (We will discuss them in more detail below.) We tried to quantify the benefits analytically, but unfortunately accurate MOSFET models are complex. Experiments also indicate that several effects can play a role, e.g., subthreshold conduction, body effect, and charge injection. Splitting and quantifying these factors proved complicated, and hence we resort to simulations combined with qualitative reasoning and rough calculations. Bottom-plate mixing proofs to have clear linearity benefits, and reasoning supports this: apart from avoiding $V_{\rm GS}$ modulation, source-bulk voltage modulation is also avoided in Fig. 5(b), reducing threshold voltage variation due to the body effect. Moreover, as in bottom-plate mixing

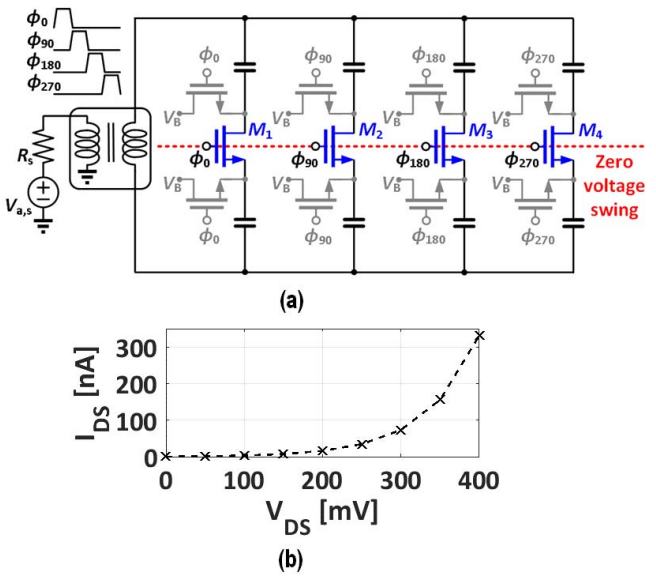


Fig. 7. (a) Circuit schematic of a four-phase differential bottom-plate mixing bandpass N-path filter. $W/L = 180$ μm/30 nm for M_1–M_4 and $W/L = 18$ μm/30 nm for other NMOS transistors, (b) simulated non-linear sub-threshold current $I_{\rm DS}$ of M_1 when it is off.

circuits, signal dependent charge injection from MOS switches is reduced as there is a low-ohmic path to ground.

Fig. 7(a) shows the circuit schematic of a four-phase differential bottom-plate mixing N-path filter. M_1–M_4 are NMOS switches with large W/L ratio for the N-path filter function, while the other NMOS switches are chosen 10× smaller to periodically reset the dc bias to the common-mode level. Larger switch size for the dc bias setting can offer faster settling (i.e., less clock cycles) to the desired common-mode level, but more LO power is required. Note that one shared NMOS switch can be used for both circuit halves, instead of two switches to ground in the conventional pseudo differential architecture of Fig. 5(b). Therefore, ρ is reduced to half of its single ended value thanks to switch sharing in the differential circuit. For $\rho \ll 1$, (1) can approximate to

$$V_{\rm IIP3} \approx \sqrt{\frac{4}{3}\frac{1}{\boldsymbol{\rho^3}(2g_2^2 - g_3)}}. \tag{2}$$

Note that (2) predicts OOB IIP3 is improved by 9 dB if ρ is halved. Fig. 6 shows the simulated IIP3 for a single-ended top-plate, single-ended bottom-plate and differential bottom-plate mixing N-path filter, driven by four-phase clocks and switch size of 180 μm/30 nm. The BPF BW $f_{-3{\rm dB,BPF}}$ is 30 MHz and $f_{\rm LO}$ is 1 GHz. TSMC 28-nm technology simulation with a PSP MOS-model was used. Comparing to the conventional topology, bottom-plate mixing improves IIP3 by 10 dB and 6 dB for in-band and OOB, respectively. As the blocker offset frequency Δf becomes very large, the $\hat{V}_S$ of single-ended top-plate mixing will almost reach zero and nearly constant $V_{\rm GS}$ is obtained. Therefore, the single-ended top-plate and bottom-plate mixing will achieve similar IIP3 (i.e., the difference of IIP3 is less than 1 dB by simulation). Note that the switch sharing in the differential bottom-plate mixing offers an additional 9-dB OOB IIP3 improvement, as predicted by (2).

An experiment was devised to find out whether weak inversion conduction in M_1–M_4 limits in-band linearity for the mixer in Fig. 7(a). Ideal switches were added in series to both sides of M_1–M_4, to block current during their off-state. This improves linearity, indicating that subthreshold current likely limits the achievable linearity. As shown in Fig. 7(a), $Z_{\rm in}$ is high ohmic for in-band signals, resulting in significant input signal swing which is ac-coupled via the N-path filter capacitors to the drain or source terminals of the transistors that are supposed to be off, but apparently modulate their current. Fig. 7(b) shows the simulated $I_{\rm DS}$ of M_1 in Fig. 7(a) as a function of $V_{\rm DS}$ (common mode of V_D and V_S is 0.2 V) when M_1 is off (gate terminal is connected to the ground). The un-constant slope indicates the sub-threshold current is non-linear.

In summary, the in-band IIP3 of conventional top-plate mixers is dominated by $V_{\rm GS}$ modulation, while far-OOB IIP3 is limited mainly by $V_{\rm DS}$ modulation. Bottom-plate mixing keeps $V_{\rm GS}$ constant to achieve high linearity for all frequencies. Moreover, OOB linearity is improved by 9 dB due to switch sharing. Subthreshold current likely limits the achievable in-band IIP3.

C. Cascading Passive RF BPF Stages

The circuit schematic of the entire proposed receiver is shown in Fig. 8(a). C_A and the corresponding switches implement the bandpass in Fig. 4(b). C_B, $R_{\rm VI}$, R_N, and the corresponding switches implement the OOB current subtraction circuit in Fig. 4(b). Because the proposed receiver is self-biased, two external RF dc blockers with low loss (<0.5 dB up to 8 GHz) are applied. A differential external clock with 4 times the LO frequency $f_{\rm LO}$ is applied to generate 4-phase 25% duty-cycle clocks via a divide-by-4 ring counter. By exploiting only one clock-edge, the pulse width of 25% duty-cycle clocks is determined by the period and not sensitive to the duty-cycle of the external clock. As a result, the timing error can be smaller than for a divide-by-2 flip-flop with extra logic circuits to realize 25% duty cycle. Note that most power is consumed in the output buffers that drive large mixer switches (not in divider itself), so that the power penalty of using a divide-by-4 compared to a divided-by-2 four-phase clock generator is not so significant. Both N-path filter stages are driven by the same clocks and hence have the same center frequency. Zero-IF frequency conversion is also implemented in the second V–I stage. The common-mode bias-voltage V_B for the mixer switches in the first V–V BPF is set to ≈0.2 V. There is a tradeoff regarding the choice of V_B. Lower V_B reduces on-resistance of switches, but increases subthreshold current when switches are off. The $W/L$of all mixer switches is 180 μm/30 nm and the differential on-resistance is as low as ≈ 2 Ω when the bulk is connected to ground. The resistance of $R_{\rm VI}$ and R_N for V–I conversion is 15 Ω, which is implemented in top metal with high-current density tolerance, low parasitic capacitance, and very high linearity. $R_{\rm VI}$ and R_N also reduce the voltage swing across mixer switches to improve the linearity. Mismatch between $R_{\rm VI}$ and R_N causes intermodulation tones at $f_{\rm LO} + f_b$ and $f_{\rm LO}$-f_b, where f_b is blocker frequency. These intermodulation tones will be down-

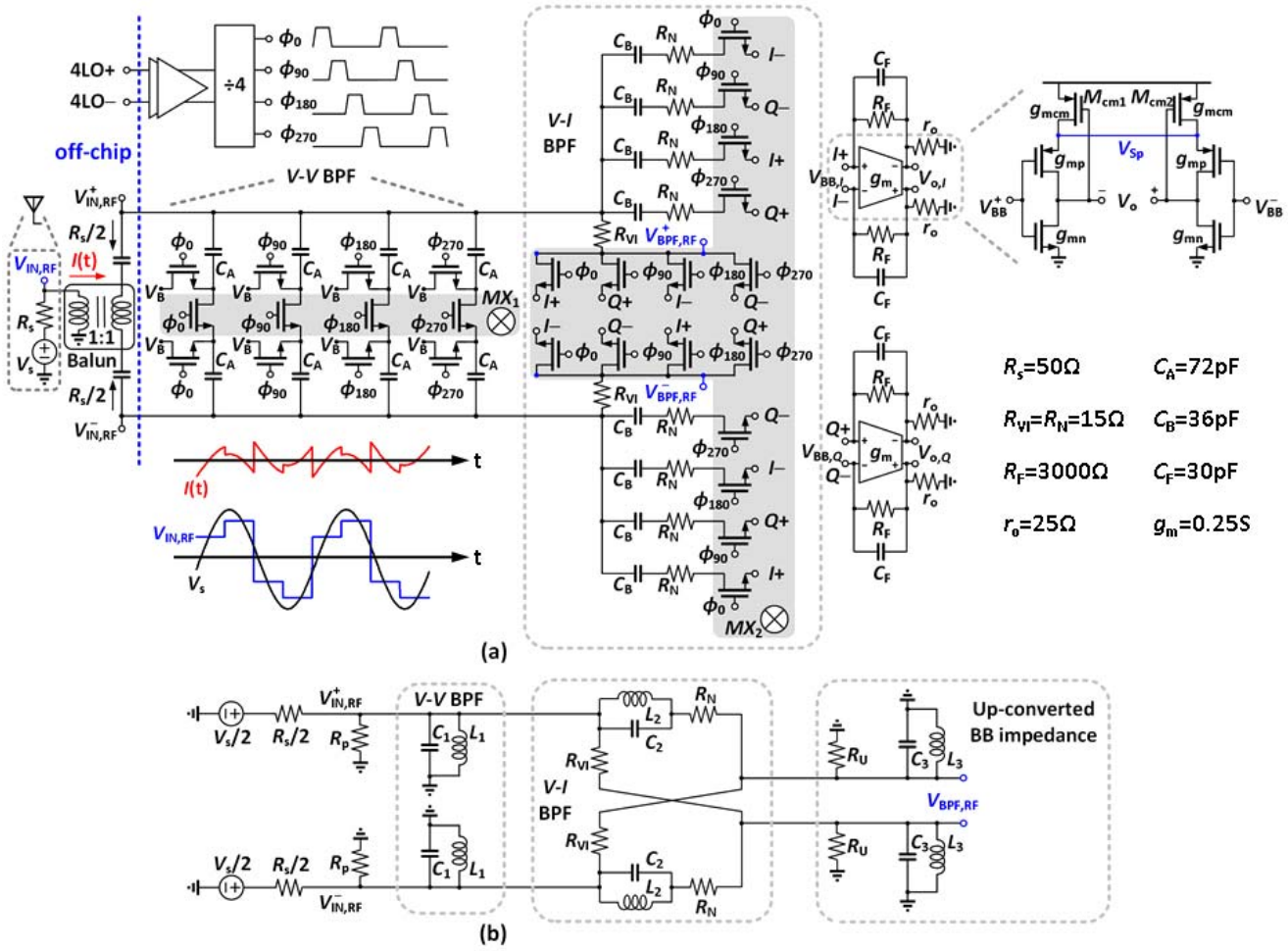


Fig. 8. (a) Circuit schematic of the proposed receiver and (b) corresponding RLC model (equivalent LTI model for the RF part)[1].

converted to a BB frequency of f_b, which is not in-band, and hence not of primary importance.

Much like the BPF, a conventional top-plate switch notch N-path filter [16] also suffers from strong V_{GS} modulation that causes non-linearity. The bottom-plate mixing technique can also be applied in the notch filter that is composed of C_B, R_N, and the corresponding mixer switches in Fig. 8(a) to gain similar benefits. The $4 \times R_N$ are used instead of one (in Fig. 4) and the switch to ground to reduce V_{GS} modulation is possible now. Also, the down-converted BB output current signals are available for OOB blocker bypassing. Switch sharing between circuit halves seems not possible.

In this receiver, the down-converted BB signal is used as output, so that the OOB rejection limitation due to switch resistance in a bandpass N-path filter [1] is avoided.

The second V–I BPF stage in Fig. 8(a), composed of R_{VI} and a notch N-path filter, enhances the selectivity, but the OOB impedance at the V–I BPF input is $(R_{VI} + R_{sw})||(R_N + R_{sw})$ while it is R_{sw} in a conventional V–V N-path filter [1]. For mixer switches in the V–I BPF that are off, still a large OOB voltage signal is directly coupled to the MOSFET-switch via capacitor C_B, again potentially resulting in non-linear subthreshold current limiting IIP3. Fortunately, the first stage V–V BPF already greatly reduces the OOB voltage signal swing, alleviating this problem.

For implementing more number of paths, a more elaborate BB I/Q re-combination circuit is required, e.g., the eight-path receiver by [13].

D. Baseband Amplifier

A CMOS inverter is one of the best transconductors in terms of dynamic range per power [17], and it can serve to make a low-noise quite-linear BB TIA. Stability concerns for closed-loop operation are avoided in a single-stage amplifier. Because it is pseudo differential, extra circuitry is needed to reduce the common mode gain, while maximizing differential mode gain, which often leads to extra power consumption and noise [18], [19]. We avoid this by implementing a low common-mode output impedance using M_{cm1} and M_{cm2} which are put above the core g_{mn} and g_{mp} devices for current re-use, as shown in the right-top corner of Fig. 8(a). Feedback resistor R_F provides self-biasing. Each BB amplifier consumes about 15 mW from a 1-V supply. The W/L values are 1700 and 1200 μm/40 nm for the PMOS and NMOS of the inverter, respectively, while $g_{mn} + g_{mp} = 250$ mS and $r_{on}||r_{op} = 25\ \Omega$. By using a higher threshold voltage

[1]One single set of mixer switches MX_2 is now implementing L_2C_2 and also L_3C_3.

for $M_{\rm cm1}$ and $M_{\rm cm2}$ and small overdrive voltage of about 60 mV for the PMOS of the inverter, all transistors can operate in saturation. $M_{\rm cm1}$ and $M_{\rm cm2}$ only generate common mode noise, which will be cancelled at the differential output. Operating $M_{\rm cm1}$ and $M_{\rm cm2}$ in saturation also provides isolation between the supply voltage and the outputs of the amplifier, which is good for supply noise rejection. For differential input signals, voltage $V_{\rm Sp}$ ideally shows very low impedance and small voltage swing due to differential symmetry and a gain of $\approx (g_{\rm mn}+g_{\rm mp})({\rm r_{on}}||{\rm r_{op}}) = 16$ dB is achieved. For a common mode input signal, $V_{\rm Sp}$ follows input signal and $g_{\rm mp}$ is degenerated. The BB amplifier output is diode-connected with output impedance of $1/g_{\rm mcm}$ giving a low common-mode gain of $g_{\rm mp}/g_{\rm mcm} \approx 3$ dB. Note that a traditional CM-feedback circuit with triode devices would lead to much smaller $g_{\rm mcm}$, i.e., more common-mode gain.

IV. Circuit Analysis

In this section, we will analyze different properties of the mixer-first receiver, like transfer function, noise and input impedance.

The equivalent RLC circuit in Fig. 8(b) models the frequency response of the multiple-stage N-path filter in magnitude. The intuition behind this semi-empirical model comes from the observation that the capacitors C_A in the first capacitor bank are not directly in parallel to the capacitors C_B in the second bank, but are coupled via resistor R_N, introducing an extra filter order.

A. RLC BPF Model

The filter shape of an N-path filter around its LO-frequency can be modeled by a parallel RLC circuit [1], [16]. The corresponding model parameter can be found as [16]

$$R_{\rm p} = \frac{N^2\sin^2(\frac{\pi}{N})}{\pi^2 - N^2\sin^2(\frac{\pi}{N})}(R_{\rm s}+R_{\rm L}) \tag{3}$$

$$C_p = \frac{\pi^2}{mN\sin^2(\pi/N)}C \tag{4}$$

$$L_p = \frac{1}{(2\pi f_{\rm LO})^2 C_p} \tag{5}$$

where $m = 2$ for single-ended circuit and $m = 8$ for differential case. N is the number of clock-phases. Note that the LC tank modeled the N-path filter only in its magnitude but not in its phase as noted in [12, eq. (43)].

Assume that mixer switches in Fig. 8(a) are ideal. The RLC equivalent circuit for the RF part of the proposed receiver is shown in Fig. 8(b). The V–V BPF is modeled by the L_1C_1 tank while the V–I BPF is modeled by $R_{\rm VI}$, R_N, and the L_2C_2 tank. The Miller approximation is applied to the BB amplifier, resulting in capacitor $(1+A)C_F$, where $A = g_m(r_o||R_{\rm F})$ is the gain of the BB amplifier. The effect of switching before this Miller capacitor is modeled with the L_3C_3 tank, which offers extra OOB rejection. In contrast to a single balanced mixer, we use a balun-driven double-balanced mixer. Now each of the BB components is connected twice per period to the RF source, doubling the conduction time, compared to the single-end case. Therefore, the BB resistance $R_{\rm BB} \approx R_F/(1+A)$ is up-converted and becomes $R_{\rm U} = 2\gamma R_{\rm BB}$, where $\gamma = 2/\pi^2$ for 4-path case [13]. Note that C_p and L_p in (4) and (5) only depend on the number of phases, the BB capacitance in a single path and the LO frequency. The mixer switches up-convert the BB low-pass impedance to an RF bandpass impedance. To be more precise, the switched-RC passive mixer in Fig. 8(a) performs frequency conversion and mixing. For a narrowband in-band signal close to the LO frequency, the capacitors contain a (quasi-) constant BB voltage. Hence a sinewave RF-excitation results in a stair-case waveform response at $V_{\rm IN,RF}$ [1], as shown in the lower left corner of Fig. 8(a). The voltage difference between the sine and stair-case renders a "spiky" current with harmonic content [Fig. 8(a)], which is dissipated in signal-source-resistance $0.5R_s$. This dissipation can be modeled as an "harmonic shunt impedance" $R_{\rm p} \approx 4.3(0.5R_s)$ for the four-phase case [13]. Note that the capacitance of C_A does not affect this in-band R_p. Moreover, as C_B contains almost the same voltage as C_A, there is hardly any difference in the voltage across $0.5R_s$ with or without C_B. Hence, only one R_p suffices to model the in-band loss of both the switched C_A and C_B in this receiver. Using the RLC model for the RX shown in Fig. 8(b) and solving the node equations at $V_{\rm IN,RF}$ and $V_{\rm BPF,RF}$, we derived $H_{\rm o,RF}(s) = V_{\rm BPF,RF}(s)/(V_{\rm s}/2)$ as

$$H_{\rm o,RF}(s) = \frac{2R_{\rm p}(0.5R_{\rm s}+R_{\rm p})^{-1}(C_1C_2C_3R^2R_{\rm A})^{-1}s^3}{s^6+D_{\rm x}s^5+D_{\rm y}s^4+D_{\rm z}s^3+D_{\rm y}\omega_{\rm LO}^2s^2+D_{\rm x}\omega_{\rm LO}^4s+\omega_{\rm LO}^6} \tag{6}$$

$$D_{\rm x} = \frac{2}{C_1R}+\frac{1}{C_2R}+\frac{2}{C_3R}+\frac{1}{C_3R_{\rm U}}+\frac{1}{C_1R_{\rm A}}$$

$$D_{\rm y} = 3\omega_{\rm LO}^2+\frac{L_2L_3(R+R_{\rm U})}{\omega_{\rm LO}^{-4}R^2R_{\rm U}}+\frac{L_1L_2(R+R_{\rm A})}{\omega_{\rm LO}^{-4}R^2R_{\rm A}} + \frac{L_1L_3(R+2R_{\rm U})(R+2R_{\rm A})}{\omega_{\rm LO}^{-4}R^2R_{\rm U}R_{\rm A}}$$

$$D_{\rm z} = \frac{2(L_2R_{\rm U}+L_3(R+2R_{\rm U}))}{\omega_{\rm LO}^{-4}RR_{\rm U}}+\frac{L_1L_2L_3(R+R_{\rm U}+R_{\rm A})}{\omega_{\rm LO}^{-6}R^2R_{\rm U}R_{\rm A}} + \frac{2L_1(R+2R_{\rm A})}{\omega_{\rm LO}^{-4}RR_{\rm A}}$$

where $\omega_{\rm LO}^{-2} = L_1C_1 = L_2C_2 = L_3C_3$, $R_{\rm A} = (0.5R_{\rm s})||R_p$ and $R = R_{\rm VI} = R_N$. Assuming the R_s is given, $R_{\rm VI}$ and R_F are designed to provide in-band matching to it. Channel Bandwidth tuning can be realized by simultaneously changing all the capacitors with the same ratio. Substituting the component values [see Fig. 8(a), top right corner] in (4)–(6), and obtaining the corresponding RLC values, we can find the poles are located at $j\omega_{\rm LO}\pm 2\pi$(5M) rad/s, $j\omega_{\rm LO}\pm 2\pi$(58M) rad/s and $j\omega_{\rm LO}\pm 2\pi$(120M) rad/s. Assuming $R_{\rm F}C_{\rm F} \gg \omega_{\rm LO}^{-1}$, $V_{\rm BB}$ at the BB amplifier input is a down-converted version of $V_{\rm BPF,RF}$, and the voltage gain from $V_{\rm RF}$ to $V_{\rm BB}$ can be derived by dividing [13, eq. (4)] by[13, eq. (6)], resulting $1/\sqrt{4\gamma}$ (= 0.9 dB) where γ is $2/\pi^2$ for four-phase case. Hence, the gain of this

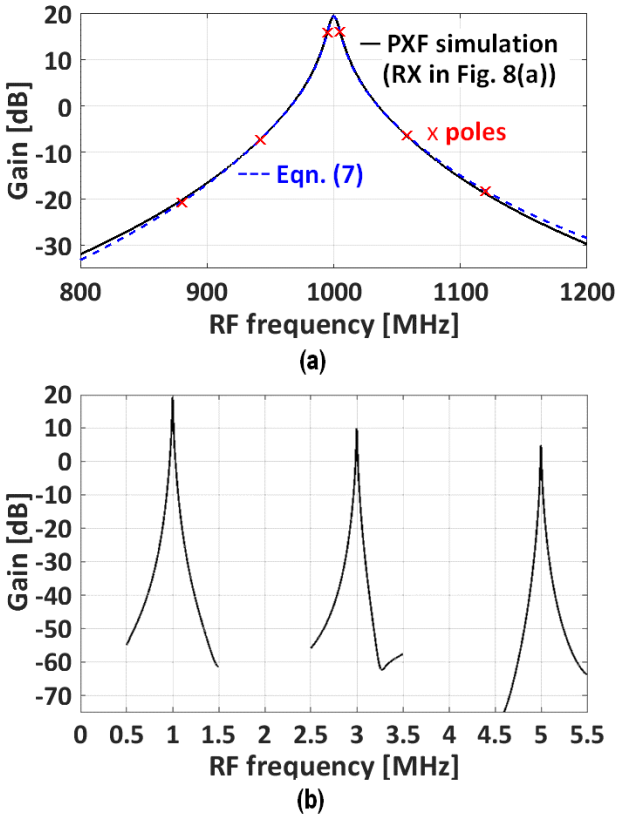


Fig. 9. (a) PXF simulation (sideband: −1, LO = 1 GHz) of the proposed receiver with ideal components and the calculated gain $|V_o/V_s/2|$ in (7). (b) Broadband filter response up to 5th harmonic (sideband: −1, −2, −3, LO = 1 GHz).

receiver can be written as

$$\left|\frac{V_o}{V_s/2}\right| \approx |H_{o,RF}(s)(\sqrt{4\gamma})^{-1} g_m(r_o||R_F)|. \tag{7}$$

To verify analysis, Fig. 9(a) shows a Spectre PSS/PXF simulation result for the receiver circuit in Fig. 8(a) and the estimate of the receiver gain of (7). As $f_{RX} - f_{TX} < 200$ MHz for most LTE frequency bands, we focus on $f_{LO} \pm 200$ MHz, and the fit is satisfactory.

Fig. 9(b) shows the filter response up to the 5th harmonics and the 1st-order roll-off in magnitude can be observed. The 2nd-order harmonic response is rejected due to differential architecture, while odd harmonic rejection is not implemented in this RX design, as in many other four-path I–Q receivers. In principle harmonic rejection can be achieved, as shown for instance in the eight-path receiver in [13].

B. OOB Rejection of the Receiver

In the proposed receiver, the first V–V N-path BPF attenuates blockers but the OOB rejection is limited by the resistance of the mixer switches [1]. Instead of using capacitors to ground, the feedback capacitor across the BB amplifier is used to save area and provide higher feedback factor for better OOB linearity [20]. Here, the OOB rejection is ultimately limited due to the finite transconductance g_m of the BB amplifier. Thanks to the differential circuit symmetry, the BB output nodes $I+$, $Q+$, $I-$, and $Q-$ of the second V–I BPF stage show very low voltage swing, resulting in effective OOB-current by passing [see Fig. 8(a)].

C. Noise Performance

The noise factor F of the receiver can be calculated as the total output noise divided by the noise contribution due to the thermal noise from the antenna or signal source, modeled as $\overline{v_{n,s}^2} = 4\ \mathrm{kTR}_s$. All the mixer switches are equal in Fig. 8(a).The resulting F of this RX can be derived as

$$F = 1 + \frac{(R_{VI}+R_{sw})}{R_s} + \frac{(R_{VI}+R_s+R_{sw})}{4.3R_s} + \frac{(R_{VI}+R_s+R_{sw})^2}{\gamma\,(2R_F)R_s} + \frac{\overline{v_{n,in,A}^2}(4(R_s+R_{VI}+R_{sw})+2R_{BB})^2}{4\ \mathrm{kT}R_s(4\gamma)(2R_{BB})^2}. \tag{8}$$

An explanation is given in the following. The thermal noise of R_N and the corresponding mixer switch is suppressed by the switched capacitor C_B in Fig. 8(a) due to its notch function. The direct noise contribution from thermal noise of R_{VI} and the mixer switch in series is $(R_{VI} + R_{sw})/R_s$. Moreover, noise degradation due to noise folding from odd harmonics of the mixing frequency occurs. Thermal noise of R_s, R_{VI}, and R_{sw} are hence down-converted and sampled [13], leading to a summation of $4kT(R_s + R_{VI} + R_{sw})/n^2$ terms, where $n = 3, 5, 7, \ldots$ for a four-path mixer. This sums up to $\approx 4kT(R_s + R_{VI} + R_{sw})/4.3$. The up-converted noise current induced by the BB feedback resistor R_F renders the term proportional to $1/(2\gamma R_F)$. Note that R_F is much higher than R_s primarily due to the negative feedback. Therefore, the noise contribution of R_F is minor. The input-referred noise of the BB amplifiers is $\overline{v_{n,in,A}^2} = \overline{v_{n,\mathrm{out},A}^2}/A^2$, where $\overline{v_{n,\mathrm{out},A}^2}$ is noise at the BB amplifier output and $\sqrt{(\overline{v_{n,\mathrm{out},A}^2})} = 1.6\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ from simulation. The noise voltage due to source resistance at the BB amplifier input undergoes a voltage division with gain of $\sqrt{4\gamma}$ and it is $\overline{v_{n,s,BB}^2} = 4\ \mathrm{kT}R_s(4\gamma)(2R_{BB}/(4(R_s + R_{VI} + R_{sw}) + 2R_{BB}))^2$, where R_{BB} is $R_F/(1+A)$. Filling the design values in (8), NF of 3.9 dB at very low frequency is obtained.

D. Influence of Parasitic Capacitance at the RF Input Port

Bottom-plate mixing can offer blocker rejection with significantly higher linearity than a conventional top-plate mixing N-path filter. However, it also brings some limitations. There is no isolation by the mixer switch between the RF input and filter capacitors when a switch is in its off-state, complicating the read-out of the BB signal across the capacitors. The floating filter capacitors will have a parasitic capacitance to substrate, which is directly connected to the RF input introducing signal loss[2]. In this design, metal-oxide-metal (MOM) capacitors were used, and the lowest layer was metal 3 instead of 1 to reduce parasitic capacitance. QRC extractions indicate that the parasitic capacitance is about 1.1% of MOM capacitance. As shown in Fig. 8(a), the total MOM

[2]The paracistic capacitance can be put only at bottom plate of the MOM capacitor on the switch side, but this has even larger disadvantage.

capacitance seen by RF input is $4C_A + 4C_B$. Since one of the bottom plates of C_A is connected to the symmetry point when the switch is on, the total MOM parasitic capacitance is $0.011(4C_A \times 7/8 + 4C_B) \approx 4.4$ pF. As large mixer switches were applied for high linearity, substantial extra parasitic MOSFET junction and overlap capacitances are introduced at other nodes. The total unwanted parasitic capacitance C_s that is from RF input $V^+_{IN,RF}$ ($V^-_{IN,RF}$) coupled to ground in Fig. 8(a) is about 5.2 pF. It decreases the harmonic shunt impedance $R_p(\omega_{LO})$ and increases the folded noise [14]. For a four-path mixer-first receiver, $R_p(\omega_{LO})$ can be approximated as [14]:

$$R_p(\omega_{LO}) \approx 4.3R_{sw}(1 + (4R_{sw}C_s\omega_{LO} + R_{sw}/R_s)^{-1}). \quad (9)$$

The reduction of $R_p(\omega_{LO})$ at higher ω_{LO} causes gain, S_{11} and NF degradation. Taking the parasitic capacitance C_s into account, the RX gain as a function of ω_{LO} can be written as

$$\left| \frac{2(R_{in}(\omega_{LO})||(j\omega_{LO}C_s)^{-1})R_U}{(0.5R_s + R_{in}(\omega_{LO})||(j\omega_{LO}C_s)^{-1})(R_{VI} + R_U)} \times (\sqrt{4\gamma})^{-1} g_m(r_o||R_F) \right| \quad (10)$$

where $R_{in}(\omega_{LO})$ is $R_p(\omega_{LO})||(R_{VI} + R_U)$, $R_U = 2\gamma R_F/(1 + A)$, $\gamma = 2/\pi^2$, $A = g_m(r_o||R_F)$ [see Fig. 8(b)].

The parasitic capacitance causes direct input attenuation and more harmonic folding noise [14]. Considering these mechanisms, the noise factor as a function of the LO frequency can be written as

$$F \approx 1 + \frac{(R_{VI} + R_{sw})}{\mathrm{Re}(Z_s)} + \frac{(\mathrm{Re}(R_{VI} + Z_s + R_{sw}))^2}{\mathrm{Re}(Z_s)R_p(\omega_{LO})} \quad (11)$$

where $Z_s = R_s||(j\omega_{LO}C_s)^{-1}$ and $R_p(\omega_{LO})$ can be obtained from (9). Since the BB noise is a minor contribution as discussed in (8), it is neglected in (11).

Note that the center frequency of an N-path filter is controlled by LO; therefore, the parasitic capacitance does not influence the tuning range. However, there is one mixer switch connected to R_N of the notch filter while there are four mixer switches connected to R_{VI} in Fig. 8(a). A difference of parasitic capacitance of three mixer switches in off-state is present. It causes small center frequency difference that slightly degrades gain and noise performance.

V. Measurement Result and Comparison

A test chip was fabricated in 1P7M TSMC 28-nm technology and packaged in a 3×3 QFN package (i.e., the same chip was characterized in [8]). The total chip area including pads and decoupling capacitors is 1 mm^2 while the active area is 0.8 mm^2. Fig. 10 shows the chip micrograph. The external differential clock is applied from the top side, while the RF input-signal is applied from the bottom to reduce coupling. An off-chip 10–8000 MHz 1:1 transformer (Mini-Circuits TCM1-83X+) serves as balun for single-to-differential conversion, while also providing impedance matching to the 50-Ω differential chip input. Both the balun and cable losses were de-embedded for all measurements except the S_{11} measurement.

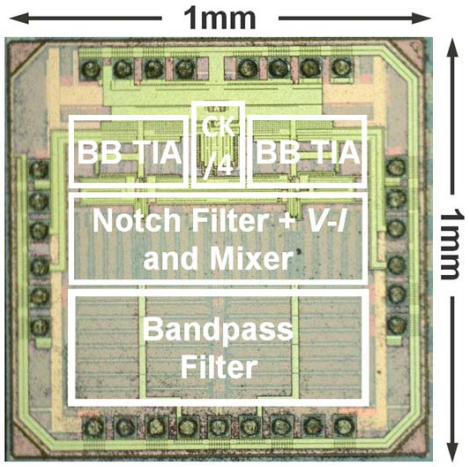


Fig. 10. Chip microphotograph.

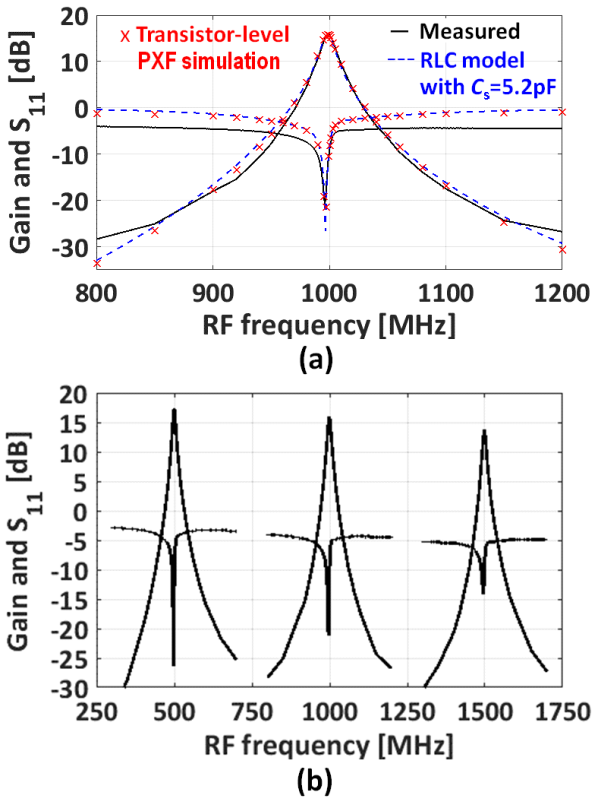


Fig. 11. (a) Measured and simulated gain and S_{11} versus RF frequency ($f_{LO} = 1$ GHz). (b) Measured gain and S_{11} for three LO frequencies.

A. Gain and S_{11}

Because the BB amplifier is not able to directly drive a 50-Ω load, a low-noise external measurement buffer (TELEDYNE LECROY AP033 Active Differential Probe) with differential high-impedance input and single-ended 50-Ω output impedance was added. A weak tone of −50 dBm is applied to the RF input, and the BB output is observed to obtain the conversion gain. Fig. 11(a) shows the measured voltage gain and S_{11} as a function of the RF input frequency for a 1-GHz LO. To compare measurement to theory, the RLC model in Fig. 8(b) was used and a shunt C_s of 5.2 pF

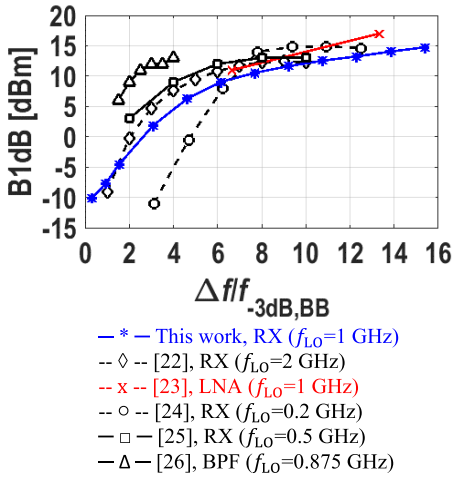


Fig. 12. Measured B1dB as a function of relative blocker frequency offset $\Delta f/f_{-3\text{dB,BB}}$ compared with other blocker-tolerant RF front ends.

is added to the RF input. Applying (9), $R_{\text{p}}(\omega_{\text{LO}})$ becomes 30 Ω. The single ended input impedance of this receiver $R_{\text{in}}(\omega_{\text{LO}})$ is $R_p(\omega_{\text{LO}})||(R_{\text{VI}}+R_{\text{sw}}+2\gamma\, R_{\text{BB}})$, it becomes ≈50 Ω differentially. The receiver conversion gain obtained from the RLC model can be computed by using (6) and (7), while R_p of (6) becomes $R_{\text{p}}(\omega_{\text{LO}})||(j\omega C_{\text{s}})^{-1}$ now. It is observed that both the gain and optimum S_{11} dip are shifted toward lower frequencies due to the presence of C_s, in agreement with the analysis in [13] and [21]. This issue can be addressed by introducing complex feedback with resistors [3] or adding a series inductor [21]. The measured gain is about 16 dB and the $f_{-3\text{dB,BPF}}$ is about 13 MHz ($f_{-3\text{dB,BB}} = 6.5$ MHz), while the filter roll-off from 20- to 200-MHz offset is about −32 dB [−34 dB from (6)] for the upper sideband, and −33 dB [−38 dB from (6)] for the lower sideband.

Note that the deviation between the measured S_{11} and the theoretical prediction is likely due to balun non-idealities. (Simulations were done with an ideal balun model.) Fig. 11(b) shows gain and S_{11} plots over three LO different frequencies to illustrate the filter tuning capability of the receiver.

B. B1dB, IIP2, and IIP3

Fig. 12 shows the measured B1dB as a function of the relative frequency offset $\Delta f/f_{-3\text{dB,BB}}$ for $f_{\text{LO}} = 1$ GHz and a desired signal at 1.001 GHz ($f_{\text{BB}} = 1$ MHz). Already at $\Delta f/f_{-3\text{dB,BB}} > 3$, B1dB is >0 dBm, while for $\Delta f/f_{-3\text{dB,BB}} > 8$, B1dB > +10 dBm. Note that this design only uses a 1.2-V supply. (The design in [23] artificially boosts B1dB by increasing the supply voltage introducing device reliability concerns.) To show this is competitive, Fig. 12 also shows results for several blocker-tolerant receivers that achieved > +10-dBm B1dB [22]–[24].

IIP3 and IIP2 measurements are performed by two-tone tests. Circulators that offer higher than 20-dB isolation are applied between the two blocker signal generators to prevent intermodulation in the test setup, so that over +55-dBm IIP3 was achieved in the test setup itself. For LTE radio applications, the transmitter signal frequency is lower than the receiver frequency for most of the bands. Therefore, the test

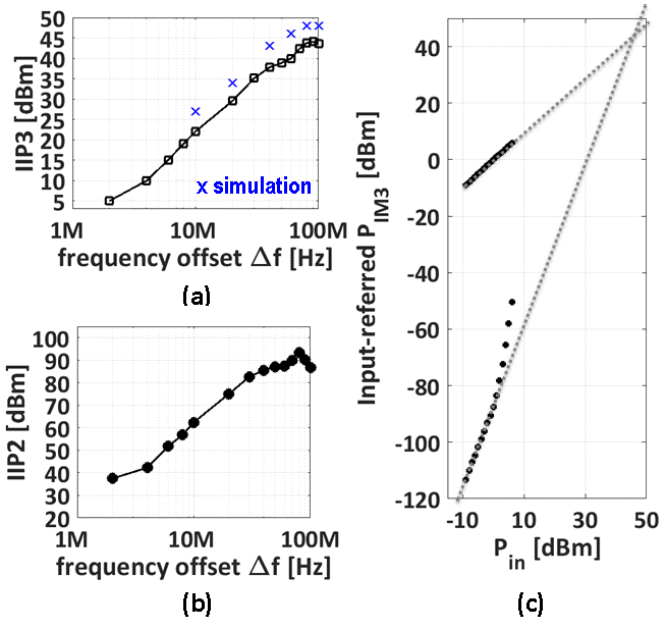


Fig. 13. Measured (a) IIP3, (b) IIP2 versus blocker frequency offset Δf at $f_{\text{LO}} = 1$ GHz, and (c) measured P_{IIM3} versus P_{in} for $\Delta f = 80$ MHz.

tones were chosen at $f_1 = f_{\text{LO}} - \Delta f$ and $f_2 = f_{\text{LO}} - 2\Delta f +$ 500 kHz for IIP3 measurements, and at $f_1 = f_{\text{LO}} - \Delta f$ and $f_2 = f_{\text{LO}} - \Delta f + 500$ kHz for IIP2 measurements. This choice keeps the resulting IM3 or IM2 product at a constant BB frequency of 500 kHz. In a practical wireless communication system such as LTE, the frequency offset between TX and RX in FDD mode is specified in the standard. The very high IIP3 and IIP2 is only required at this specified frequency offset Δf. Measured IIP3 and IIP2 as a function of Δf for a 1-GHz LO are shown in Fig. 13. At $\Delta f = 80$ MHz, very high IIP3 of +44 dBm and IIP2 of +90 dBm are achieved. As shown in Fig. 13(a), there is discrepancy between simulated and measured IIP3. It is due to the circuit mismatch and the amplitude and phase imbalance of the balun. Simulation shows that 10% amplitude imbalance causes 1-dB IIP3 degradation while 10% phase imbalance causes about 2-dB IIP3 degradation. Fig. 13(c) shows the input referred IM3 as a function of the blocker power for a 1-GHz LO and $\Delta f = 80$ MHz. The measured P_{IIM3} follows the extrapolation line up to an input power as high as 0 dBm. Basically $R_{sw} \ll R_s$ is required to achieve such high linearity, causing large switch gate capacitance. As the required power consumption of the clocking circuit to drive switches is proportional to the clock frequency and switch gate capacitance, there is a tradeoff between linearity and LO power.

In this receiver design, phase shifts in the LO between the bandpass and notch mixers will contribute to charge sharing between BB capacitors. To investigate how it influences the linearity, we deliberately add a delay on the LO clock that drives notch filter. Simulation shows that the IIP3 variation of this receiver is kept less than 0.5 dB, NF and gain variations are kept less than 0.1 dB when the clock delay between bandpass and notch is within 5 ps. The possible charge sharing has a minor impact on the linearity.

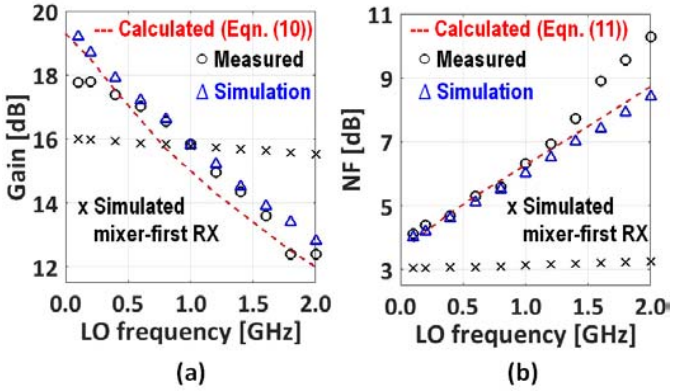


Fig. 14. (a) Gain and (b) DSB NF versus LO frequency of the proposed receiver and the conventional mixer-first receiver [3].

C. NF and Gain Versus LO Frequency

Fig. 14(a) shows the measured and transistor-level (with QRC layout extraction) simulated gain as a function of LO frequency. The gain loss at higher f_{LO} is due to input impedance reduction as a result of parasitic capacitance C_s as discussed in Section IV-D. The measured conversion gain at a low LO frequency of 100 MHz is about 18 dB while the simulated gain is about 19 dB. This deviation is due to variation as a function of frequency in the output impedance of the on-board balun (35 Ω, instead of 50 Ω). As a result, the harmonic shunt impedance and the RF input impedance will be smaller, and the conversion gain at the RF input becomes lower.

NF measurements were performed using the Y-factor method with an external noise source. As shown in Fig. 14(b), at low LO frequency of 100 MHz, NF is 4.2 dB. The parasitic capacitance C_s at RF input is not taken into account in (8) derived in Section IV-C. In the practical circuit, this lowers the impedance seen by the source voltage at higher RF frequencies. Therefore, the source resistance contributes a lower percentage of the total output noise at higher frequencies and NF increases.

The proposed receiver can achieve steeper filter roll-off and better linearity than a conventional mixer-first receiver [3]. However, the gain and NF of the proposed receiver degrade more rapidly at higher operating frequency. The simulated gain and NF as a function of LO frequency for a conventional mixer-first receiver [3] is also shown in Fig. 14 for comparison. Note that the same mixer switch size is applied but smaller BB feedback resistor is used for input matching in the conventional mixer-first receiver [3].

D. Blocker NF

Fig. 15 shows the measured NF as a function of blocker power for 0.7- and 1.3-GHz LO-frequency, while the blocker offset was 80 MHz. The measured desensitization is only 0.6 dB for a 0-dBm blocker and 3.5 dB for a 10-dBm blocker at 0.7-GHz LO. Overall, the presence of strong blockers degrades NF due to reciprocal mixing and gain compression. Since the measured B1 dB is as high as +13 dBm, the blocker NF degradation is most likely due to reciprocal mixing which is proportional to blocker power and phase noise of LO. To obtain satisfactory measured blocker NF, two external

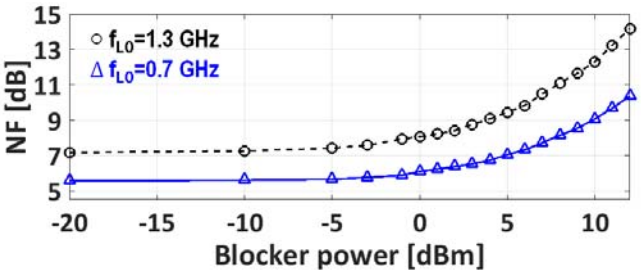
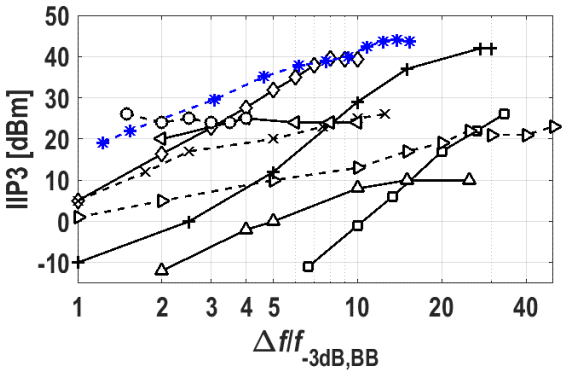


Fig. 15. Measured blocker NF (blocker frequency offset $\Delta f = 80$ MHz) for $f_{\mathrm{LO}} = 0.7$ GHz and $f_{\mathrm{LO}} = 1.3$ GHz.



—*— This work, (NF=6.3dB@1GHz)
-- ◊ -- [22], NF=2.8dB@2GHz
-- x -- [2], NF=3 dB@1GHz
— □ — [5], NF=2.9dB@1.5GHz
-- ▷ -- [28], NF=3.5dB@1GHz
— Δ — [29], NF=2.9dB@1.5GHz
— + — [30], NF=6dB@0.2GHz
— ◁ — [25], NF=7dB@0.5GHz
-- ○ -- [26], NF=5dB@0.875GHz

Fig. 16. IIP3 benchmark of blocker-tolerant RF front ends as a function of $(\Delta f/f_{-3\mathrm{dB,BB}})$.

tunable narrowband BPFs in cascade were applied to the output of the signal generators used to supply 4 × LO for ensuring low phase noise. The clocking circuit consumes about 33 mW/GHz from 1.2-V supply to achieve a simulated phase noise of −170 dBc/Hz for 1-GHz LO at 80-MHz offset frequency. As also discussed in [27], generating an LO with such strict requirements is one of the biggest challenges of passive mixing SAW-less receiver designs.

E. Performance Comparison

Fig. 16 shows an IIP3 benchmark of blocker-tolerant RF front ends as a function of $\Delta f/f_{-3\mathrm{dB,BB}}$. The proposed bottom-plate mixing N-path filter with switch sharing improves both in-band and OOB linearity. Hence, this design achieves the highest reported linearity while achieving a moderate NF of 6.3 dB for a 1-GHz LO. A detailed performance summary and comparison is shown in Table I. Compared to prior art, the receiver achieves higher IIP3 and IIP2 for comparable NF and power consumption. This confirms the effectiveness of the higher order RF filtering provided by the proposed cascading of passive V–V and V–I N-path BPFs as well as the linearity improvement by bottom-plate mixing and switch sharing.

TABLE I
RESULT SUMMARY AND COMPARISON WITH PRIOR ARTS

	*JSSC*10[3]	*JSSC*12[19]	*JSSC*13[2]	*RFIC15*[6]	*RFIC15*[5]	*RFIC15*[23]	*RFIC17*[22]	*ISSCC17*[25]	*ISSCC18*[26]	This Work
Circuit type	Receiver	Receiver	LNA/Filter	Receiver	Receiver	LNA/Filter	Receiver	Receiver	BPF	Receiver
Technology	65nm	40nm	65nm	28nm	65nm	32nm SOI	45nm SOI	65nm	65nm	28nm
f_{RF}[GHz]	0.1-2.4	0.08-2.7	0.1-1.2	0.4-3.5	0.7-3.8	0.4-6	0.2-8	0.1-1	0.8-1.1	0.1-2.0
Gain[dB]	40-70	72	25	35	40	12	21	23	NA	16
BB BW[MHz]	10	2	4	15-50	5	7.5	10	5	20	6.5
OOB IIP3[dBm]	25 Δf/BW=10	10 Δf/BW=5 13.5 Δf/BW=40	20 Δf/BW=5 26 Δf/BW=12.5	20.5 Δf/BW=3.3	0 Δf/BW=6 26 Δf/BW=20	36 Δf/BW=6.7	39 Δf/BW=8	21 Δf/BW=2.4 24 Δf/BW=6	24 Δf/BW=2 25 Δf/BW=4	35 Δf/BW=4.6 44 Δf/BW=12.3
OOB IIP2[dBm]	56	55	NA	64	65	NA	88	64	NA	90
B1dB[dBm]	10 Δf/BW=10	−6 Δf/BW=5 −2 Δf/BW=40	2 Δf/BW=5 7 Δf/BW=12.5	4.6 Δf/BW=3.3	−20 Δf/BW=6 3 Δf/BW=20	11 Δf/BW=6.7	12 Δf/BW=8	5 Δf/BW=2.4 12 Δf/BW=6	9 Δf/BW=2 13 Δf/BW=4	6 Δf/BW=4.6 13 Δf/BW=12.3
NF[dB]	4±1	1.9 (@2GHz)	2.8	2.4-2.6	2.5-4.5	3.6-4.9	2.3-5.4 (0.5-6GHz)	7	5.0-8.6	4.1-10.3
0dBm Blocker NF	NA	4.1dB @1.5GHz	NA	6.5dB @2GHz	NA	NA	4.7dB @1.4GHz	NA	NA	8.1dB @1.3GHz
Supply[V]	1.2/2.5	1.2/2.5	1.2	1/1.5	1.2	2	1.2	1.2/1	NA	1.2/1.0
Power [mW]	37-70	27-60	15-48	38-75	27-75	81-209	LO: 30mW/GHz BB Amp: 50mW	64-84	80-97	34-96 LO: 33mW/GHz BB Amp: 30mW

VI. CONCLUSION

In this paper, a high-linearity receiver combining 2-stage N-path filtering with passive mixing is proposed, analyzed, implemented, and evaluated. The N-path filter is a cascade of a passive V–V and a V–I BPF, enhancing selectivity. Very high linearity is achieved exploiting a bottom-plate mixing technique that improves both in-band and OOB linearity. Switch sharing further improves linearity and can offer an additional 9-dB IIP3 enhancement. Implemented in 28-nm CMOS, a high-linearity RX achieving +44-dBm IIP3, +90-dBm IIP2, +13-dBm B1dB with moderate NF of 6.3 dB at 1-GHz LO frequency is demonstrated, offering robustness to strong TX leakage.

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