Guest Editorial: Special Section on the 48th European Solid-State Circuits Conference (ESSCIRC)

THIS Special Section of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) features expanded versions of papers selected from those presented at the 48th ESSCIRC Conference, held at Technische Universität Dresden, Dresden, Germany, during September 3–6, 2018.

The aim of ESSCIRC, held in conjunction with the European Solid-State Device Research Conference (ESSDERC), is to provide an annual European forum for the presentation and discussion of advances in solid-state circuits and devices. The increasing level of integration for system-on-chip design made available by the advances in semiconductor technology is, more than ever before, calling for deeper interaction among technologists, device experts, IC designers, and system designers. While having separate technical program committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities.

The selection of papers was done by the Guest Editors based on the input from the TPC Committee, the session chairs, and the audience feedback. Corresponding authors were invited to provide extended version including additional details on methods, architectures, circuits, measurements, and benchmarking data. All papers were peer-reviewed according to the regular JSSC procedure.

Papers from all ESSCIRC topics are included in the Special Section and can be roughly grouped into four categories. The first one "Analog, Data Converters and Sensors" includes papers covering a wide variety of topics and technologies, from bandgap references to single photon counting imagers. A capacitance-to-digital converter, a T&H frontend for Hall sensors, a time-based temperature sensor, a bridge for magnetic sensing applications, an ECG recording system, and a readout for touch sensors are also presented in this category. The second category, "Communications," includes papers addressing spread spectrum transceivers, SAW-less receivers, Class-G PAs, relaxation oscillator design, and dielectric waveguide communication links, respectively. In the third category, "Processors," three papers describing different processor architectures in deep submicrometer are included. Namely, a low-power, parallel SoC core for IoT; a deep neural networks (DNN) processor; and an SoC for spectral analysis. The last category, "Power Management" includes a paper on ac–dc converters.

The Guest Editors would like to acknowledge the contributions of all the papers submitted to the conference. We also wish to express our greatest appreciation to the authors of the selected papers for their commitment to write and revise their manuscripts under a tight publication schedule. We would also like to thank the anonymous reviewers for their constructive feedback to help improve the quality of the manuscripts. Special thanks go to the ESSCIRC 2018 TPC Chairs, R. Thewes, R. Brederlow and B. Staszewski, the Track Chairs as well as J. Craninckx, JSSC Editor-in-Chief, together with the JSSC Administration M. Erickson and A. Levinson for their excellent assistance.

We hope that this Special Section gives the readers a flavor of the state-of-the-art developments in integrated circuit design at the circuit, system, and application levels. We encourage the readers to attend ESSCIRC/ESSDERC 2019, which will be held in Krakow, Poland, during September 23–26, 2019.

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Ángel Rodríguez-Vázquez (F'99) co-founded the Instituto de Microelectrónica de Sevilla, Seville, Spain, a joint undertaking of Consejo Superior de Investigaciones Científicas (CSIC), Spain, and Universidad de Sevilla, Seville, Spain, and started a Lab on Analog and Mixed-Signal Circuits for Sensors and Communications. In 2001, he was the main Promotor of AnaFocus Ltd., Sevilla, Spain, and served as the CEO until 2009, when the company reached maturity as a worldwide provider of smart CMOS imagers. He also participated in the foundation of the Hungarian startup, AnaLogic Ltd. AnaFocus was founded on the basis of his patents on vision chip architectures. He also produced teaching materials on data converters that were delivered to companies and got the Quality Label of EuroPractice. He has authored or coauthored more than 9500 citations. He has filed nine patents. His research and development production includes three generations of vision chips, analog front ends for XDSL MoDems, ADCs for wireless communications, ADCs for automotive sensors, and complete MoDems for power-line communications, among many other mixed-signal SoCs. Many of these chips were state-of-the-art in their respective fields. Some of them entered massive production.

Mr. Rodríguez-Vázquez was a recipient of several awards: the IEEE Guillemin-Cauer Best Paper Award, two Wiley's IJCTA Best Paper Awards, the two IEEE ECCTD Best Paper Awards, the IEEE-ISCAS Best Paper Award, the SPIE-IST Electronic Imaging Best Paper Award, the IEEE ISCAS Best Demo-Paper Award, and the IEEE ICECS Best Demo-Paper Award. He has an h-index of 47 and an i10-index of 192 (Google Scholar). He was also a recipient of the 2019 Mac Van Valkenburg Award of IEEE-CASS.

Kaushik Sengupta (SM'17) received the B.Tech. and M.Tech. degrees in electronics and electrical communication engineering from IIT Kharagpur, Kharagpur, India, in 2007, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2008 and 2012, respectively.

In 2013, he joined the Department of Electrical Engineering, Princeton University, Princeton, NJ, USA, as a Faculty Member. His current research interests include high-frequency ICs, electromagnetics, and optics for various applications in sensing, imaging, and high-speed communication.

Dr. Sengupta was a recipient of the DARPA Young Faculty Award in 2018, the Bell Labs Prize in 2017, the Young Investigator Program Award from the Office of Naval Research in 2017, the E. Lawrence Keys, Jr./Emerson Electric Co. Junior Faculty Award from Princeton School of Engineering and Applied Science in 2018, and the Excellence in Teaching Award in 2018 nominated by the Undergraduate and Graduate Student Council in Princeton School of Engineering and Applied Science. He was also a recipient of the Charles Wilts Prize in 2013 from the Department of Electrical Engineering, Caltech, for the Best Ph.D. Thesis, the Caltech Institute Fellowship and the Prime Minister Gold Medal Award of the IIT Kharagpur in 2007, the IBM Ph.D. Fellowship in 2011 and 2012, the IEEE Solid State Circuits Society Predoctoral Achievement Award in 2012, the IEEE Microwave Theory and Techniques Graduate Fellowship in 2012, and the Analog Devices Outstanding Student Designer Award in 2011, the Most Innovative Student Project Award of the Indian National Academy of Engineering in 2007, and the IEEE Microwave Theory and Techniques Undergraduate Fellowship in 2006. He was selected five times to the Princeton Engineering Commendation List for Outstanding Teaching in 2014 and 2016–2018. He was a co-recipient of the IEEE RFIC Symposium Best Student Paper Award in 2012 and the 2015 Microwave Prize from IEEE Microwave Theory and Techniques Society. He serves on the Technical Program Committees for the IEEE Custom Integrated Circuits Conference (CICC), the IEEE European Solid-State Circuits Conference (ESSCIRC), Progress in Electromagnetics Research (PIERS), and International Conference on Communications (ICC) workshops. He serves as a member on the MTT-4 Committee of Terahertz Technology and Applications in IEEE Microwave Theory and Techniques Society and a Distinguished Lecturer for the IEEE Solid-State Circuits and Systems Society.

Stefan Rusu (M'85–SM'01–F'07) received the M.S.E.E. degree from Polytechnic University, Bucharest, Romania.

He was with Intel Corporation, Santa Clara, CA, USA, for more than 23 years, where he was experienced in VLSI circuit design and was with Sun Microsystems, Mountain View, CA, USA, for six years.

He is currently a Senior Director with TSMC Technology, Inc., San Jose, CA, USA. He developed key technologies that were adopted across multiple processor designs, including differential clocking, thermal mapping, adaptive clock deskew, cache leakage shut-off, serial VID, and yield recovery for core, cache, and I/O circuits. He has authored more than 95 papers on VLSI circuit technology. He holds 48 U.S. patents.

Mr. Rusu is a member of the Technical Program Committees of the ESSCIRC and A-SSCC Conferences. He was a recipient of the ISSCC Beatrice Winner Award for Editorial Excellence in 2009 and the Chapters Coordinator for the Solid-State Circuits Society AdCom. He served as an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2005 to 2015.