Introduction to the Special Section on the 2019 IEEE International Solid-State Circuits Conference (ISSCC)

I. Introduction

IT HAS been an annual tradition ever since the start of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) in 1966 to publish extended manuscripts of a selected set of articles presented at the annual International Solid-State Circuits Conference (ISSCC). In this November issue, you will find selected articles from the Imagers, Medical, MEMS, and Displays (IMMD) and the Technology Directions (TD) sessions. Most of the bio-related articles are covered in these topics. Next month, the sessions of Analog, Power Management, Data Converters, RF, and Wireless will be covered, and in January, you will find the selected articles from the Wireline, Digital Circuits, Digital Architectures and Systems, and Memory subcommittees.

II. Imagers, Medical, MEMS, and Displays

This section includes six articles selected from the IMMD sessions presented at the ISSCC 2019. The selection contains four articles that report the latest advances in CMOS image sensors for a wide range of applications, such as the Internet of Things (IoT), object detection in embedded systems, light detection and ranging (LIDAR) or 3-D imaging, as well as neural imaging. The other two articles report on biomedical electronics for wearable health monitoring and high-performance molecular testing. The first article reports a low-power image sensor for IoT applications that supports near-pixel motion detection run on a heavily sub-sampled frame (32×20 pixels), while consuming only 1.7 nJ/frame. The second article reports a low-power image sensor for always-on object detection with a readout scheme that extracts logarithmic intensity gradients at 1.5 or 2.75 bit of resolution. The third article reports a 256×256 single-photon avalanche diode (SPAD) image sensor integrated into a 3-D-stacked process for flash LIDAR or high-speed direct time-of-flight 3-D imaging. The fourth article reports an implantable CMOS neural imaging probe in which 512 SPADs are distributed along two shanks with a 6-bit depth in-pixel memory and an on-chip digital-to-time converter. The fifth article reports a bioimpedance readout IC with a wide-input impedance range that employs a digital-assisted baseline cancellation technique to enable vital sign acquisition using a two-electrode setup as opposed to the more conventional four-electrode setup. Finally, the last article reports a CMOS electrochemical biochip for high-performance molecular testing that includes an array of 32×32 three-electrode voltammetry pixels and on-chip temperature control between 25 °C and 95 °C. Results from DNA melt-analysis and real-time label-free DNA hybridization detection are reported.

III. Technology Directions

This section includes six articles selected from the TD sessions presented at the ISSCC 2019. The selection includes an eclectic mix of articles highlighting advances in non-volatile memory integration, acoustic voice activity detection, neural recording systems, magnetic human body communication (mHBC) transceivers, 3-D-integrated optical phased arrays, and superconductive qubit controllers. The first article presents the first-known integrated non-volatile FPGA, CPU, and STT-MRAM with the lowest average power consumption, while the second article features a voice and acoustic activity detector using mixer-based architecture and an ultra-low power neural network-based classifier, achieving 91.5%/90% speech/non-speech hit rate at 10-dB SNR with only 142-nW power consumption. The third article describes a 0.8-mm^3 neural recording system that is powered by and communicates via ultrasound. A linear AM backscatter technique is introduced that enables operation at a depth of up to 5 cm. The fourth article presents a transceiver design to exploit the low path loss enabled by mHBC. A test chip demonstrates reliable trans-body communication at 5 Mb/s at TX and RX power consumptions of 18.56 and 6.3 μW, respectively. The fifth article presents an optical phased array implemented in a 3-D platform, where photonics and CMOS, independently optimized, are oxide-bonded and connected through high-density vias. With 18.5°/16° steering range and 0.15°/0.6° beamwidth, the system achieves an effective antenna aperture of 500 μm $\times$ 130 μm resulting in a lateral resolution of 0.26 m $\times$ 1 m at 100 m. The last article describes a chip designed to control superconductive qubits by means of 4–8-GHz signal patterns operating at deep-cryogenic temperatures (3 K). The 28-nm cryo-CMOS chip generates up to 16 waveforms to perform several gate operations on qubits, dissipating less than 2 mW/qubit.

The Guest Editors would like to express their sincere appreciation to all the authors and anonymous reviewers for contributing their efforts and time to ensure high-quality manuscripts under a tight schedule. They would also like to thank all the members of the IMMD and TD international technical program subcommittees (ITPCs) and the session chairs for their help in scoring the articles for selection. Finally, they would like to thank Jan Craninckx, the former JSSC Editor-in-Chief, and Pavan Hanumolu, the current Editor-in-Chief for their guidance, and Ania Levinson and the JSSC staff for their invaluable assistance in publishing this Special Issue.

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In 2005, he joined Case Western Reserve University, Cleveland, OH, USA, where he is currently a Professor and the Interim Chair of the Electrical, Computer, and Systems Engineering (ECSE) Department, with a secondary appointment in the Biomedical Engineering Department. He has authored two book chapters and over 105 refereed technical and scientific articles. He holds six issued and pending patents. His research interests include analog/mixed-signal/RF integrated circuits and microsystems for neural engineering, wireless sensing/actuating systems for brain–machine interfaces, interface circuits for micro-/nano-scale sensors/actuators, and point-of-care diagnostic platforms for personalized health.

Dr. Mohseni was a member of the Technical Program Committee (TPC) of the IEEE Radio Frequency Integrated Circuits Symposium from 2012 to 2015 and the IEEE Custom Integrated Circuits Conference from 2012 to 2019, and has been a member of the TPC of the International Solid-State Circuits Conference since 2017. He has been a member of the IEEE Solid-State Circuits, Circuits and Systems, and Engineering in Medicine and Biology Societies. He was a member of the Administrative Committee of the IEEE Sensors Council from 2014 to 2017. He was a recipient of several awards, including the National Science Foundation CAREER Award, the Case School of Engineering Research Award, the First-Place Prize of the Medical Device Entrepreneur's Forum at the 58th Annual Conference of the American Society of Artificial Internal Organs, and the ECSE Mihajlo "Mike" Mesarovic Award for Extraordinary Impact. He was the TPC Co-Chair of the IEEE BioCAS Conference in 2017 and the General Co-Chair of the conference in 2018. He has been an associate editor and a guest editor of several IEEE journals since 2008.

Sriram Vangal (M'90–SM'13) received the B.E. degree in electrical engineering from Bangalore University, Bengaluru, India, in 1993, the M.S. degree in electrical engineering from the University of Nebraska, Lincoln, NE, USA, in 1995, and the Ph.D. degree in electrical engineering from Linköping University, Linköping, Sweden, in 2007.

In 1995, he joined Intel Corporation, Hillsboro, OR, USA, where he has played a lead role in multicore high-performance "tera-scale" CPU development and ultra-low-power silicon research. He was the Research Lead for the industry's first monolithic 80-core, sub-100 W "Polaris" TeraFLOPS network on chip (NoC), and the 48-IA core "Rock Creek" single-chip cloud computer (SCC) and developed the first near-threshold voltage (NTV) IA silicon. He is currently a Principal Engineer with Intel Labs, Hillsboro, where he is researching energy-efficient computing silicon. He has authored or coauthored over 35 conference and journal articles and three book chapters, and holds over 30 patents.

Dr. Vangal is a member of the IEEE Solid-State Circuits Society. He was a recipient of two Intel Achievement Awards for his work and the Gordon Moore Award for the most impactful research prototype. He was the Co-Chair of the 2018 International Symposium on NoCs.