Introduction to the Special Issue on the 2019 IEEE International Solid-State Circuits Conference (ISSCC)

I. Introduction

THIS SPECIAL Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is dedicated to a collection of the best articles selected from the 2019 IEEE International Solid-State Circuits Conference (ISSCC) that took place on February 17–21, 2019, in San Francisco, CA, USA. This issue covers articles from the Analog, Power Management, Data Converters, RF, and Wireless Committees.

Analog Articles

Four articles have been selected from two sessions on analog techniques and sensor interfaces. The first article introduces an oscillator architecture that enables sub-nW power consumption in a 32-kHz crystal oscillator (XO) by amplifying the oscillation signal at dc, instead of the oscillation frequency. The second article presents a way to improve start-up time of crystal oscillators. The proposed two-step injection technique reduces the crystal oscillator start-up time to within 1.5× the theoretical minimum, achieving a start-up time of <20 μs across a temperature range from -40 °C to 85 °C. The third article presents an ac energy measurement front end that can continuously monitor and report on the accuracy of the measurement system. It can measure rms current to 0.1% accuracy over a 1000:1 dynamic range and active energy to 0.25% accuracy over a 5000:1 dynamic range over the full supply and temperature range while monitoring the system accuracy in the background. The last article introduces a hybrid voltage reference with BGR and CMOS, which incorporates the process skew compensation by utilizing a dimension-dependent effect of the process skew on the threshold voltage. The voltage reference is verified in three wafers of a 0.18-μm CMOS and the measurements show untrimmed process, voltage, temperature (PVT) variations of 0.53%, 0.020%/V, and 33 ppm/°C.

Power Management Articles

Seven articles have been selected from three sessions on power management, including dc–dc converters, wireless power transfer, power amplifiers, and energy harvesting. A dc–dc converter utilizes the parasitic inductance of a USB cable to provide two output voltages suitable for charging one- or two-cell batteries. An EMI optimized 8.3-MHz GaN-based dc–dc converter suppresses the output voltage jittering from 240 mV to below 10 mV. A fully integrated dc–dc converter with nH-scale air-core inductors in 14-nm CMOS achieves a peak efficiency of 88% for 1.6–1.2-V conversion at 70 MHz. Isolated power transfer >1 W with 52% peak efficiency and 5-kV galvanic isolation is demonstrated using an on-chip transformer with magnetic core, passing CISPR 22 Class-B. An envelope modulation combines a hysteretic-controlled three-level switching converter and a slew-rate enhanced linear amplifier to support switching frequencies of 80 MHz with a peak efficiency of 91%. Two articles present energy-harvesting interface circuits for piezoelectric and thermoelectric energy harvesting, respectively, with improved power extraction and conversion efficiency over a wide input range.

Data Converter Articles

In the data converter category, four articles from two sessions were selected, each tackling a different challenge in this field. The first article substantially reduces the required input capacitance of the converter without incurring a large sampled noise penalty by using a continuous-time SAR-based first stage, thereby avoiding a front-end sample-and-hold. The second article describes the first time-interleaved noise-shaping SAR converter, achieving bandwidth previously out of reach for this class of converter. The third article introduces a voltage/time hybrid two-step architecture to enhance the conversion rate at low supply voltage while still retaining PVT robustness. The final article describes how a ring amplifier can be used in a precision data converter that achieves over 90-dB SNDR.

Radio Frequency Articles

The seven invited RF articles have been selected from three sessions and cover topics, including RF and 5G power amplifiers and RF and millimeter-wave (mm-wave) frequency synthesizers. Wang *et al.* presented a mixed-signal Doherty power amplifier architecture for simultaneous linearity and efficiency enhancement. El-Aassar *et al.*presented a dc-to-108-GHz CMOS SOI distributed power amplifier and modulator driver. Zhang *et al.* presented a watt-level multi-subharmonic switching digital power amplifier architecture for enhancing power back-off efficiency. Kim *et al.*presented an ultra-low-jitter, mm-wave frequency synthesizer based on digital sub-sampling phased-locked loop (PLL) that employs optimally spaced voltage comparators. Liu *et al.* presented fractional-N digital PLL (DPLL) achieving 265-μW ultra-low-power operation. Bertulessi *et al.* described the implementation of a CMOS 30-GHz digital sub-sampling fractional-N PLL with -238.6-dB jitter-power figure of merit. Finally, Shi *et al.*

Digital Object Identifier 10.1109/JSSC.2019.2946496

demonstrated a CMOS 16-GHz frequency-modulated continuous waveform (FMCW) modulator based on subsampling PLL for radar applications.

Wireless Articles

Six articles selected from the wireless subcommittee focus on advanced design techniques for low-power and high-data-rate mm-wave transceivers. The first article describes a wake-up receiver in 65-nm CMOS using a 40-stage MOS RF envelope detector and time-domain windowed integrator achieving −78-/−79-dBm sensitivity at 151/434 MHz while consuming 370/420 pW from 0.4 V. The second article presents the first full-duplex 2×2 MIMO receiver consisting of integrated circulator and self-interference cancellation with shared delay time in baseband. Next, a 14-nm FinFET CMOS RFIC with 14RX and 2TX paths that supports 2G, 3G, LTE, and SA/NSA sub-6-GHz 5G NR achieving the peak data of 3.15-Gb/s DL and 1.27-Gb/s UL is reported. The fourth article proposes a novel approach to extend spatial cancellation to mm-wave frequencies using cascaded spatial filters that support Gb/s MIMO operation at 27–41-GHz carrier frequencies. A 28-nm CMOS 60-GHz digital polar transmitter with on-chip pulse shaping with an on-PCB dual-polarization antenna transmits 28.2-Gb/s data is reported in the fifth article. Finally, the last article presents a 300-GHz transceiver in 40-nm CMOS with the data rate of 80 Gb/s over a distance of 3 cm.

Acknowledgment

The Guest Editors wish to thank the IEEE ISSCC session chairs for providing article recommendations, the ITPC members for reviewing the submitted ISSCC articles, including those selected here, the IEEE ISSCC audience for rating the articles at the conference, and, finally, the anonymous reviewers for their valuable comments and article reviews.

YOUNGCHEOL CHAE, *Guest Editor*
Department of Electrical and Electronic Engineering
Yonsei University
Seoul 03722, South Korea
e-mail: ychae@yonsei.ac.kr

BERNHARD WICHT, *Guest Editor*
Institute of Microelectronic Systems
Leibniz University
30167 Hannover, Germany
e-mail: bernhard.wicht@ims.uni-hannover.de

BOB VERBRUGGEN, *Guest Editor*
Xilinx
Dublin, Ireland
e-mail: bob.verbruggen@xilinx.com

PAYAM HEYDARI, *Guest Editor*
Department of Electrical Engineering
and Computer Science
University of California at Irvine
Irvine, CA 92697-2625 USA
e-mail: jssc.heydari@gmail.com

HOWARD LUONG, *Guest Editor*
Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology
Hong Kong
e-mail: eeluong@ust.hk

Youngcheol Chae (M'09–SM'19) received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2003, 2005, and 2009, respectively.

From 2009 to 2011, he was a Post-Doctoral Researcher with the Delft University of Technology, Delft, The Netherlands. Since 2012, he has been a Faculty Member with Yonsei University, where he is currently an Associate Professor. His work has focused on data converters, sensor interfaces, and CMOS imagers, and has resulted in more than 80 technical articles. He holds over 30 patents.

Dr. Chae is a member of the Technical Program Committee of the International Solid-State Circuits Conference and the Asian Solid-State Circuits Conference. He was a recipient of the Best Young Professor Award in Engineering from Yonsei University in 2018, the Haedong Young Engineer Award from the IEE Korea in 2017, the Outstanding Research Awards of Yonsei University in 2017 and 2018, the Outstanding Teaching Awards of Yonsei University in 2013 and 2014, the Research Grant from the Samsung Research Funding Center in 2017, and the VENI Grant from the Dutch Technology Foundation STW in 2011. He is also a Distinguished Lecturer of the IEEE Solid-State Circuits Society.

Bernhard Wicht received the Dipl.Ing. degree in electrical engineering from the Dresden University of Technology, Dresden, Germany, in 1996, and the Ph.D. degree *(summa cum laude)* from the University of Technology Munich, Munich, Germany, in 2002.

He has over 20 years of experience in the analog and power management integrated circuit (IC) design. From 2003 and 2010, he was with Texas Instruments, Freising, Germany, where he was responsible for the design of automotive power management ICs. In September 2010, he became a Full Professor of integrated circuit design and a member of the Robert Bosch Center for Power Electronics, Reutlingen University, Reutlingen, Germany. Since April 2017, he has been heading the Chair for Mixed-Signal IC Design, Leibniz University, Hannover, Germany. He invented 17 patents with several more pending. His research interest includes IC design with a focus on power management, gate drivers, and high-voltage ICs.

Dr. Wicht currently serves as a member of the Technical Program Committee of ESSCIRC and the IEEE International Solid-State Circuits Conference (ISSCC). He was a co-recipient of the 2015 ESSCIRC Best Paper Award and the 2018 First Prize Paper Award of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was recipient of the Faculty Award for Excellent Teaching at his university in 2018.

Bob Verbruggen received the M.S. and Ph.D. degrees in electrical engineering from the Vrije Universiteit Brussel in 2005 and 2010, respectively.

During his Ph.D. studies, he worked on high-speed calibrated analog-to-digital converters at the Smart Systems and Energy Technology Group, imec. From 2010 to 2014, he was a Researcher with imec, working on analog-to-digital converters for software-defined radio systems. In 2014, he joined Xilinx, Dublin, Ireland, to work on high-performance RF data converters.

Dr. Verbruggen has been serving on the Data Converters Subcommittee of the IEEE International Solid-State Circuits Conference since 2016.

Payam Heydari (M'01–SM'09–F'17) received the Ph.D. degree from the University of Southern California, Los Angeles, CA, USA, in 2001.

He is currently a Full Professor of electrical engineering with the University of California at Irvine (UC-Irvine), Irvine, CA, USA. His group created the world's first fundamental frequency CMOS transceiver operating above 200 GHz. He is the (co)author of two books, two book chapters, and more than 150 journal and conference articles. His research covers the design of terahertz/millimeter-wave/RF and analog integrated circuits.

Dr. Heydari was a member of the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC). He is a member of the Technical Program Committee of the IEEE Custom Integrated Circuits Conference (CICC). He was a recipient of the 2016–2017 UCI's School of Engineering Mid-Career Excellence in Research, the 2014 Distinguished Engineering Educator Award from the Orange County Engineering Council, the 2009 Business Plan Competition First Place Prize Award and the Best Concept Paper Award from the Paul Merage School of Business, UC-Irvine, the 2010 Faculty of the Year Award from the UC-Irvine's Engineering Student Council (ECS), the 2009 School of Engineering Best Faculty Research Award, the 2007 IEEE Circuits and Systems Society Guillemin-Cauer Award, the 2005 IEEE Circuits and Systems Society Darlington Award, and the 2005 National Science Foundation (NSF) CAREER Award. He serves on the AdCom of the IEEE Solid-State Circuits Society. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I. He serves as an Associate Editor and a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and an Associate Editor for the IEEE SOLID-STATE CIRCUITS LETTERS. He was a Distinguished Lecturer of the IEEE Solid-State Circuits Society from January 2014 to January 2016. He is also a Distinguished Microwave Lecturer of the IEEE Microwave Theory and Techniques Society for the period of January 2019 to December 2022.

Howard Luong (F'14) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences (EECS) from the University of California at Berkeley, Berkeley, CA, USA, in 1988, 1990, and 1994, respectively.

In September 1994, he joined the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong, where he is currently a Professor. In 2014, he was appointed as the MediaTek Endowed Visiting Professor in IC design at Nanyang Technology University, Singapore. His research interests are in RF and millimeter-wave (mm-wave) integrated circuits and systems for wireless and medical applications. He has coauthored three technical books, *Design Techniques for Transformer-Based VCOs and Frequency Dividers*, *Low-Voltage RF CMOS Frequency Synthesizers*, and *Design of Low-Voltage CMOS Switched-Opamp Switched-Capacitor Systems*.

Dr. Luong serves as a Technical Program Committee Member of the IEEE International Solid-State Circuits Conference (ISSCC). He also serves as an Associate Editor for the IEEE SOLID-STATE CIRCUITS LETTERS (SSCL) and the IEEE RFIC VIRTUAL JOURNAL (VJ-RFIC). He was a Distinguished Lecturer of the IEEE Solid-State Circuits Society from 2012 to 2014.