# Introduction to the Special Issue on the 2019 Symposium on VLSI Circuits

THIS Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS highlights some of the best papers presented at the 33rd Symposium on VLSI Circuits, held on June 10-14, 2019, at Rihga Royal Hotel Kyoto, Kyoto, Japan. Industry and university engineers from all over the world reported innovative new techniques and state-of-the-art results. Articles presented covered a broad range of topics important to VLSI circuit and system designers, including topics also important to integrated circuit technology developers.

Founded in 1987, the Symposium on VLSI Circuits is jointly sponsored by the IEEE Solid-State Circuits Society and the Japan Society of Applied Physics in cooperation with the Institute of Electronics, Information, and Communications Engineers and the IEEE Electron Devices Society. The Symposium on VLSI Circuits is jointly organized and co-located with the Symposium on VLSI Technology and thus provides excellent opportunities for interactions among integrated circuit and technology experts on topics of mutual interest.

The Symposium on VLSI Circuits received 299 submissions. The program committees selected 108 articles for presentation with subjects including digital circuits, processors, SoCs, machine learning accelerators, memories, biomedical circuits, sensors and displays, power conversion circuits, analog amplifiers and filters, wireless and wireline communications, data converters, and frequency generation and clock circuits. This issue of the journal includes 25 outstanding articles selected as highlights of the work presented at the 2019 Symposium. The journal articles describe the work introduced at the Symposium with greater detail than provided by corresponding articles in the Symposium digest. The articles were subject to the standard journal review process. We enjoyed working with the authors on these articles, and we certainly hope that the technical details presented in these articles will be interesting and useful to journal readers. The following paragraphs give an overview of the article content of this Special Issue.

The first article demonstrates a temperature-stabilized 11-bit resolution 2-D mechanical stress sensor by the Technical University of Munich and Texas Instruments.

In the second article, researchers of the Pohang University of Science and Technology demonstrate Glucose-Monitoring Smart Contact Lens IC by using a dual-mode transmitter for wireless-powered backscattering and RF-radiated transmission.

The third article by the University of Leuven presents an innovative SoC chip for near-microphone keyword spotting and speaker verification, consuming only 18 $\mu$W.

The fourth article by Yonsei University uses a convolutional neural network and a long short-term memory to recognize static and dynamic gestures, respectively. The underlying signals are produced by a time-domain radar that is efficiently sampled at 33 GS/s.

The next two articles propose novel image sensors. First, researchers of Samsung Electronics demonstrate a 640 $\times$ 480 indirect time-of-flight CMOS image sensor that has been designed with 4-tap 7-$\mu$m global-shutter pixel and fixed-pattern phase noise self-compensation scheme. Then, the sixth article presents a 640 $\times$ 640 fully dynamic CMOS image sensor for the always-on object recognition application by Yonsei University and Kumoh National Institute of Technology.

Then, three novel machine learning accelerators are presented. Researchers of the University of Wisconsin–Madison propose "Liquid Silicon," a nonvolatile fully programmable processing-in-memory processor. The chip is based on monolithically integrated ReRAM. Research teams of NVIDIA, Stanford University, Stanford, CA, USA, and MIT introduce scalable, multi-chip-module-based deep neural network accelerator with ground-reference signaling fabricated with 16-nm technologies, achieving 0.11 pJ/Op and 0.32–128 TOPS. Finally, researchers of the University of Michigan, the University of Washington, and Arizona State University demonstrate 7.3 M output nonzeros/J sparse matrix–matrix multiplication (SpMM) accelerator using memory reconfiguration.

The next article by Intel introduces a novel security solution with side-channel attack resistant AES-128 fabricated by 14-nm CMOS technologies with heterogeneous Sboxes, linear Masked MixColumns, and dual-rail key addition, realizing 839 Mb/s throughput.

TSMC presents a novel dual-chiplet chip-on-wafer-on-substrate solution by using the latest 7-nm technologies. A 4-GHz-operation ARM-core-based CoWoS chiplet design for high-performance computing is demonstrated.

The next four articles describe power management solutions. The National University of Singapore presents an integrated power management unit and a microcontroller for wide power range adaptation down to nW. Researchers of

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Intel Labs introduce variation-adaptive computational digital LDO for achieving fast transient response. The University of Texas at Dallas demonstrates a GaN power converter which realizes 48/1V dc–dc voltage conversion by two-phase DSD architecture operating at 2 MHz. The final power article is by the University of Science and Technology of China, The Hong Kong University of Science and Technology, and the Chinese Academy of Sciences. It is a wireless battery charger that uses only four power transistors to handle rectification, regulation, and smooth transition between constant-current and constant-voltage charging modes. Peak efficiencies exceed 92% and the maximum charging current is 1.5 A.

Three data converter articles demonstrate improvements in energy efficiency and dynamic range. Comparators provide the key transition from continuous to discrete value in an analog-to-digital converter. Researchers at the University of Texas at Austin and the University of California, Davis, use a floating reservoir capacitor to power the inverter-based input stage of a comparator to operate with $7\times$ better energy efficiency than the classical Strong-Arm latch. The next data converter article by the Delft University of Technology and NXP Semiconductors combines an asynchronous SAR ADC and a continuous-time delta-sigma modulator to create a continuous-time zoom ADC with relaxed requirements for the reference and input buffers, while achieving $>$108-dB dynamic range. In a article from the University of Texas at Austin, the inter-stage gain error is shaped out-of-band to improve in-band SNDR in a low OSR pipelined ADC, and the technique can be applied independently of the type of residue amplifier.

The next two articles represent advancements in frequency generation. A 7-nm FinFET CMOS PLL is described by TSMC, where a track-and-hold charge pump and automatic loop gain control overcome the process node's high gate resistance and middle-end-of-line parasitics to achieve 388-$\text{fs}_{\text{rms}}$ jitter and $-80$-dBc reference spur. At upper mm-wave frequencies, wideband LO generation is extremely challenging. A article by the Hong Kong University of Science and Technology describes using injection-locked frequency multipliers with embedded frequency-tracking loops to generate frequencies spanning from 61 to 273.6 GHz.

Researchers from Auburn University and Intel demonstrate a direct RF-to-digital receiver for polar receivers. Here, an analog-to-digital converter and time-to-digital converter separately digitize the amplitude and phase of the RF signal, eliminating dedicated downconversion while generating an output directly at the baseband rate. It can process 1.94 Gb/s while consuming only 3.8 mW.

The final four articles advance the state of the art in wireline and optical transceivers. A 112-Gb/s PAM4 SERDES receiver in a 10-nm FinFET is described by Intel, which combines analog and digital equalization and a 64-way time-interleaved SAR ADC to achieve a bit error rate (BER) of 1e-6 over a channel with 35-dB loss at Nyquist. In a article by Xilinx, an electro-absorption modulator enables a 50Gb/s silicon photonic optical link in 16-nm FinFET. Researchers at the University of California, Berkeley, show a coherent optical receiver using a forwarded laser signal that improves the laser power budget by 6–8 dB. The full transceiver achieves BER $<$1e-9 at 10 Gb/s. The final article, by Kandou Bus, is an ultra-short reach transceiver that uses correlated nonreturn to zero signaling to transmit 5 bits over six wires while being robust to the common mode and crosstalk noise sources, achieving 20.83 Gb/s/wire.

This Special Issue required substantial efforts from the authors and the reviewers to meet the high standards of quality maintained by the journal. We would like to thank them for their efforts. We would also like to thank the Japan/Far East and North America/Europe Technical Program Committees of the Symposium on VLSI Circuits for coordinating and successfully running the conference, and for recommending articles for this Special Issue. We highly appreciate their work and the support of the Symposium Executive Committees. Finally, we would like to thank the Journal Editors-in-Chief, Dr. Jan Craninckx and Dr. Pavan Hanumolu, for their guidance, and the staff of the IEEE TRANSACTIONS and Journals Department for their invaluable assistance in publishing this issue.

In closing, we encourage readers to attend the 2020 Symposium on VLSI Circuits to be held from June 15 to 19, 2020, at the Hilton Hawaiian Village, Honolulu, Hawaii. Please visit the Symposium website, www.vlsisymposium.org, for more details.

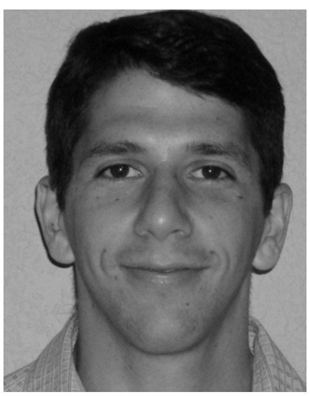
KEN TAKEUCHI, *Guest Editor*
Department of Electrical, Electronic,
and Communication Engineering
Chuo University
Tokyo 192-0393, Japan
e-mail: takeuchi@takeuchi-lab.org

BRIAN GINSBURG, *Guest Editor*
Texas Instruments
Dallas, TX 75266-0199 USA
e-mail: bginzz@ti.com

**Ken Takeuchi** received the B.S. and M.S. degrees in applied physics and the Ph.D. degree in electric engineering from The University of Tokyo, Tokyo, Japan, in 1991, 1993, and 2006, respectively, and the M.B.A. degree from Stanford University, Stanford, CA, USA, in 2003.

He was an Associate Professor with the Department of Electrical Engineering and Information Systems, Graduate School of Engineering, The University of Tokyo, from 2007 to 2012. In 2012, he joined Chuo University, Tokyo, where he is currently a Professor with the Department of Electrical, Electronic, and Communication Engineering, Faculty of Science and Engineering. He is also working on the database storage system for big-data applications, VLSI circuit design, signal processing, and devices such as the emerging non-volatile memories, 3-D-integrated SSDs, low-power 3-D-LSI circuits, and ultra-low-voltage SRAMs. In 1993, he joined Toshiba, Yokohama, Japan, where he has been leading Toshiba's NAND Flash Memory Circuit Design for 14 years. He designed six of the world's highest density NAND flash memory products, including 0.7-$\mu$m 16-Mbit, 0.4-$\mu$m 64-Mbit, 0.25-$\mu$m 256-Mbit, 0.16-$\mu$m 1-Gbit, 0.13-$\mu$m 2-Gbit, and 56-nm 8-Gbit NAND flash memories. He holds 228 patents worldwide, including 124 U.S. patents. He has authored numerous technical articles.

Dr. Takeuchi served as the Program Committee Member for the International Solid-State Circuits Conference (ISSCC), the Custom Integrated Circuits Conference (CICC), the Asian Solid-State Circuits Conference (A-SSCC), the International Memory Workshop (IMW), the International Conference on Solid State Devices and Materials (SSDM), and the Non-Volatile Memory Technology Symposium (NVMTS). With his invention, multipage cell architecture, presented at the Symposium on VLSI Circuits in 1997, he successfully commercialized the world's first multi-level cell NAND flash memory in 2001. He has served as a Tutorial Speaker at ISSCC 2008, a Forum Speaker at ISSCC 2015, an SSD Forum Organizer at ISSCC 2009, a 3-D-LSI Forum Organizer at ISSCC 2010, an Ultra-Low Voltage LSI Forum Organizer at ISSCC 2011, and a Robust VLSI System Forum Organizer at ISSCC 2012. He received the Takuo Sugano Award for Outstanding Paper at ISSCC 2007. He served as the Program Chair/Co-Chair for the Symposium on VLSI Circuits in 2018 and 2019. He is currently serving as the Symposium Co-Chair for the Symposium on VLSI Circuits.



**Brian P. Ginsburg** (Senior Member, IEEE) received the B.S. and M.Eng. degrees in electrical engineering and computer science and the Ph.D. degree from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2003 and 2007, respectively.

He joined Texas Instruments, Dallas, TX, USA, in 2007, where he has been working with Wireless Business Unit, Kilby Laboratories, and the embedded processing organization. He is currently a Distinguished Member of Technical Staff and the Systems Manager with the Radar Business Unit, Texas Instruments.

Dr. Ginsburg was a member of the ISSCC Technical Program Committees from 2016 to 2019. He was named a Siebel Scholar in 2003, received the NDSEG Fellowship in 2004, and was a winner of the 2006 ISLPED International Low Power Design Contest. He is currently the Program Chair of the IEEE Symposium on VLSI Circuits Technical Program Committee.