A Single-Pin Antenna Interface RF Front End Using a Single-MOS DCO-PA and a Push–Pull LNA

Kai Xu, *Student Member, IEEE*, Jun Yin, *Member, IEEE*, Pui-In Mak, *Fellow, IEEE*, Robert Bogdan Staszewski, *Fellow, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*— We propose a simple power-efficient sub-1-V fully integrated RF front end (RFE) for 2.4-GHz transceivers. It introduces the following innovations. First, a function-reuse single-MOS digitally controlled oscillator power amplifier (DCO-PA) with full supply utilization improves antenna-to-DCO isolation for better resilience to jammers. Second, a noninverting transmitter (TX) matching transformer with a zero-shifting capacitor suppresses the second-harmonic emission of the DCO-PA and allows a single-pin antenna interface for both TX and receiver (RX) modes eliminating the transmit/receive (T/R) switches in the signal path. Third, a push–pull low-noise amplifier (LNA) reuses the TX matching transformer for passive gain boosting that reduces power consumption. Fabricated in 65-nm CMOS, the RFE occupies merely 0.17 mm^2. Through the functional merge of the oscillator and PA, it can transmit 0 dBm at RF, featuring 10.2% power efficiency when delivering the RF power as low as −10 dBm at a 0.3-V supply. Under a 0.5-V supply, the LNA shows 11-dB gain and 6.8-dB noise figure (NF) while consuming 174 μW.**

***Index Terms*— Digitally controlled oscillator (DCO), function reuse, harmonic suppression, low-noise amplifier (LNA), power amplifier (PA), RF front end (RFE), transformer, transmit/receive (T/R) switch.**

I. Introduction

ULTRA-LOW-POWER (ULP) radios play a crucial role in the expansion of Internet-of-Things (IoT) connectivity where wireless sensors gather and exchange a massive amount of data. In battery-operated low-data-rate, short-range sensor applications, such as temperature, humidity and pressure monitoring, as well as health tracking, the major bottleneck lies in the battery life. Bluetooth low energy (BLE) is the key standard, which has gained popularity [1]–[7] not only due to its support for a lower duty-cycle operation but also for various low-power states allowing to reduce current consumption in line with the usage profile and application scenarios. Indeed,

Manuscript received August 4, 2019; revised December 17, 2019, March 9, 2020, and April 13, 2020; accepted April 27, 2020. Date of publication May 19, 2020; date of current version July 23, 2020. This article was approved by Associate Editor Waleed Khalil. This work was supported in part by the Science Foundation Ireland under Grant 14/RP/I2921 and in part by the Science and Technology Development Fund, Macau SAR, under Grant 0044/2019/A1 and Grant SKL Fund. *(Corresponding author: Jun Yin.)*

Kai Xu and Robert Bogdan Staszewski are with the School of Electrical and Electronic Engineering, University College Dublin, Dublin D04 V1W8, Ireland (e-mail: kai.xu@ucd.ie).

Jun Yin, Pui-In Mak, and R.P. Martins are with the State-Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macau (e-mail: junyin@um.edu.mo; pimak@um.edu.mo).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2020.2991520

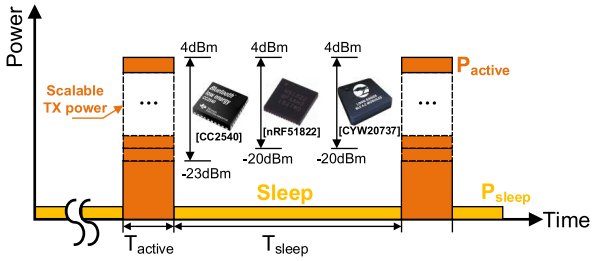

Fig. 1. BLE SoCs with programmable RF power.

the BLE transmitters (TXs) typically support programmable RF output power from −20 to +4 dBm, as shown in Fig. 1 for a few commercial chipsets. The TX comprises an RF power amplifier (PA) and a frequency synthesizer as major components and dominates the total power consumption of the RF transceiver. Hence, there are intensive ongoing efforts on improving its efficiency, especially at deep power back-off levels.

Open-loop modulation has recently gained popularity in ULP TXs due to its energy-saving feature by shutting down the all-digital phase locked loop (ADPLL) loop after quickly acquiring the channel center frequency [1], [6], [8]–[10]. Further improvements in substantially lowering of the DCO flicker noise help to bring the carrier frequency drift to well within the IoT specifications [6], [10]. Under the open-loop scenario, the conventional TX architectures can be simplified as a convenient arrangement of a separate oscillator (e.g., voltage controlled oscillator (VCO) or DCO) and a PA [see Fig. 2(a)], which are the two most power-hungry blocks.[1] Generally, the oscillator runs at 2× PA carrier frequency to mitigate the potential injection pulling attributed to the parasitically coupled (but frequency modulated via the amplitude modulation (AM) component) aggressor from the PA [11]. Consequently, this necessitates divider and buffer stages in cascade to drive the PA in which the consumed power into the PA driving does not scale with the back-off of the TX output power. At the deep power back-off, where the power spent into the PA driving is comparable to the targeted RF power, the total TX efficiency will be heavily compromised. Even with state-of-the-art highly

[1]The power-saving benefits of the open-loop modulation can be extended for quasi-open-loop modulation. An ADPLL for BLE in [10] features a mere 1-kHz loop bandwidth so that almost all of its digital circuitry can operate in subthreshold, resulting in the DCO consuming 70% of its 0.9-mW power budget.

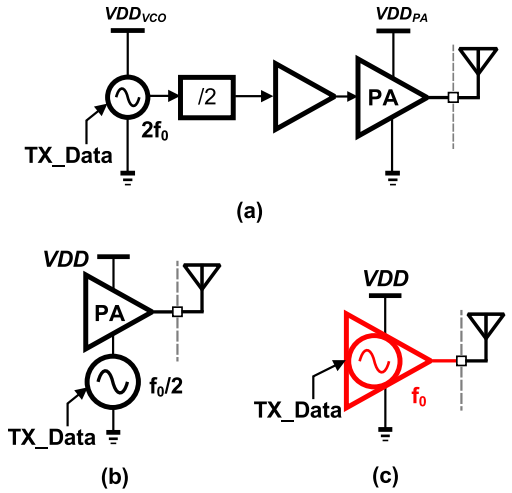

Fig. 2. ULP TXs. (a) Traditional, i.e., separate DCO and PA. (b) Current-reuse PA-DCO stack. (c) Function-reuse DCO-PA.

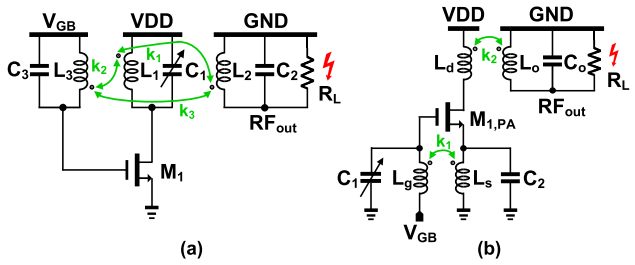

Fig. 3. Function-reuse DCO-PA. (a) Class-F DCO-PA based on six-port transformer in [14]. (b) Proposed DCO-PA.

efficient solutions [6], [12], the total TX efficiency is restricted to 8% at deep power back-off (−10 dBm) even under an open-loop operation. The latest ring-oscillator-based 4× frequency edge combiner [7] remarkably reduces the power consumed to drive the PA while introducing significant compromise on its phase noise (PN). Separate optimization of the PA, oscillator, and other driving stages is not desirable in the low-power regime.

A current-reuse PA-VCO stack [13] aims to optimize the VCO and PA as an indivisible entity [see Fig. 2(b)]. However, it is incompatible with the ultra-low-voltage (ULV) operation and has a constrained output power due to the reduced voltage headroom. There is an inherent tradeoff between the oscillator's PN and total PA efficiency in terms of the supply division between these two. Instead of the current-reuse TX topology, the function-reuse DCO-PA first proposed in [14] seems more promising through assimilating the power consumption of the DCO into the DCO-PA with full V_{DD} utilization and breaking the aforementioned PN and efficiency tradeoff with purely passive (transformer) optimization [see Fig. 2(c)]. Nevertheless, the six-port transformer that merges the oscillator resonance tank and the PA matching network (MN) would inevitably incur unfavorable mutual coupling between these two, as shown by a coupling factor k_3 in Fig. 3(a). Consequently, this class-F DCO-PA is extremely vulnerable to jammers appearing at the antenna. In addition, the second impedance peak at the third harmonic for higher efficiency of this class-F DCO-PA could inevitably require off-chip filtering of HD_3.

To avoid the mutual coupling resulting from the forced coexistence of oscillation tank and impedance MN in the shared six-port (i.e., three-winding) transformer of Fig. 3(a), a single-MOS DCO-PA based on source-to-gate (S-to-G) transformer feedback oscillation is proposed in this article. It is shown in Fig. 3(b). The output matching transformer is simultaneously utilized as a single-pin antenna interface (T/R switch) for both TX and receiver (RX) modes while offering passive gain boosting to the push–pull low-noise amplifier (LNA), hence saving extra power.

The rest of this article is organized as follows. Section II introduces the new single-MOS DCO-PA topology for ULP TX accompanied by the zero-shifting capacitor across the MN transformer windings to suppress the second harmonic. The single-pin antenna interface and the passive gain-boosting push–pull LNA are investigated in Section III. Section IV reveals the top-level implementation of the prototype with experimental results. Section V wraps up the article with conclusions.

II. Single-MOS DCO-PA for ULP TX

The concept of implementing the oscillator and PA using the same transistor and operating at the same frequency was initially introduced in [15], where the tuned power oscillator can be as energy efficient as the class-E PA. However, the scheme requires complicated phase correction to guarantee the −196° feedback loop phase shift. A DCO-PA-LNA-TX/RX-switch co-designed block proposed in [16] delivers TX power by connecting the antenna to the sources of the cross-coupled transistors pair in the DCO, which suffers from limited output power and injection pulling. Analogously, the impediment to the practical application of the class-F DCO-PA in [14] arises from the insufficient isolation between the antenna and the oscillator, which would make the carrier frequency rather sensitive to the interferers, as previously mentioned in Section I. All the abovementioned techniques are at the expense of introducing additional tradeoffs between system complexity, reliability, and efficiency.

A. S-to-G Transformer-Feedback DCO-PA

The basic idea behind the DCO-PA architecture is to make the PA self-driven for the additional purpose of generating self-oscillation. Consequently, it can eliminate the need for a separate PA driving circuitry necessarily, including an oscillator, divider, and buffer, whose power consumption cannot easily scale when backing off the optimal PA power levels. This can benefit the overall TX efficiency, especially in the low-power regime. To meet Barkhasusen's criteria for oscillation, a third coil L_3 is added to produce another 180° loop phase shift through the inverting coupling between L_3 and L_1 in [14] enabling the drain-to-gate (D-to-G) transformer feedback oscillation [see Fig. 3(a)]. The inescapable coupling between L_3 and L_2 characterized by k_3 will expose the resonance tank to the antenna leading to vulnerability to jammers or interferers. The D-to-G feedback oscillation is replaced

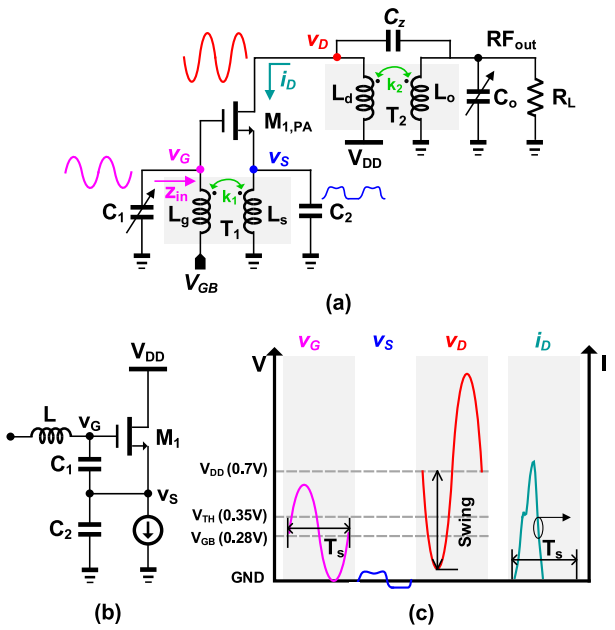

Fig. 4. (a) Proposed S-to-G transformer feedback DCO-PA. (b) Analogy to a Colpitts oscillator. (c) Illustration of the DCO-PA's node voltage and current waveforms.

here by an S-to-G feedback to enhance the antenna-to-DCO isolation, breaking the tradeoff between system efficiency and jammer resilience performance [17].

The feedback mechanism of the S-to-G feedback oscillator is analogous to that in a Colpitts oscillator [18]. The capacitive divider in the Colpitts oscillator provides the required positive feedback, while the feedback in the proposed oscillator is given by the S-to-G feedback transformer, as shown in Fig. 4(b). In the Colpitts case, a scaling factor n_{Colp} can be expressed as

$$n_{\text{Colp}} = \frac{v_G}{v_S} = \frac{C_1 + C_2}{C_1}. \tag{1}$$

As for the S-to-G transformer feedback case being distinct from the DCO-only implementation in [18], a rather large device is commonly used in the PA in order to lower its power loss. Considering the device capacitance C_{gs}, the scaling factor in the proposed DCO-PA is then described as

$$n_{\text{DCOPA}} = \frac{v_G}{v_S} = \frac{k_1}{n_1} - C_{\text{gs}} L_s \omega^2 \left(\frac{k_1}{n_1} - 1 \right) \tag{2}$$

where $n_1 = (L_s/L_g)^{1/2}$ is the turns ratio of transformer T_1 and k_1 is the magnetic coupling factor. Therefore, with $|Z_s|$ representing the tank impedance seen at source, the loop gain can be estimated

$$A_{\text{loop}} \approx \frac{g_m |Z_s|}{1 + g_m |Z_s|} n_{\text{DCOPA}} \tag{3}$$

indicating that a smaller turns ratio n_1 (a larger L_g/L_s) in the S-to-G transformer-feedback oscillator is preferred to enlarge n_{DCOPA}, increase the A_{loop}, boost v_g swing, and lower the PN. This is verified via simulation results shown in Fig. 5(a), where L_g and L_s are the self-inductances of the primary and secondary coils of T_1, respectively. In the simulations, L_g is kept constant with an assumed value of 2 nH, while $k_1 = 1$ is chosen for simplicity. Neglecting the series resistance inherent with the transformer coils, the input impedance z_{in} at the gate of $M_{1,\text{PA}}$ without C_1 [see Fig. 4(a)] is given by the long formula (4), as shown at the bottom of this page, where $M = k_1 (L_g L_s)^{1/2}$ represents the mutual inductance between the two coils. The imaginary part of z_{in} will resonate with C_1 at the targeted frequency and the negative real impedance part happens to be beneficial in compensating for the LC tank losses. Since the second resonance of T_1 is designed at $3\times$ of the oscillating frequency to suppress the third-harmonic current, as will be detailed later, the effect from C_2 is relatively small and is further ignored to obtain a simplified expression of z_{in}

$$z_{\text{in}} \approx \frac{C_{\text{gs}}(L_g L_s - M^2)s^3 + g_m(L_g L_s - M^2)s^2 + L_g s}{C_{\text{gs}}(L_g + L_s - 2M)s^2 + g_m(L_s - M)s + 1}. \tag{5}$$

It is, therefore, straightforward to obtain the real part of the impedance z_{in} after some simple manipulations

$$z_{\text{in,real}} \approx \frac{g_m L_g L_s \omega^2 k_1^2 \left(1 - \frac{1}{k_1}\frac{1}{n_1}\right)\left[1 - C_{\text{gs}} L_s \omega^2 \left(\frac{1}{k_1} - k_1\right)\frac{1}{n_1}\right]}{\left(1 - C_{\text{gs}} L_s \omega^2 \left(\frac{1}{n_1^2} - 2\frac{k_1}{n_1} + 1\right)\right)^2 + g_m^2 L_s^2 \omega^2 \left(1 - \frac{k_1}{n_1}\right)^2}. \tag{6}$$

Obviously, $0 < k_1 < 1$, so, $1/k_1 - k_1 > 0$. Furthermore, C_{gs} is generally on the order of few hundreds of femtofarad with L_s at the level of nanohenry. Hence, we can presume that the square-bracketed factor in the numerator of (6) is positive, i.e., $\left[1 - C_{\text{gs}} L_s \omega^2 (1/k_1 - k_1) 1/n_1\right] > 0$. In order to provide the negative real impedance to compensate for the losses of the LC resonant tank, $1/n_1 > 1 \rightarrow L_g > L_s$ is favored, which also coincides with the conditions for lower PN. The simulated real part of the input impedance z_{in} across L_g/L_s is plotted in Fig. 5(b). From (2) and (6), it is apparent that the presence of C_{gs} would have a negative effect of decreasing n_{DCOPA} and $|z_{\text{in,real}}|$. Moreover, when the influence of C_{gs} is further disregarded, z_{in} proves out to be exactly the same as the expression given in [18]. The PN equation for the generated waveform can be straightforwardly obtained in [19, eq. (39)].

The PA is realized by transferring the power of drain oscillation waveform to the antenna with an appropriate impedance transformation ratio provided by transformer T_2 in Fig. 4(a). The overall PA efficiency is composed of two parts

$$\eta_{\text{PA}} = \eta_{\text{PA,T}} \cdot \eta_{\text{MN}} \tag{7}$$

where $\eta_{\text{PA,T}}$ indicates the PA efficiency considering only the loss from the lone power transistor. Correspondingly, the efficiency of the MN is labeled as η_{MN}. An intuitive way to lower the transistor's dissipation, thus improving $\eta_{\text{PA,T}}$, is to reduce the fraction of a cycle over which the drain voltage and

$$z_{\text{in}} = \frac{(L_g L_s - M^2)(C_{\text{gs}} + C_2)s^3 + g_m(L_g L_s - M^2)s^2 + L_g s}{(L_g L_s - M^2)C_{\text{gs}} C_2 s^4 + (C_{\text{gs}} L_g + (C_{\text{gs}} + C_2)L_s - 2MC_{\text{gs}})s^2 + g_m(L_s - M)s + 1}. \tag{4}$$

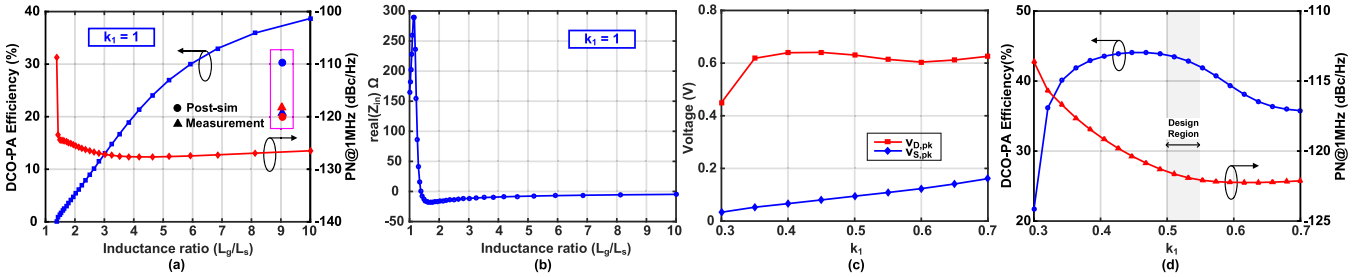

Fig. 5. Simulation results of the proposed DCO-PA. (a) PN, efficiency, and (b) input impedance versus inductance ratio. (c) Voltage swing. (d) PN, efficiency versus coupling factor.

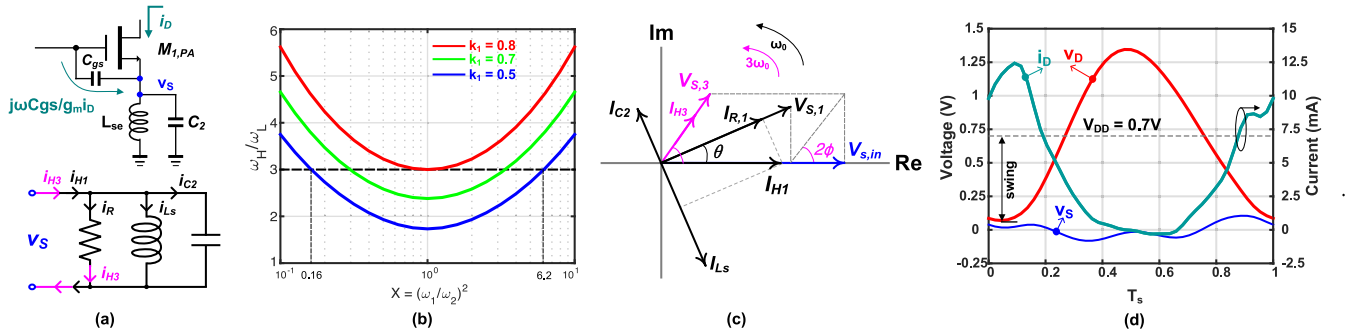

Fig. 6. LC tank at the source node. (a) Equivalent model and current distribution. (b) Ratio of the tank resonant frequencies versus X-factor for different values of k_1. (c) Phasor diagram of harmonic currents and voltages. (d) Time-domain voltage and current waveforms.

drain current waveforms of the single-MOS $M_{1,\mathrm{PA}}$ in Fig. 4(a) are simultaneously nonzero through properly arranging the gate bias V_{GB}. The mathematical expression for $\eta_{\mathrm{PA,T}}$ as a function of the total conduction angle 2ϕ described in [20] is retrospected with first assuming a cosine drain current

$$i_D = I_{\mathrm{DC}} + I_{\mathrm{RF}} \cos \omega_0 t, \quad i_D > 0 \tag{8}$$

and then, $\phi = \omega_0 t$ can be solved by setting the current i_D to zero

$$\phi = \cos^{-1}\left(-\frac{I_{\mathrm{DC}}}{I_{\mathrm{RF}}}\right). \tag{9}$$

The average drain current $\overline{I_{\mathrm{DC}}}$ from the supply is evaluated by integrating i_D over the conduction interval 2ϕ and substituting with the expression for I_{DC} in (9), which yields

$$\overline{I_{\mathrm{DC}}} = \frac{I_{\mathrm{RF}}}{\pi}(\sin\phi - \phi\cos\phi). \tag{10}$$

To gain insight into the power delivered to the load R_d seen at the drain, as well as into the PA efficiency, the fundamental coefficient I_{h1} for the fundamental current i_{H1} in the Fourier expansion of i_D is determined by the integral as follows:

$$\begin{aligned} I_{h1} &= \frac{2}{2\pi}\int_0^{2\pi} i_D(\phi)\cos\phi \, \mathrm{d}\phi \\ &= \frac{I_{\mathrm{RF}}}{2\pi}(2\phi - \sin 2\phi). \end{aligned} \tag{11}$$

In a similar way, we can get the coefficient I_{h3} for the third-harmonic current i_{H3}

$$I_{h3} = \frac{I_{\mathrm{RF}}}{12\pi}(2\sin 2\phi - \sin 4\phi). \tag{12}$$

The L_s inductive degeneration would have a detrimental effect on $\eta_{\mathrm{PA,T}}$ since it consumes the output swing of $M_{1,\mathrm{PA}}$ in the presence of $v_S(t)$ voltage across its source node [21]. Moreover, C_2 is added in parallel with L_s to produce a high impedance at $3\omega_0$, thus obstructing the third-harmonic current. To understand this better and to obtain a mathematical expression for $v_S(t)$, the L_sC_2 tank at source node is redrawn in Fig. 6 with the corresponding phasor diagrams representing the voltage and current waveforms at different harmonic frequencies. It is noteworthy that the two possible modes of oscillation in our two-port transformer-based resonator happen at two frequencies, the same to that in the one-port case [22], which under a high-Q assumption can be expressed as

$$\omega_{H,L}^2 = \frac{1 + X \pm \sqrt{(1-X)^2 + 4k_1^2 X}}{2\left(1-k_1^2\right)}\omega_2^2 \tag{13}$$

where $\omega_1^2 = \left(L_gC_1\right)^{-1}$, $\omega_2^2 = (L_sC_2)^{-1}$, and $X = (\omega_1/\omega_2)^2$. To find the X-factor that can secure the second impedance peak at $3\omega_0$, the frequency ratio between the high and low oscillation modes ω_H/ω_L as a function of X-factor is plotted in Fig. 6(b). The X-factor reaches the desired value of 3 at two points for the coupling factor $k_1 < 0.8$. A moderate k_1 with small $X = L_sC_2/L_gC_1$ is expected to mitigate the efficiency impairment caused by L_s. It thus offers a good estimation of the high resonant frequency in (13) to be $\omega_H \approx \omega_2/(1-k_1^2)^{1/2} = 1/\left(\left(1-k_1^2\right)L_sC_2\right)^{1/2}$ revealing that the effective inductance at the source is $L_{\mathrm{se}} \approx \left(1-k_1^2\right)L_s$. For a certain amount of drain current i_D, there would be a portion of $i_{C_{\mathrm{gs}}} = i_D \cdot j\omega C_{\mathrm{gs}}/g_m$ flowing through the parasitic path due to C_{gs} [23]. To maintain the same $v_S(t)$ at the source, this is equivalent to adding another LC tank in parallel to the L_sC_2 tank with a scaling $j\omega C_{\mathrm{gs}}/g_m$ such that the total admittance

seeing into the tank is

$$Y_{t,1} = \left(1 + \frac{j\omega C_{\rm gs}}{g_m}\right)\left(\frac{1}{j\omega L_{\rm se}} + j\omega C_2 + \frac{1}{R_p}\right) \quad (14)$$

where $R_p \approx \omega L_s Q_{L_s}$ dominates the tank losses.

At fundamental frequency ω_0, the fundamental current $i_{H1} = I_{h1}\cos\omega_0 t$ with an initial phase of zero would split into three parts, i_{R_1}, i_{Ls}, and i_{C2}, flowing through the equivalent RLC components in Fig. 6(a), respectively. Thereinto, $v_{S,1}$ is marked out to be the reference as it is common to all the three branches. Correspondingly, the current signal i_{R_1} is in-phase to the reference $v_{S,1}$, while the signals i_{L_s} and i_{C_2} are $\pi/2$ behind and $\pi/2$ ahead of $v_{S,1}$, which are all sketched as the black arrow lines in Fig. 6(c). In view that there is a phase difference of π between i_{L_s} and i_{C_2}, the fundamental current i_{H1}, which is equivalent to the phasor addition of these three branch currents, can be obtained by applying the parallelogram law and drawing the diagonal line between i_{L_s}–i_{C_2} and i_{R_1}. Due to the fact that the L_sC_2 tank resonates at $3\omega_0$, the inductive susceptance would dominate the tank at ω_0 ($1/j\omega_0 L_{\rm se} \gg j\omega_0 C_2$) causing the lagging effect of i_{H1} with respect to $v_{S,1}$. The total tank admittance $Y_{t,1}$ at ω_0 can be simplified as

$$Y_{t,1} \approx \left(\frac{1}{g_m L_{\rm se}/C_{\rm gs}} + \frac{1}{R_p}\right) + \frac{1}{j\omega_0 L_{\rm se}} + \frac{j\omega_0}{g_m R_p/C_{\rm gs}}. \quad (15)$$

Under the circumstance $g_m/C_{\rm gs} \approx \omega_T \gg \omega_0$ and assuming $\omega_T = \alpha\omega_0$, $Y_{t,1}$ can be further simplified

$$Y_{t,1} \approx \frac{1}{\omega_0 L_s}\left(\frac{1}{\alpha\left(1-k_1^2\right)} + \frac{1}{Q_{\rm Ls}}\right) + \frac{1}{j\omega_0 L_{\rm se}}. \quad (16)$$

Consequently, the equivalent parallel resistance R of the tank at ω_0 in Fig. 6(a) can be obtained as $R_1 = \omega_0\ L_s \cdot \alpha\left(1-k_1^2\right)Q_{\rm Ls}/\left(\alpha\left(1-k_1^2\right) + Q_{\rm Ls}\right)$, which is crucial for determining the swing at the source node. The angle θ between the resultant signal i_{H1} and the reference $v_{S,1}$ is given by

$$\theta = \tan^{-1}\frac{B_{\rm Ls} - B_{C2}}{G} = \tan^{-1}\frac{1/\omega_0 L_{\rm se} - \omega_0 C_2}{1/R_1} \quad (17)$$

where G is the relevant conductance of R_1. $B_{\rm Ls}$ and B_{C2} stand for the corresponding susceptances.

At third-harmonic frequency $3\omega_0$ where the resonance happens, the inductance and capacitance would cancel out each other leaving the tank purely resistive with $R_3 \approx 3\omega_0\ L_s Q_{\rm Ls}$, which is shown in Fig. 6(a) as the purple current i_{H3} circulating through the R path only. The corresponding voltage signal $v_{S,3}$ is identically in-phase with i_{H3}, with zero initial phase shown in Fig. 6(c). In addition to the high-Q tank at the output filtering the third harmonic, the fairly high-impedance peak $R_3 \approx 3\omega_0\ L_s Q_{\rm Ls}$ at the source would lift up the knee voltage, thus limiting the swing of third-harmonic component at the output.

It is then straightforward to indicate that the signal $v_{S,1} = V_{s,1}\cos(\omega_0\ t + \theta)$ has an amplitude $V_{s,1} = I_{h1}\cos\theta \cdot R_1$ with $0 < \theta < \pi/2$ due to $B_{\rm Ls} > B_{C2}$. Likewise, the third-harmonic signal can be expressed as $v_{S,3}(t) = V_{s,3}\cos(3\omega_0\ t)$ with amplitude $V_{s,3} = I_{h3} \cdot R_3$. So far, we have not involved a discussion on second-harmonic nonlinearity, but it will be pointed out in Section II-B that the $\rm HD_2$ component at the output MN is suppressed through the introduced zero-shifting capacitor C_z. Without considering even higher order harmonics, the source voltage is the superposition of its fundamental and third harmonics, $v_S(t) = V_{s,1}\cos(\omega_0 t + \theta) + V_{s,3}\cos(3\omega_0 t)$. When the drain current $i_{H1}(t)$ attains its peak, the source voltage in the direction of $i_{H1}(t)$ is of interest, which can be written as $V_{\rm s,in} = V_{s,1}\cos\theta + V_{s,3}$.

Assuming that $M_{1,\rm PA}$ behaves all the time as a current source, the output voltage will reach its maximum swing $V_d = |-I_{h1} \cdot R_d|$. The negative sign means that the current flowing into the load is inverse to the drain current. Considering the effect of $V_{\rm s,in}$, the maximum swing

$$V_d = I_{h1} \cdot R_d \approx V_{\rm DD} - V_{\rm s,in}. \quad (19)$$

From (10) and (11), it is easy to solve for the average dc current $\overline{I_{\rm DC}}$ in terms of I_{h1}

$$\overline{I_{\rm DC}} = 2 \cdot \frac{\sin\phi - \phi\cos\phi}{2\phi - \sin 2\phi} \cdot I_{h1}. \quad (20)$$

Substituting the expression for $V_{\rm DD}$ from (19), the DC power consumption can be derived as

$$P_{\rm DC} = 2 \cdot \frac{\sin\phi - \phi\cos\phi}{2\phi - \sin 2\phi} \cdot I_{h1}^2 \cdot \left(\cos^2\theta R_1 + \beta R_3 + R_d\right) \quad (21)$$

where β is defined as the ratio between I_{h3} and I_{h1} in (12) and (11). Together with the RF power delivered to the load

$$P_{\rm RF} = \frac{1}{2} \cdot I_{h1}^2 \cdot R_d \quad (22)$$

the transistor efficiency $\eta_{\rm PA,T}$ can be readily calculated from the long formula (18), as shown at the bottom of this page, in which the third factor stands for the efficiency drop in the presence of the LC tank at the source and the MOS nonlinearity. When $L_s \to 0$, the third factor would vanish to one, leaving $\eta_{\rm PA,T}$ to be exactly the same as that of the class-C PA.

Intuitively, the denominator of the third fraction in (18) defines the equivalent resistive loss due to L_s in the "direction" of the drain load R_d, although the "direction" comes from the phase difference between the aforementioned two signals i_R and i_{H3} to i_{H1}. Under numerical boundaries, when $\theta \to 0$, the "anti-phase" resistive loss reaches its maximum, raising up the knee voltage and bringing down the efficiency. At the other extreme of $\theta \to \pi/2$, the L_s-induced loss reaches its minimum. The anticipated load resistance R_p is realized

$$\eta_{PA,T} = \frac{1}{4} \cdot \frac{2\phi - \sin 2\phi}{\sin\phi - \phi\cos\phi} \cdot \frac{1}{1 + \left(\frac{1}{1 + \frac{Q_{Ls}}{\alpha\left(1-k_1^2\right)}}\cos^2\theta + \frac{1}{2}\frac{2\sin 2\phi - \sin 4\phi}{2\phi - \sin 2\phi}\right)\frac{\omega_0 L_s Q_{Ls}}{R_d}} \quad (18)$$

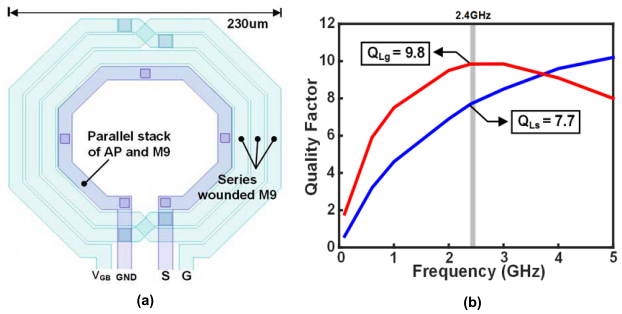

Fig. 7. S-to-G feedback transformer. (a) Layout pattern. (b) L_g and L_s Q-factors.

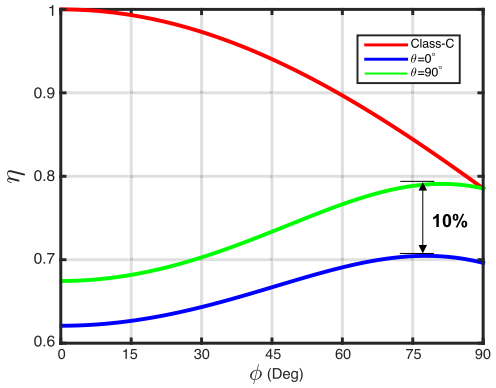

Fig. 8. $\eta_{\mathrm{PA,T}}$ given in (18) by substituting the design parameters.

through the impedance transformation provided by transformer T_2 upon the amount of RF output power targeted. Assuming that a quality factor $Q_L = 10$ applies for all the windings in T_1 and T_2 in the DCO-PA circuit using a simple, but parameterized transformer model, the maximum swing we can reach under the 0.7-V supply is $V_d \approx 0.6$ V, and thus, $R_d \approx 1/2V_d^2/P_{\mathrm{RF}} = 180\ \Omega$, indicating that the step-down transformer T_2 should have a turns ratio $n_2 \approx (R_L/R_d)^{1/2} \approx 1/2$ with $R_L = 50\ \Omega$ representing the antenna.

Furthermore, to assure the feasibility of T_1 physical implementation, $L_s \approx 0.2$ nH is chosen in this design to minimize its negative impact. The exact amount of inductance seen at $M_{1,\mathrm{PA}}$ source would also be affected by the coupling factor k_1 between the L_g and L_s coils. Under a relatively large $L_g/L_s = 10$, the effects of different values of k_1 on the output swing v_D, fundamental voltage peak at source V_s, PN $\mathcal{L}(\Delta\omega)$, and DCO-PA efficiency η_{PA} are shown in Fig. 5(c)–(d). Conspicuously, there is a comparatively great compromise between the total efficiency of the proposed single-MOS DCO-PA and its PN at a moderate coupling factor $k_1 \approx 0.5$. The corresponding time-domain node voltages and current waveforms are shown in Fig. 6(d). As previously discussed, $C_2 \approx 2.4$ pF is adopted to induce the expected impedance peak at $3\omega_0$. The physical layout pattern of T_1 with a coupling factor $k_1 = 0.52$ is revealed in Fig. 7(a). It consists of a series-wound three turns on top metal (M9) as L_g and a parallel stack of two innermost turns of AP and M9 as L_s. By virtue of simply overlaying the AP layer, this contributes to diminishing the L_s inductance by 20 pH while increasing its quality factor Q_{Ls} by 1. The resultant inductances, $L_g \approx 2$ nH and $L_s \approx 220$ pH, are confirmed by electromagnetic (EM) simulations with their quality factors plotted in Fig. 7(b). In addition, T_1 exhibits a self-resonant frequency (SRF) of roughly 12 GHz. By substituting the design parameters into (18), $\eta_{\mathrm{PA,T}}$ is compared in Fig. 8 to the efficiency of an ideal class-C suggesting the influence of source degeneration with near 30% efficiency drop at low conduction angles. It also reveals a near 10% efficiency difference between the two numerical boundaries of θ. In addition, the total conduction angle 2ϕ strongly depends on the gate bias V_{GB} and there is generally a trade-off between the width of RF current pulse and efficiency. At $2\phi \approx 150°$, $\eta_{\mathrm{PA,T}}$ in (18) reaches its peak, as shown in Fig. 8.

Remarkably, in contrast with the conventional PAs which might exhibit stability issues, there is no such concern here as the gate and source nodes of the single-MOS $M_{1,\mathrm{PA}}$ in this DCO-PA are actually resonating as intended.

B. HD_2 Suppression Through Zero-Shifting Capacitor C_z

Transfer function behavior of a general transformer-based MN for a PA has been discussed comprehensively in [24], including the effects of inter-winding capacitance C_{tot}. Similarly, by means of neglecting the frequency response below the first pole $\omega_{p1} = r_d/L_d$ in T_2, established mainly by L_d and its equivalent series resistance r_d [25], the voltage gain transfer function $G(s)$ can be simplified as a second-order system

$$G(s) \approx \frac{L_oC_{\mathrm{tot}}\left(1-k_2^2\right)s^2 + L_oC_{\mathrm{tot}}\omega\left(\frac{1}{Q_{L_d}} + \frac{1}{Q_{L_o}}\right)s + \frac{M_{T2}}{L_d}}{L_oC_o\left(1-k_2^2\right)s^2 + L_o\left[C_o\omega\left(\frac{1}{Q_{L_d}} + \frac{1}{Q_{L_o}}\right) + \frac{1-k_2^2}{R_L}\right]s + 1} \tag{23}$$

where $C_{\mathrm{tot}} = C_{\mathrm{int}} + C_z$, implying that the total effective inter-winding capacitance C_{tot} is composed of the intrinsic inter-winding capacitance C_{int} and the artificially added zero-shifting capacitor C_z across the primary and secondary coils of T_2. Although the MN together with C_z looks superficially similar as that in [24], the working principle and system response are essentially different, primarily due to the fact that the T_2 transformer in this implementation is in the non-inverting configuration (i.e., $M_{T2} > 0$). After the numerator's second-order polynomial is rearranged into a more standard form $N(s) = s^2 + 2\xi_n\omega_n s + \omega_n^2$, it is straightforward to derive the corner-frequency damping factor ξ_n and the corner frequency ω_n of $N(s)$

$$\xi_n = \frac{1}{2}\omega\left(\frac{1}{Q_{L_d}} + \frac{1}{Q_{L_o}}\right)\sqrt{\frac{L_oC_{\mathrm{tot}}}{n_2k_2\left(1-k_2^2\right)}} \tag{24}$$

$$\omega_n = \sqrt{\frac{k_2n_2}{L_oC_{\mathrm{tot}}\left(1-k_2^2\right)}} = \sqrt{\frac{k_2}{\sqrt{L_oL_d}C_{\mathrm{tot}}\left(1-k_2^2\right)}}. \tag{25}$$

In this form, the quadratic formula gives the zero locations as

$$s = -\xi_n\omega_n \pm \omega_n\sqrt{\xi_n^2 - 1}. \tag{26}$$

With $\xi_n \approx 0.05$ in this design falling into the interval $0 < \xi_n < 1$, we can expect that the numerator polynomial $N(s)$ will exhibit one complex-conjugate zero pair. Furthermore, when damping factor ξ_n satisfies $0 < \xi < 1/\sqrt{2}$,

the amplitude–frequency response of $N(s)$ unveils a valley (i.e., minimum value) at frequency $\omega_v = \omega_n\sqrt{1-2\xi^2}$ whose depth is bound up with its damping factor ξ. The amplitude of this valley is given by

$$|H(j\omega_v)| = \frac{1}{2\xi\sqrt{1-\xi^2}} \rightarrow -20\log\left(2\xi\sqrt{1-\xi^2}\right)[\text{dB}]. \quad (27)$$

Under the case $\xi_n \approx 0.05 \ll 1$, the valley is located roughly at $\omega_v \approx \omega_n$ with approximate 20 dB roll-off. Recalling that C_z is the design-adjustable part of C_{tot}, (25) can certainly be optimized to shift the valley location to $\omega_v = 2\pi f_0$, thus suppressing the second-harmonic component. Following a similar fashion, the damping factor ξ_d for the denominator's second-order polynomial can be derived as:

$$\xi_d = \frac{1}{2}\left(\sqrt{\frac{L_oC_o}{1-k_2^2}}\omega\left(\frac{1}{Q_{L_d}}+\frac{1}{Q_{L_o}}\right)+\frac{1}{R_L}\sqrt{\frac{L_o}{C_o}(1-k_2^2)}\right). \quad (28)$$

By substituting into the same design parameters, we can thus achieve $\xi_d \approx 0.3$, indicating that $G(s)$ involves one complex-conjugate pole pair with a corner frequency

$$\omega_{n,d} = \sqrt{\frac{1}{L_oC_o(1-k_2^2)}}. \quad (29)$$

All of the main conclusions on the complex-conjugate zero pair would pertain to the complex-conjugate pole pair apart from its amplitude–frequency response being merely a mirror image to that of the complex zeros. The initiated peaking effect resides at $\omega_{pk} \approx \omega_{n,d} \approx 4.1$ GHz with a peak amplitude of around 5 dB calculated by substituting $\xi_d \approx 0.3$ into (27). Equations (23)–(29) form a good guideline to the frequency response of the T_2 MN with respect to the locations and amplitudes of the peak and valley originated by the zeros and poles in the system. Circuit-level simulation results in Fig. 9(a) verify a total of 26-dB rejection at $2f_0 = 4.8$ GHz at a cost of sub-1 dB in passband loss. The proposed HD_2 suppression technique is fairly well contained under the expected capacitance variations, as depicted with a zoomed-in plot embedded in Fig. 9(a). In this implementation, for the sake of maintaining the high-Q factor, we retain the HD_2 suppression under process, voltage and temperature (PVT) variations [see Fig. 9(b)] through tuning C_o, which indirectly alters the valley location and depth of the system response by adapting the peaking effect at $\omega_{n,d}$ (29) and regulating V_{GB} that partly compensates for the $M_{1,\text{PA}}$ threshold voltage variation. In case an even wider frequency range would be required, the zero-shifting capacitor C_z can also be implemented with a varactor or switched capacitors (sw-cap), which could directly alter the valley location ω_v but at a cost of the reduced valley depth and power efficiency. [2]

Note that the complex-conjugate zero pair does not arise in the absence of inter-winding capacitance ($C_{\text{tot}} = 0$). Practically, it will be located at a fairly high frequency limited

[2]A quick investigation following a well-established methodology of designing an sw-cap tuning tank in a DCO for its maximum Q-factor in the ON-state and minimum parasitic capacitance in the OFF-state reveals that a 2-bit 1.7–3.7-pF range sw-cap will maintain Q $\geq$ 39 while adding $\leq$1 pF parasitic to ground. This ensures HD2 suppression of < -42 dBm with 4% degradation of the DCO-PA efficiency.

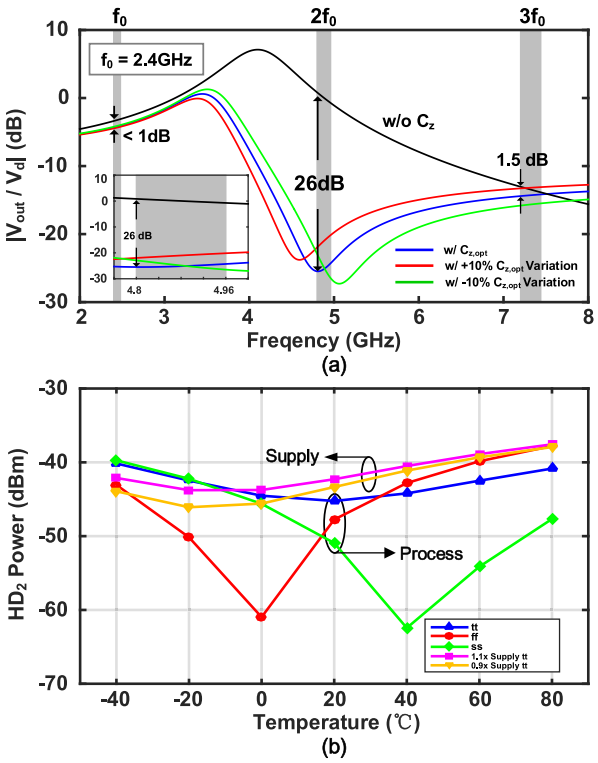

Fig. 9. (a) Simulated HD_2 suppression using the zero shifting C_z. (b) HD_2 suppression under PVT variations.

only by the intrinsic inter-winding capacitance C_{int} from the T_2 transformer. More intuitively, we name C_z as the zero-shifting capacitor, as it actually shifts the valley frequency ω_v, which is extremely close to the corner frequency ω_n of the complex zero pair when the damping factor ξ_n is small. The detailed discussion about the visible zero notch in a general non-inverting transformer with operational loading was first presented in [26]–[28].

III. Single-Pin Antenna Interface

Single-pin direct antenna connection with fully integrated T/R switches is highly desired in ULP radios in order to maximally reduce the system cost [1]. Conventional integrated T/R switches utilize series–shunt physical switch pair (carrying RF signals) in both the TX and RX modes to connect to the antenna. This incurs high insertion loss and insufficient isolation, which has been discussed thoroughly in [28]. There have been continuous efforts to merge the RX mode switches into the input MN of the LNA for high TX power tolerance and strong RX isolation through proper high-Q resonant tank design [29]–[31]. Similarly, the explicit series–shunt switches can be further eliminated [1]. All those solutions are at a cost of introducing additional LC tanks on top of the TX MN and involving complex programmable capacitor banks to assist with the mode switching. It would be preferable for the T/R switching to be accomplished by re-using the TX MN without resorting to the extra on-chip inductors/transformers, thus switching only the minimum number of capacitors.

As formerly discussed in Section II, in the TX mode, a step-down transformer is chosen to augment the equivalent

TABLE I
COMPARISON WITH STATE-OF-THE-ART INTEGRATED T/R SWITCHES

	Technology	Frequency (GHz)	SW Topology	IL (TX / RX) (dB)	Isolation (TX / RX) (dB)	Number of Ind. / Switchable Cap.	Fully-integrated RFIO
[29]	90nm	2.4	series-shunt switches with resonance	0.4 / 0.2	30 / 16	5 / 1	No
[30]	32nm	2.4	series-shunt switches with resonance	1.3 / 1.1	32 / -	>3 / 1	No
[31]	65nm	2.4	series-shunt switches with resonance	- / -	- / -	4 / 5	Yes
[1]	28nm	2.4	*soft* switches * with resonance	- / -	- / -	3 / 3	Yes
This work	65nm	2.4	*soft* switches * with resonance	- / 2.2	30 / -	1 / 1	Yes

* *soft means without any explicit switches carrying RF signals*

impedance seen at the drain of DCO-PA in order to ensure a lower RF power transfer to the antenna. On the other hand, provided that the same antenna can be reused in the RX mode, the RF signal from the antenna will then come across a step-up transformer with a passive gain boosting. This is precisely the scenario of time-division duplex (TDD) systems where TX and RX paths share an antenna while operating in the same frequency band [28]. By virtue of the proposed single-MOS DCO-PA topology with the fully integrated solutions handling the spurious emissions, the single-pin antenna interface not only eliminates any physical transmit/receive (T/R) switch in the signal path (in favor of using purely DC power switches) [32] but can also manage to share the same natural LC resonance of the transformer for the RF frequency selection in both TX and RX modes such that only one tunable capacitor (C_o) is required to fulfill the mode switching.

To take full advantage of the passive gain boosting while preserving good linearity [30] at low power consumption, a push–pull topology is exploited for the LNA in the RX mode, as shown in Fig. 10. When the DC supply switch $M_{\rm TX}$ of Fig. 12 is toggled to ground in Fig. 11(a), the single-MOS $M_{1,\rm PA}$ in the TX mode is completely cut off, turning itself into a mere capacitive load to the RX LNA symbolized by $C_{\rm p,TX}$ in the circuit model in Fig. 10(b). This can be compensated by shifting C_o (3-bit sw-cap bank) to a lower code, thus retaining good frequency selectivity of T_2-based MN at 2.4 GHz, which facilitates a more independent optimization of the TX-mode DCO-PA and RX-mode LNA. Likewise, in the TX mode, the parasitic capacitance of the RX input, which is rather small compared to $C_{\rm p,TX}$, is absorbed into the implementation of C_o. High resistance due to the OFF-state of M_2 and M_3 has a negligible penalty on the DCO-PA. Nevertheless, the single MOS $M_{1,\rm PA}$ cannot get overly large for the sake of DCO-PA efficiency, otherwise, its OFF-state parasitic $C_{\rm p,TX}$ may inadvertently break the tunability range of the switchable C_o, ruining the RX-mode input matching. Comparison with state-of-the-art integrated T/R switches is presented in Table I.

The RX-mode input matching is realized through the inductive source degeneration provided by the supply/ground

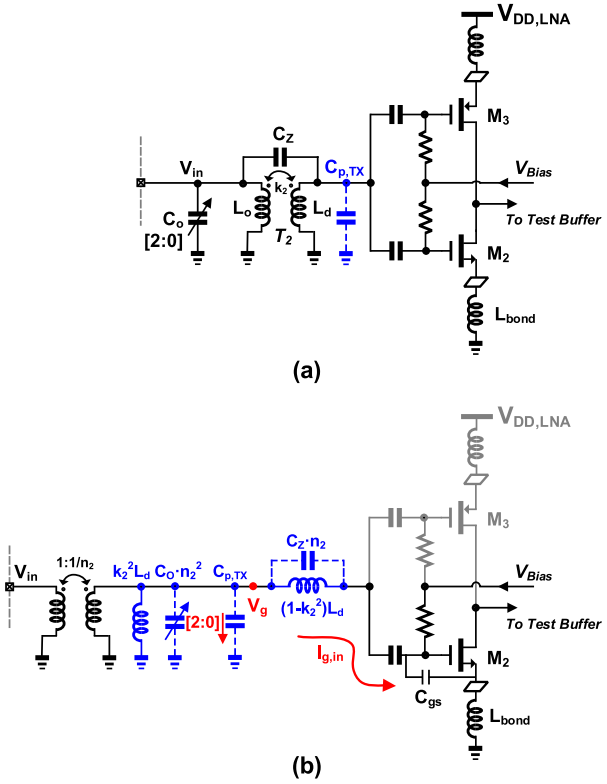

Fig. 10. (a) Transformer T_2 and the LNA in the RX mode. (b) Equivalent circuit model for LNA input matching.

bond-wire inductances $L_{\rm bd}$ to create a real part of the input impedance, thus avoiding any additional bulky on-chip inductors. Assuming a good symmetry between the PMOS and NMOS transistors, with $I_{g,\rm in}$ flowing entirely through $C_{\rm gs}$, the input impedance looking into the LNA from V_g node in Fig. 10(b) can be derived as

$$z_{in,g} \approx \frac{s\left(1-k_2^2\right)L_d}{1+\frac{s^2}{\frac{1}{\sqrt{L_o L_d}C_z\left(1-k_2^2\right)}}}+2sL_{\rm bd}+\frac{2}{sC_{\rm gs}}+\frac{2}{sC_c}+2\frac{g_{m_2}L_{\rm bd}}{C_{\rm gs}}$$
$$\approx s\left(\left(1-k_2^2\right)L_d+2L_{\rm bd}\right)+\frac{2}{sC_{\rm gs}}+\frac{2}{sC_c}+2\frac{g_{m_2}L_{\rm bd}}{C_{\rm gs}}. \quad (30)$$

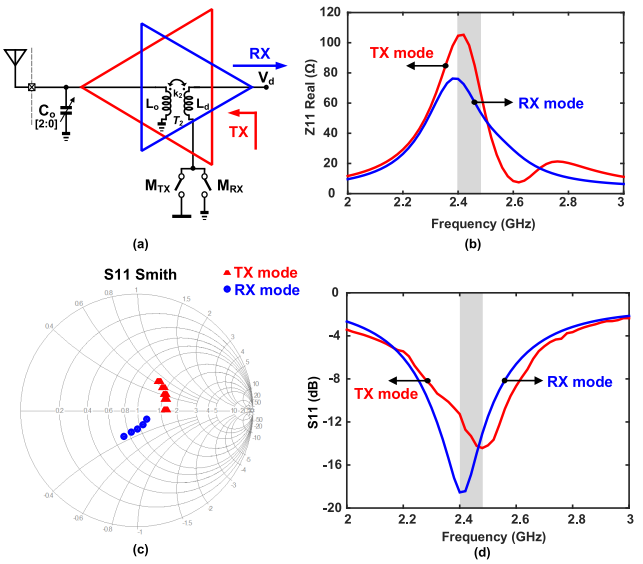

Fig. 11. (a) Proposed single-pin antenna interface. (b) Simulated Z_{11} in T/R modes. (c) Simulated S_{11} Smith chart for T/R modes. (d) Simulated S_{11}.

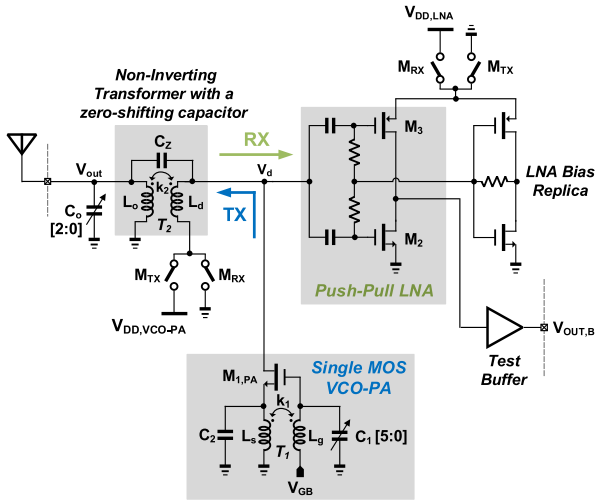

Fig. 12. Schematic of the single-pin antenna interface RFE. Port V_{out} is connected to the antenna through a bondwire in the PCB test.

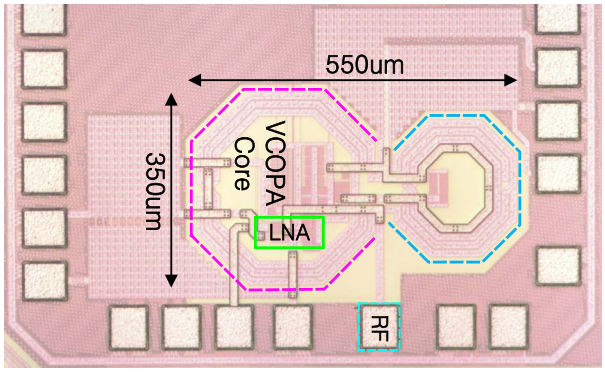

Fig. 13. Chip micrograph of the single-pin antenna interface RFE.

Note that the effect of C_z can be neglected at around ω_0 due to the induced zero in the RX mode, which is also located at $2\omega_0$ and confirmed by ω_n in (25). Deploying a

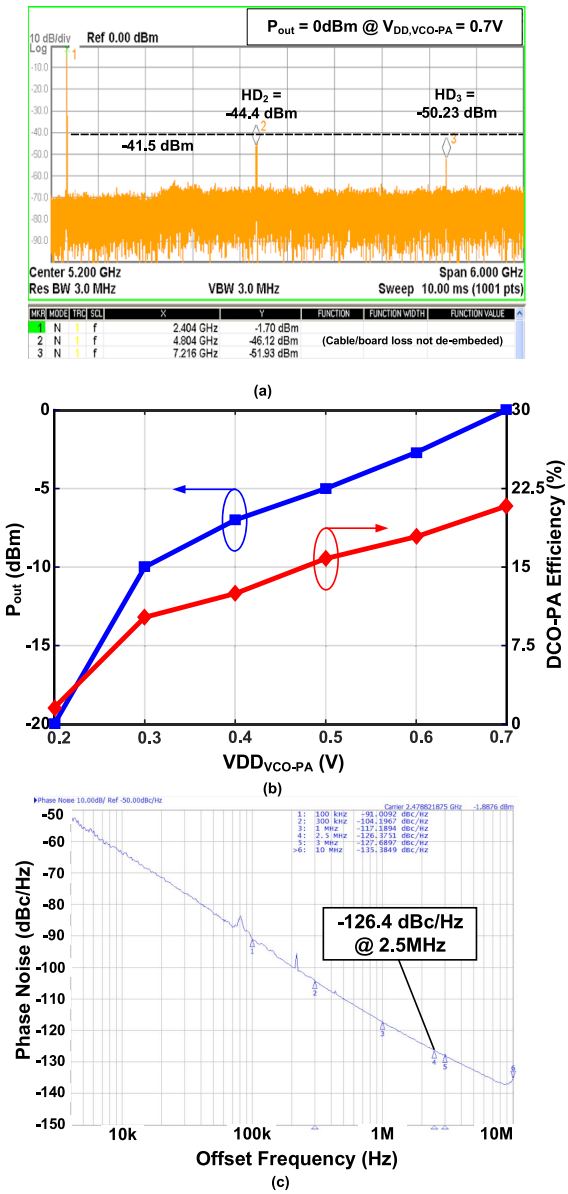

Fig. 14. TX mode measurements. (a) Single-tone output spectrum. (b) DCO-PA efficiency and P_{out} versus supply voltage. (c) DCO-PA PN under $P_{out} = 0$ dBm.

practical bond-wire inductance, $L_{bd} \approx 0.5$ nH, a real part of the impedance $z_{g,\text{real}} \approx 160\ \Omega$ with $g_{m_2} \approx 8.5$ mS and $C_{gs} \approx 53$ fF under the supply $V_{DD,LNA} = 0.5$ V. Furthermore, $z_{g,\text{real}}$ is then scaled down by a factor of n_2^2/k_2^2 when reflected to the antenna port due to the impedance transformation of T_2. The real part of impedance looked into from the antenna port is thus roughly 74 Ω, which is quite close to the simulation result shown in Fig. 11(b). Furthermore, the simulated S_{11} and Smith chart in both T/R modes are shown in Fig. 11(c) and 11(d). They cover the intended frequency band of interest of 2.4–2.48 GHz with margin and validate the feasibility of the introduced T/R switch.

The passive gain boost due to the step-up transformer is $A_{v,\text{tran}} \approx k_2/n_2 \approx k_2(L_d/L_o)^{1/2} \approx 1.5$ (3.5 dB), which is favorable for the voltage amplification and to alleviate noise contribution from the succeeding push–pull stage, thus

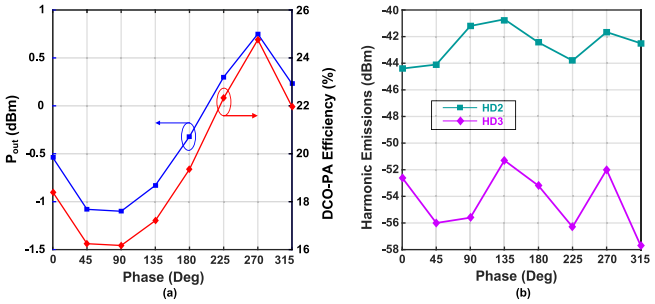

Fig. 15. TX mode measurements. (a) P_{out} and DCO-PA efficiency under VSWR = 1.5:1. (b) Harmonic emissions under VSWR = 1.5:1.

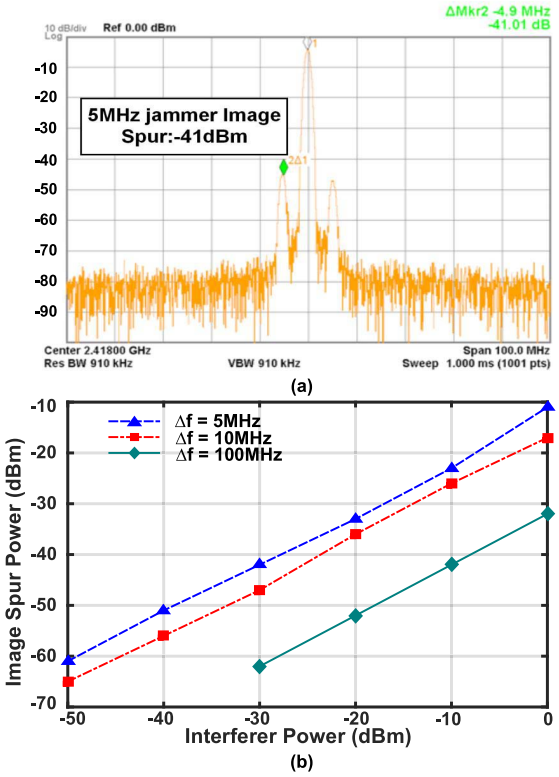

Fig. 16. Jammer resilience performance. (a) Output spectrum in face of a −30-dBm jammer at 5-MHz offset. (b) Image spur power versus the interferer power at various offsets from the carrier.

ultimately saving consumed power [33]. The noise figure (NF) of the cascaded lossy passive network and LNA is described as $\mathrm{NF_{tot}} = \mathrm{L}\cdot\mathrm{NF_{LNA}}$ in [21], while $L = P_{\mathrm{in}}/P_{\mathrm{out}}$ stands for the power loss defined by the ratio of available powers between the input and the output. Consequently, the expression for $\mathrm{NF_{tot}}$ is given as

$$\mathrm{NF_{tot}} \approx \frac{R_s M_2^2 \omega^2}{\left(R_s + r_{L_o}\right)\omega^2 + r_{L_d}\left(R_s + r_{L_o}\right)^2}\left(1 + \frac{8\gamma}{g_{m_2} R_{\mathrm{in}}}\right) \quad (31)$$

where R_s is the source impedance, r_{L_o} and r_{L_d} represent the series losses of the transformer coils, and the excess noise coefficient γ is assumed to be 2/3 for long-channel transistors. Moreover, the input resistance of the push–pull stage $R_{\mathrm{in}} = z_{g,\mathrm{real}}$, as previously discussed. The first term at the right-hand side of (31) is exactly the available power gain of the transformer. Theoretically, it gives a total

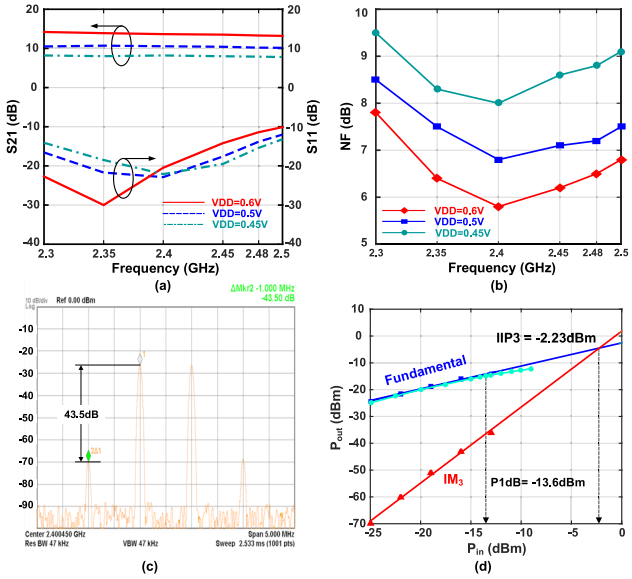

Fig. 17. RX mode (LNA) measurements. (a) S-parameters at various $V_{\mathrm{DD,LNA}}$ values. (b) NF at various $V_{\mathrm{DD,LNA}}$ values. (c) IM3 tones. (d) $P_{1\ \mathrm{dB}}$ and IIP3.

TABLE II
COMPARISON WITH STATE-OF-THE-ART 2.4-GHz LNA

	Technology	Frequency (GHz)	Supply (V)	P_{DC} (μW)	NF (dB)	Gain (dB)	IIP3 (dBm)	FOM * (dB)
[34]	65nm	2.4	0.7	475	2.8	17.4	-10.7	28.8
[35]**	40nm	2.4	0.8	30	3.3	14.2	-11.6	38.2
[35]**	40nm	2.4	0.18	30	5.2	14	-8.6	37.7
[36]	65nm	2.4	0.3	930	4.7	20.2	-20	20.7
This work	65nm	2.4	0.5	174	6.8	11	-2.2	30.2

* $\mathrm{FOM}=10\log\left(10^{\mathrm{Gain}/20}\cdot 10^{(\mathrm{IIP3}-10)/20}/(10^{\mathrm{NF}/10}\cdot P_{\mathrm{DC}}\cdot 10^{-3})\right)$ [34] ** [35] includes two LNA designs with simulation results only

$\mathrm{NF_{tot}} \approx 5.5$ dB[3] by substituting into all the design parameters at 0.5-V supply without engaging any noise cancellation technique [34]. Device mismatches introduce a maximum 0.15-dB standard deviation on the key LNA performances confirmed by the Monte Carlo simulation. At the slow–slow (SS) corner, the key performance of the LNA, namely S_{11}, S_{21}, and NF, degrades mainly attributing to the current drop, which can be easily compensated by raising the power supply a bit.

With a DC-blocking capacitor of 2 pF at the LNA output, the simulated input second-order intercept point ($\mathrm{IIP_2}$) is +42.5 dBm. Monte Carlo simulations of $\mathrm{IIP_2}$ show a standard deviation of 0.1 dB due to device mismatches.

A full schematic of the proposed single-pin antenna interface RF front end (RFE) is shown in Fig. 12. A self-biased replica circuitry is intended to bias the LNA in the RX mode. A test buffer with a low-voltage gain is designed to facilitate the measurements, especially from the system linearity standpoint. Switching between the TX/RX modes is realized through toggling the relevant supply switches between V_{DD} and ground.

[3] $\mathrm{NF_{tot}}$ will slightly increase by 0.38 dB if the gate-induced noise is considered.

TABLE III
COMPARISON WITH STATE-OF-THE-ART 2.4-GHz RFE

	CICC' 18 [12]		JSSC' 19 [7]		JSSC' 14 [16]		JSSC' 16 [13]		JSSC' 17 [14]		This work		
CMOS Technology	40nm		40nm		130nm		130nm		65nm		65nm		
Supply Voltage (V)	0.4		0.6 to 0.9		1		1.2		0.3 to 0.7		0.3 to 0.7		
RF band (GHz)	2.4		2.4		2.4		2.4		2.4		2.4		
TX Architecture (in open loop operation)	LC-VCO + Class-D PA		Ring OSC + Edge Combiner + SC-DPA		VCO-PA-LNA co-design		PA-VCO Stack		Function-Reuse Class-F DCO-PA		Single-MOS DCO-PA		
RF Power (dBm)	-10	0	-20	-3.3	-30	-4.4	-5	-1	-5	0	-20	-10	0
Power Consumption (mW) (VCO + Divider + Buffer + PA)	1.27	4.22	0.27	1.62	1.5	7	2.58	4.46	2.04	4.4	0.62	0.98	4.8
Efficiency (%)	8	23.7	3.7	28.9	0.07	5.2	12.2	17.9	15.5	22.6	1.6	10.2	20.8
Active Area (mm^2)	0.35		0.0166		0.5		0.2		0.39		0.17		
HD2/HD3 (dBm) @ P_{out}	-52 / - @ 0dBm		-42.5 / -48.5 @ 0dBm ***		N/A		-50 / -47 @ 0dBm		-43.2 / -47.6 @ 0dBm		-44.4 / -50.2 @ 0dBm		
VCO Phase Noise (dBc/Hz) @ 2.5 MHz / RF power	-123 **		-90		-125 @ -4.4dBm		-129 @ -1dBm		-125 @ 6dBm		-126 @ 0dBm -108 @ -20dBm		
VCO Frequency Range (GHz)	2.3-2.5		2.4-2.5		2.2-2.488		2.26-2.58		2.376-2.408		2.2-2.5		
TX_FOM * (dBm) @ 0dBm	-75.7		-		-		-73.5 @ -1dBm		-66.7		-67.6		
5MHz jammer Image Spur (dBm) @ -30dBm interferer	N/A		N/A		N/A		N/A		-13		-41		
Max P_{out} Variation (dB) under VSWR = 1.5 : 1 @ P_{out}	N/A		N/A		N/A		N/A		2.1dB @ 6dBm		1.1dB @ 0dBm		
VCO-PA efficiency (%) under VSWR = 1.5 : 1 @ P_{out}	N/A		N/A		N/A		N/A		14 to 27.5 @ 6dBm		16 to 24.5 @ 0dBm		
No. of external components	2		2		0		2		1		0 ****		
Integrated T/R Switch	No		No		Yes		No		No		Yes		

* TX_FOM = HD2 + 10log(PDC) [12] ** Normalized from 2X carrier frequency *** DPA operated in saturation region under 1.2V supply **** Bondwire utilized for input matching in RX mode

IV. EXPERIMENTAL RESULTS

The RFE chip is fabricated in 65-nm standard CMOS, occupying a compact active area of 0.17 mm^2, as shown in the die photograph in Fig. 13. Measurement results of the introduced RFE in the TX mode are summarized in Fig. 14. The single-MOS DCO-PA achieves 20.8% total power efficiency at 0-dBm RF output and 0.7-V supply. The measured HD_2 emission, shown in Fig. 14(a) when delivering a single tone at 0 dBm, is less than -44 dBm, which verifies the effectiveness of the zero-shifting capacitor C_z. A relatively high efficiency of 10.2% is retained at 10-dB large power back-off by scaling the supply in the TX mode to 0.3 V, which is confirmed by Fig. 14(b). The measured PN of the DCO-PA is plotted in Fig. 14(c). At 0.7-V supply, it reaches -126.4 dBc/Hz at a 2.5-MHz offset from the 2.4-GHz carrier. The DCO-PA covers a frequency tuning range from 2.2 to 2.5 GHz, leaving enough margin to cover the targeted frequency band of interest in the case of process variations. The DCO-PA stability over antenna impedance variations is measured under VSWR $=$ 1.5:1 and captured in Fig. 15. It shows a maximum 1.1-dB P_{out} variation when delivering 0-dBm RF power.

Resilience to jammers is validated in the same manner as in [14] by means of connecting the signal generator, DCO-PA output, and spectrum analyzer to a three-port circulator, which allows the signal to travel in the direction of signal generator $\rightarrow$ DCO-PA output pin $\rightarrow$ spectrum analyzer. The scenario of applying a -30-dBm interferer at $\Delta f = 5$ MHz offset frequency from the 2.4-GHz carrier is sketched in Fig. 16(a) showing a jammer image spur at -41 dBm, which is 28 dB better (lower) than that in [14], which barely provides any isolation between the antenna and oscillator. The single-MOS DCO-PA is so robust that can hardly get injection-locked by the interferers even as strong as 0 dBm, shown as the blue curve in Fig. 16(b). Jammers at large offsets of $\Delta f = 10, 100$ MHz from the carrier are also captured in the same plot.

When switching from the DCO-PA output pin to the LNA input, the measured key LNA performance metrics are shown in Fig. 17. At a 0.5-V supply, the LNA exhibits $S_{21} = 11$ dB with $S_{11} < -20$ dB, consuming only 174-μW power. The corresponding NF is 6.8 dB within which the test buffer contributes roughly 0.2 dB as per simulations. The worsened NF versus the calculation in (31) may stem from the degraded

Q-factor of the transformer in which the passive devices and wires are put right underneath and which could not be modeled in the EM simulation. The LNA performance under lower (0.45-V) or higher (0.6-V) supplies are also captured in Fig. 17(a) and (b) with 90- and 540-μW power consumption, respectively. The two-tone test is applied to measure IIP_3, as explained in Fig. 17(c) and (d). The power for fundamental tone and output inter-modulation (IM) products is captured from the spectrum analyzer and then extrapolated over increasing the fundamental tone amplitude, yielding an excellent $IIP_3 = -2.23$ dBm. Furthermore, the 1-dB compression point of the LNA is measured at -13.6 dBm. Table II compares it with state-of-the-art LNAs.

The DCO-PA performance is summarized in Table III and favorably compares with state-of-the-art 2.4-GHz TXs. To the best of our knowledge, the presented single-MOS DCO-PA architecture is the first fully integrated single-ended solution with competitive carrier PN and power efficiency, especially at low power modes while simultaneously handling the harmonic emissions and easy switching to the RX LNA. Even the most recent contender [7], which uses a ring-oscillator-based edge-combining frequency generation TX, no longer shows the power efficiency advantage at lower (-20 dBm) RF power, especially given that only drain efficiency is reported there with off-chip matching and filtering. In addition, the proposed single-MOS DCO-PA outperforms it at least 18 dB in terms of PN performance. The deep HD_2 rejection is achieved (< -44 dBm) without resorting to complex circuitry, external filtering, or calibration and with insignificant degradation in power efficiency.

V. Conclusion

A simple RFE with a fully integrated MN for 2.4-GHz TDD radios is introduced in this article. It features a function-reuse single-MOS DCO-PA with full V_{DD} utilization while improving antenna-to-DCO isolation for better resilience to interferers. The second-harmonic emission is deeply suppressed by a zero-shifting capacitor that crosses over the non-inverting matching transformer. This not only allows sharing the same antenna pin with the RX but also provides passive-gain boosting to the push–pull LNA.

Acknowledgment

The authors would like to thank Integrand Software for the EMX license.

References

[1] F.-W. Kuo *et al.*, "A Bluetooth low-energy transceiver with 3.7-mW all-digital transmitter, 2.75-mW high-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1144–1162, Apr. 2017.

[2] M. Ding *et al.*, "A 0.8 V 0.8 mm^2 Bluetooth 5/BLE digital-intensive transceiver with a 2.3 mW phase-tracking RX utilizing a hybrid loop filter for interference resilience in 40 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 446–448.

[3] Y.-H. Liu *et al.*, "13.2 A 3.7 mW-RX 4.4 mW-TX fully integrated Bluetooth low-energy/IEEE802.15.4/proprietary SoC with an ADPLL-based fast frequency offset compensation in 40 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[4] W. Yang *et al.*, "A +8 dBm BLE/BT transceiver with automatically calibrated integrated RF bandpass filter and −58 dBc TX HD2," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig Tech. Papers*, Feb. 2017, pp. 136–137.

[5] H. Liu *et al.*, "An ADPLL-centric Bluetooth low-energy transceiver with 2.3 mW interference-tolerant hybrid-loop receiver and 2.9 mW single-point polar transmitter in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 444–446.

[6] M. Babaie *et al.*, "A fully integrated Bluetooth low-energy transmitter in 28 nm CMOS with 36% system efficiency at 3 dBm," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1547–1565, Jul. 2016.

[7] X. Chen *et al.*, "Analysis and design of an ultra-low-power Bluetooth low-energy transmitter with ring oscillator-based ADPLL and 4×frequency edge combiner," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1339–1350, May 2019.

[8] Y. Shi, X. Chen, H.-S. Kim, D. Blaauw, and D. Wentzloff, "28.3 A 606 μW mm-scale Bluetooth low-energy transmitter using co-designed 3.5×3.5 mm^2 loop antenna and transformer-boost power oscillator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 442–444.

[9] S. Yang, J. Yin, H. Yi, W.-H. Yu, P.-I. Mak, and R. P. Martins, "A 0.2-V energy-harvesting BLE transmitter with a micropower manager achieving 25% system efficiency at 0-dBm output and 5.2-nW sleep power in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1351–1362, May 2019.

[10] C.-C. Li, M.-S. Yuan, C.-C. Liao, Y.-T. Lin, C.-H. Chang, and R. B. Staszewski, "All-digital PLL for Bluetooth low energy using 32.768-kHz reference clock and ≤0.45-V supply," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3660–3671, Dec. 2018.

[11] O. E. Eliezer, R. B. Staszewski, I. Bashir, S. Bhatara, and P. T. Balsara, "A phase domain approach for mitigation of self-interference in wireless transceivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1436–1453, May 2009.

[12] M. Sharifzadeh, A. H. Masnadi-Shirazi, Y. Rajavi, H. M. Lavasani, and M. Taghivand, "A fully integrated multi-mode high-efficiency transmitter for IoT applications in 40 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.

[13] C. Li and A. Liscidini, "Class-C PA-VCO cell for FSK and GFSK transmitters," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1537–1546, Jul. 2016.

[14] X. Peng, J. Yin, P.-I. Mak, W.-H. Yu, and R. P. Martins, "A 2.4-GHz ZigBee transmitter using a function-reuse class-F DCO-PA and an ADPLL achieving 22.6% (14.5%) system efficiency at 6-dBm (0-dBm) P_{out}," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1495–1508, Jun. 2017.

[15] J. Ebert and M. Kazimierczuk, "Class E high-efficiency tuned power oscillator," *IEEE J. Solid-State Circuits*, vol. 16, no. 2, pp. 62–66, Apr. 1981.

[16] S. Sayilir *et al.*, "A −90 dBm sensitivity wireless transceiver using VCO-PA-LNA-switch-modulator co-design for low power insect-based wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 996–1006, Apr. 2014.

[17] K. Xu, J. Yin, P.-I. Mak, R. B. Staszewski, and R. P. Martins, "A 2.4-GHz single-pin antenna interface RF front-end with a function-reuse single-MOS VCO-PA and a push-pull LNA," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2018, pp. 293–294.

[18] A. W. L. Ng, G. C. T. Leung, K.-C. Kwok, L. L. K. Leung, and H. C. Luong, "A 1-V 24-GHz 17.5-mW phase-locked loop in a 0.18-μm CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1236–1244, Jun. 2006.

[19] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[20] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[21] B. Razavi, *RF Microelectronics* (Prentice-Hall Communications Engineering and Emerging Technologies Series). Upper Saddle River, NJ, USA: Prentice-Hall, 2011.

[22] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "Transformer-based dual-mode voltage-controlled oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 4, pp. 293–297, Apr. 2007.

[23] V. Bhagavatula and J. C. Rudell, "Analysis and design of a transformer-feedback-based wideband receiver," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1347–1358, Mar. 2013.

[24] K. Xu *et al.*, "A 0.85 mm^2 51%-efficient 11-dBm compact DCO-DPA in 16-nm FinFET for sub-gigahertz IoT TX using HD_2 self-suppression and pulling mitigation," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 2028–2037, Jul. 2019.
[25] Y. Hu, T. Siriburanon, and R. B. Staszewski, "A low-flicker-noise 30-GHz class-F_{23} oscillator in 28-nm CMOS using implicit resonance and explicit common-mode return path," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1977–1987, Jul. 2018.
[26] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.
[27] Q. Liu *et al.*, "A 1.4-to-2.7 GHz high-efficiency RF transmitter with an automatic 3FLO-suppression tracking-notch-filter mixer supporting HPUE in 14 nm FinFET CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 172–174.
[28] X. Xiao *et al.*, "A 65-nm CMOS wideband TDD front-end with integrated T/R switching via PA re-use," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1768–1782, Jul. 2017.
[29] A. A. Kidwai, C.-T. Fu, J. C. Jensen, and S. S. Taylor, "A fully integrated ultra-low insertion loss T/R switch for 802.11b/g/n application in 90 nm CMOS process," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1352–1360, May 2009.
[30] C.-T. Fu, H. Lakdawala, S. S. Taylor, and K. Soumyanath, "A 2.5 GHz 32 nm 0.35 mm^2 3.5 dB NF −5 dBm P1 dB fully differential CMOS push-pull LNA with integrated 34 dBm T/R switch and ESD protection," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 56–58.
[31] Z. Sun *et al.*, "A 0.85 mm^2 BLE transceiver with embedded T/R switch, 2.6 mW fully-passive harmonic suppressed transmitter and 2.3 mW hybrid-loop receiver," in *Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2018, pp. 310–313.
[32] T. Sano *et al.*, "13.4 A 6.3 mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
[33] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "A wideband noise-canceling CMOS LNA exploiting a transformer," in *Proc. IEEE Radio Freq. Integr. Circuits (RFIC) Symp.*, Jun. 2006, p. 4.
[34] M. Rahman and R. Harjani, "A 2.4-GHz, sub-1-V, 2.8-dB NF, 475-μW dual-path noise and nonlinearity cancelling LNA for ultra-low-power radios," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1423–1430, May 2018.
[35] E. Kargaran, D. Manstretta, and R. Castello, "Design and analysis of 2.4 GHz 30 μW CMOS LNAs for wearable WSN applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 3, pp. 891–903, Mar. 2018.
[36] F. Zhang, Y. Miyahara, and B. P. Otis, "Design of a 300-mV 2.4-GHz receiver using transformer-coupled techniques," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3190–3205, Dec. 2013.

Kai Xu (Student Member, IEEE) was born in Dongying, China. He received the B.Sc. degree *(summa cum laude)* from Shandong Normal University, Jinan, China, in 2012, and the M.Sc. degree in electronics engineering from Peking University, Beijing, China, in 2015. He has recently defended his Ph.D. thesis at University College Dublin, Dublin, Ireland.

From 2018 to 2019, he was with imec-Holst Center, Eindhoven, The Netherlands, as an RFIC Research and Development Intern. From 2013 to 2014, he was with imec/INTEC_Design Group (now IDLab), Ghent University, Ghent, Belgium, as an Exchange Student. In 2015, he was a Visiting Scholar with the John A. Paulson School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, USA. From 2017 to 2018, he was a Visiting Research Assistant with the State Key Laboratory of Analog and Mixed-Signal Very Large Scale Integration (VLSI), University of Macau, Macau. He held an industry internship at Beijing BLX IC Design Corporation, Beijing, during the summer of 2017. He currently holds a post-doctoral position at UCD and Equal1 Labs, Dublin, Ireland, as a high-speed communication link designer for CMOS quantum computers. His current research interests include CMOS ultra-low-power (ULP) RF and mixed-signal integrated circuits and systems for wireless/wireline communications and quantum computing.

Mr. Xu serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON CIRCUITS and SYSTEMS—I: REGULAR PAPERS and the IEEE TRANSACTIONS ON CIRCUITS and SYSTEMS—II: EXPRESS BRIEFS.

Jun Yin (Member, IEEE) received the B.Sc. and M.Sc. degrees in microelectronics from Peking University, Beijing, China, in 2004 and 2007, respectively, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology, Hong Kong, in 2013.

He is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau. His research interests are on the CMOS RF integrated circuits for wireless communication and radar systems.

Pui-In Mak (Fellow, IEEE) received the Ph.D. degree from the University of Macau (UM), Macau, in 2006.

He is currently a Full Professor with the Department of Electrical and Computer Engineering, Faculty of Science and Technology, UM, where he is also an Associate Director (Research) of the State Key Laboratory of Analog and Mixed-Signal VLSI. He has been inducted as an Overseas Expert of the Chinese Academy of Sciences since 2018. His research interests include analog and radio frequency circuits and systems for wireless and multidisciplinary innovations.

Prof. Mak is a fellow of the IET. He was the TPC Vice Co-Chair of ASP-DAC in 2016 and a TPC Member of A-SSCC from 2013 to 2016, ESSCIRC from 2016 to 2017, and ISSCC from 2017 to 2019. He was a member of the Board of Governors of the IEEE Circuits and Systems Society from 2009 to 2011. He has been a Distinguished Lecturer of the IEEE Circuits and Systems Society from 2014 to 2015 and the IEEE Solid-State Circuits Society from 2017 to 2018. He was a co-recipient of the DAC/ISSCC Student Paper Award in 2005, the CASS Outstanding Young Author Award in 2010, the National Scientific and Technological Progress Award in 2011, the Best Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS and SYSTEMS—II: EXPRESS BRIEFS from 2012 to 2013, the A-SSCC Distinguished Design Award in 2015, the ISSCC Silkroad Award in 2016, and the Honorary Title of Value for Scientific Merits by the Macau Government in 2005. He was the Editorial Board Member of the IEEE Press from 2014 to 2016 and a Senior Editor of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS from 2014 to 2015. He has been an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS since 2018 and the IEEE SOLID-STATE CIRCUITS LETTERS since 2017. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS and SYSTEMS—I: REGULAR PAPERS from 2010 to 2011 and from 2014 to 2015, and the IEEE TRANSACTIONS ON CIRCUITS and SYSTEMS—II: EXPRESS BRIEFS from 2010 to 2013. He has been a Distinguished Lecturer of the IEEE Circuits and Systems Society since 2018.

Robert Bogdan Staszewski (Fellow, IEEE) was born in Bialystok, Poland. He received the B.Sc. *(summa cum laude)*, M.Sc., and Ph.D. degrees in electrical engineering from The University of Texas at Dallas, Richardson, TX, USA, in 1991, 1992, and 2002, respectively.

From 1991 to 1995, he was with Alcatel Network Systems, Richardson, where he was involved in SONET cross-connect systems for fiber optics communications. He joined Texas Instruments Inc., Dallas, TX, USA, in 1995, where he was an elected Distinguished Member of Technical Staff (limited to 2% of technical staff). From 1995 to 1999, he was engaged in advanced CMOS read channel development for hard disk drives. In 1999, he co-started the Digital RF Processor (DRP) Group, Texas Instruments, with a mission to invent new digitally intensive approaches to traditional RF functions for integrated radios in deeply scaled CMOS technology. He was appointed as a CTO of the DRP group from 2007 to 2009. In 2009, he joined the Delft University of Technology, Delft, The Netherlands, where currently he holds a guest appointment of Full Professor (*Antoni van Leeuwenhoek Hoogleraar*). Since 2014, he has been a Full Professor with the University College Dublin (UCD), Dublin, Ireland. He is also a Co-Founder of a startup company, Equal1 Labs, with design centers located in Silicon Valley and Dublin, Ireland, aiming to produce single-chip CMOS quantum computers. He has authored or coauthored five books, eight book chapters, and 110 journal and 200 conference publications. He holds 190 issued U.S. patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters, and receivers as well as quantum computers.

Dr. Staszewski was a recipient of the 2012 IEEE Circuits and Systems Industrial Pioneer Award. He was a TPC Chair of the 2019 IEEE ESSCIRC Conference, Krakow, Poland. In May 2019, he received the title of Professor from the President of the Republic of Poland.

Rui P. Martins (Fellow, IEEE) was born in April 30, 1957. He received the bachelor's, master's, Ph.D., and the Habilitation for Full-Professor degrees in electrical engineering and computers from the Department of Electrical and Computer Engineering (DECE), Instituto Superior T*é*cnico (IST), University of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the DECE/IST, University of Lisbon, since October 1980. Since 1992, he has been on leave from the University of Lisbon and with the DECE, Faculty of Science and Technology (FST), University of Macau (UM), Macao, where he has been a Chair-Professor since August 2013. In FST, he was the Dean of the Faculty from 1994 to 1997 and has been a Vice-Rector of UM since 1997, from September 2008 to August 2018, Vice-Rector (Research) and from September 2018 to August 2023, Vice-Rector (Global Affairs). Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and, in UM, has supervised (or cosupervised) 46 theses, Ph.D. (25) and masters (21). He has coauthored seven books and 11 book chapters; 33 patents, USA (30) and Taiwan (3); 507 articles, in scientific journals (188) and in conference proceedings (319); and other 64 academic works, in a total of 622 publications. In 2003, he created the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in January 2011 to the State Key Laboratory (SKLAB) of China (the first in Engineering in Macao), being its Founding Director. He was the Founding Chair of UMTEC (UM company) from January 2009 to March 2019, supporting the incubation and creation in 2018 of Digifluidic, Macau SAR, the first UM spin-off, whose CEO is a SKLAB Ph.D. graduate. He was also a Co-Founder of Chipidea Microelectronics (Macao) [now Synopsys-Macao], Macau SAR, in 2001.

Dr. Martins received the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award in 2016. He received two Macao Government decorations: the Medal of Professional Merit (Portuguese-1999) and the Honorary Title of Value (Chinese-2001). He was the Vice-President and the President of the Association of Portuguese Speaking Universities (AULP) from 2005 to 2014 and from 2014 to 2017, respectively. In July 2010, he was elected, unanimously, as a Corresponding Member of the Lisbon Academy of Sciences, being the only Portuguese Academician living in Asia. He was the Founding Chair of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of the IEEE CAS Society (CASS)], the General Chair of the IEEE Asia-Pacific Conference on CAS (APCCAS 2008), the Vice-President (VP) of Region 10 (Asia, Australia, and Pacific) from 2009 to 2011, and a VP-World Regional Activities and Membership of the IEEE CASS from 2012 to 2013, an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS and SYSTEMS—II: EXPRESS BRIEFS from 2010 to 2013. He was nominated as the Best Associate Editor for the period of 2012–2013. He was a member of the IEEE CASS Fellow Evaluation Committee as the Chair in 2013, 2014, and 2018, and in 2019; the IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS) in 2014; and the IEEE CASS Nominations Committee from 2016 to 2017. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC 2016).