A 0.7–5.7 GHz Reconfigurable MIMO Receiver Architecture for Analog Spatial Notch Filtering Using Orthogonal Beamforming

Sajad Golabighezelahmad[®], Student Member, IEEE, Eric A. M. Klumperink[®], Fellow, IEEE, and Bram Nauta^D, *Fellow*, *IEEE*

Abstract—A highly reconfigurable direct-conversion softwaredefined multiple-input multiple-output (MIMO) receiver with four RF inputs and four I/Q baseband outputs is proposed. It allows for digital MIMO but also analog interference rejection by spatial notch filtering through four flexible and simultaneous orthogonal beams. A segmented constant-Gm vector modulator (VM) with improved interference tolerance and wide RF frequency range targeting the sub-6-GHz bands is proposed. It exploits current-domain beamforming before I-V conversion by transimpedance amplifiers. A 0.7-5.7-GHz 22-nm fully depleted silicon-on-insulator (FD-SOI) prototype chip achieves >29 dB spatial filtering for a single notch and an ultrawideband 20-dB notch suppression bandwidth of 2.3 GHz at broadside excitation at an local oscillator (LO) frequency of 2.5 GHz. In the notches, an IIP3 of +16 dBm and B1dB of -11.5 dBm at a 41-dB gain is achieved, improving IIP3 and B1dB by 35 and 27 dB, respectively, by spatial filtering. A single-element noise figure (NF) of 5.5-7 dB is achieved on the VM constellation corners, degrading about 2 dB on the points nearby the biggest circle fitting into a square constellation. However, sub-3-dB system NF is potentially achievable, taking into account up to 6-dB improvement by the four-element beamforming. Given both gain and phase control provided by the VM, spatial patterns with up to three independent nulls can be synthesized with the four-element antenna array. The chip of 0.52 mm² active area consumes 77-139 mW at an LO-frequency of 0.7-5.7 GHz from a 0.8-V supply.

Index Terms—Analog beamforming, interference rejection, multiple-input multiple-output (MIMO), receiver, software-defined radio, spatial filtering, vector modulator (VM).

I. INTRODUCTION

THE increasing demand for wireless connectivity is leading to congested radio spectrum, especially in the sub-6-GHz bands that are favored over millimeter-wave frequencies for their propagation characteristics and energy efficiency. This makes the interference problem a major challenge for wireless systems. To reduce interference, a cognitive radio (CR) can sense the spectrum and allocate free channels to

Manuscript received April 8, 2020; revised July 1, 2020 and September 1, 2020; accepted September 21, 2020. This work was supported by Dutch Research Council (NWO) through the TTW-Research Program MIRABEAM under Project 14689. This article was approved by Associate Editor Pui-In Mak. (Corresponding author: Sajad Golabighezelahmad.) The authors are with the IC Design Group, Faculty of Electrical Engineering, Mathematics, and Computer Science, University of Twente,

7500 Enschede, The Netherlands (e-mail: s.golabighezelahmad@utwente.nl). Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2020.3028811

users [1]. Moreover, the spatial domain provides other degreesof-freedom to the interference problem. At the receiver side, this can be achieved by canceling out the unwanted signals using spatial filtering.

Multiple antenna systems are needed to leverage spatial signal processing techniques in the analog and digital domains. In analog beamforming phased-array receivers [2]-[8], amplitude and/or phase weighting is applied to multiple antenna signals before summing into a single output that only requires one analog-to-digital converter (ADC) per array. Analog beamforming is a favorable method because of SNR improvement, its ability to cancel out the interferers before entering the ADC, and its ability to improve the interference robustness of the receiver. However, many analog beamforming receivers lack flexibility to realize adaptive beamforming. On the other hand, digital multiple-input multiple-output (MIMO) systems are capable of more advanced signal processing, achieving an improved data capacity and link reliability for realistic channel models, i.e., propagation reflections and multipath fading environments [9]. In a digital MIMO receiver, however, element-level analog-to-digital conversion exposes the RF front ends and following ADCs to strong in-band interferes, as shown in Fig. 1(a), limiting the dynamic range of the receiver. Adding analog spatial filtering before entering the ADCs can relax dynamic range limits [the baseband implementation is shown in Fig. 1(b)] [10]–[17].

Only a few research articles have focused on spatial notch filtering techniques for MIMO receivers in sub-6-GHz bands [12], [14], [16]. The cancellation at RF, implemented at the LNA output in [11] at 10 GHz requires bulky and band-limiting quadrature hybrids that makes its implementation less attractive for low-GHz frequencies. A sigma-deltabased IF/baseband digital MIMO beamformer was proposed in [18]. Mondal and Paramesh [19] presents an adaptive beam/null-steering mm-wave MIMO receiver. An analog-fast fourier transform (FFT)-based spatio-spectral MIMO Rx was presented in [20]. In [12], a spatial filter realizing one notch in a programmable direction was proposed. The notch is realized in the baseband, after RF amplification and frequency downconversion through a feed-forward canceling circuit, consisting of an angle-independent signal path and a beamformer that contains only the interferer. As linearity and notch rejection bandwidth are limited in [12], Zhang and Krishnaswamy [14] improve them by canceling interference current to avoid

0018-9200 © 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

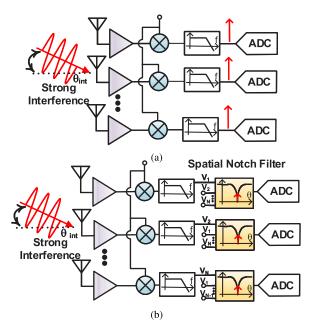


Fig. 1. (a) Conventional digital MIMO receiver array that is susceptible to a strong co-channel interferer, demanding a high-dynamic range ADC. (b) MIMO receiver incorporating analog spatial notch filtering in the baseband for relaxing the ADC dynamic range [12]–[17].

voltage swing at the output of the baseband beamformer. In addition, the synthesis of multiple notches was demonstrated. Although frequency-translated baseband spatial notch impedance reduces RF gain somewhat, distortion in the RF front-end and active baseband beamformer poses linearity limitations. In [12] and [14], a high-voltage swing at the low noise transconductance amplifier (LNTA) output due to voltage-mode operation of the passive mixer inherently limits the RF frequency range.

In this article, we describe a new reconfigurable multibeam architecture supporting both digital MIMO and analog spatial filtering [21]. Spatial interference rejection is achieved using a set of flexible orthogonal beams with a programmable spatial direction. RF/analog beamforming is realized by an improved constant-Gm vector modulator (VM). In addition to significant linearity enhancement, RF frequency range is extended in a compact and power-efficient way, so that the MIMO receiver covers sub-6-GHz bands in a software-defined radio fashion. Compared with [21], this article explains the concept in depth provides an analysis of key performance parameters and adds extra measurement results. Furthermore, the LNTA has been redesigned, and a new chip was fabricated to improve the noise performance of the receiver. Section II discusses the proposed receiver architecture. Section III provides the details of circuit implementation, while circuit analysis is presented in Section IV. The experimental results and performance comparison with the state-of-the-art are included in Section V. Finally, Section VI concludes this article.

II. PROPOSED INTERFERENCE NULLING RECEIVER A. Orthogonal Multibeamforming MIMO Receiver Architecture

The principle of the proposed MIMO receiver is shown in Fig. 2, where N orthogonal beams are formed for an

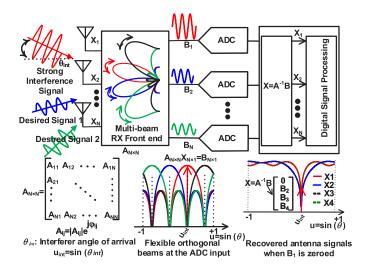


Fig. 2. Proposed analog spatial notch filtering using orthogonal analog beamforming. N orthogonal beams result for N half-wavelength spaced antennas.

N-element antenna array and the N ADCs digitize analog beamformed outputs, rather than the individual antenna signals, as in Fig. 1(a). Mathematically, the output beams are independently weighted sums of the input signals. There are as many beams as antenna elements; therefore, they can be used to recover the received signal of each antenna element for further signal processing, providing full-digital MIMO functionality. Overall, the system can be considered as a hybrid beamforming system with analog beamforming targeting rejection of the strongest interferers prior to A/D conversion, while the digital part does regular digital MIMO processing. The digital part also adaptively controls the analog rejection, but this will be addressed in a future article. Here, we demonstrate the interference rejection capabilities of the analog front end. The basic idea of the proposed architecture is to separate a strong interferer from a weaker wanted signal, assuming they come from different directions. As shown in Fig. 2, this can be achieved using orthogonality, i.e., the beam angle of one output corresponds to the nulls of other outputs (see the lower middle plots in Fig. 2). This feature allows for capturing the interferer in only one beam, e.g., B_1 in Fig. 2, and reject it at all other remaining outputs, relaxing the dynamic range of all analog circuits after the summing point including the corresponding ADCs. As shown in [22], orthogonality ensures that no information is lost after combining input signals. Hence, orthogonal multibeamforming being lossless makes it compatible with an MIMO system.

The described interference rejection by orthogonal beamforming is equivalent to analog spatial notch filtering shown in Fig. 1(b). However, with the proposed method, the notch filtering is achieved by recovering the antenna signals arriving from directions other than the notch angle-of-incidence in the digital domain, as shown in the lower right of Fig. 2. This can be done simply by ignoring the heavily distorted output beam containing the interference (e.g., $B_1 = 0$). If the inverse of analog preprocessing matrix ($A_{N\times N}$) is applied to the ADC outputs, the input antenna signals can be reconstructed while forming a spatial notch in interferer's angle-of-arrival,

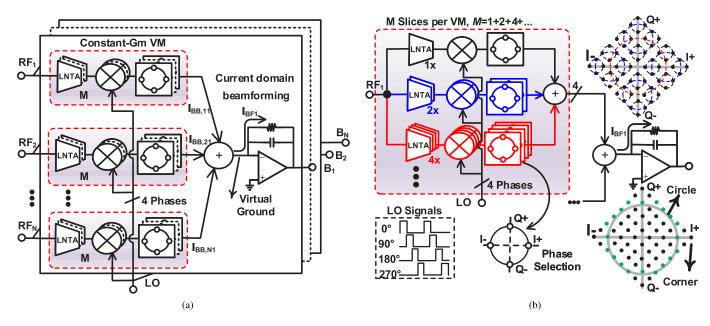


Fig. 3. (a) Proposed architecture of multibeam MIMO receiver with multiple RF phased arrays and current domain beamforming. (b) Proposed segmented constant-Gm VM with current summing at the input of TIA. This structure of M slices is repeated N times per beam for beamforming. An example constellation created by a constant-Gm VM with M = 1 + 2 + 4 = 7 slices (8 × 8 points). The points nearby the biggest circle fitting into the constellation square are used for beam steering in an arbitrary direction.

as shown in the lower right of Fig. 2. Note that this will not make the system 4×3 MIMO (e.g., zero one output with N = 4) and all four antenna signals can be reconstructed in the directions away from B_1 beam (θ_{int}). The key point here is that B_1 does not contribute significant useful information in the other directions anyway $(B_1$ has nulls in the main beam directions of B_2 , B_3 , and B_4 and "in between" contributes a relatively small part of the signal). Therefore, zeroing B_1 can admittedly result in some SNR degradation (up to 2.6 dB with four antenna elements at the sidelobes of B_1), but all N = 4antenna signals can be reconstructed in the other directions. Although in a single-beamformed output, the main reception angle cannot be arbitrarily steerable if a null angle is fixed, and this does not limit the field-of-view for the proposed multibeam system because other outputs can still provide significant signal power. This is evident from the lower right plots in Fig. 2, where the reconstructed antenna signal's spatial patterns are almost flat across the out-of-notch angles. It is also possible to reduce the signal gain (AGC) in the interference beam direction in order to fit it to the ADC dynamic range. This likely comes at the cost of some NF degradation in that direction, but it is then at least possible to use that signal digitally. Doing so, the full MIMO capability is still available, allowing to gather signals from all directions, avoiding loss of useful signals that might arrive from the interferer direction as well. Overall, this method promises better interference tolerance because each ADC is only exposed to the interfering signals coming from the direction that analog beams are steered in, while the ADCs in Fig. 1(b) are more susceptible to interference because of their larger field-of-view.

Several receiver architectures can be envisioned to create a multibeam phased-array receiver. A traditional approach is to use RF multibeam matrices, such as a Butler matrix [23]. Recent CMOS implementation of this passive network can be

found in [24]. However, a Butler matrix can only provide fixed beams, lacking the flexibility for arbitrary spatial interference cancellation. While a passive Butler matrix can be highly linear, it consists of bulky passive hybrid couplers that are dedicated for a rather narrow and fixed frequency band and not very CMOS friendly. To overcome these limitations, we propose a flexible multibeam MIMO receiver architecture employing parallel RF phased arrays, as shown in Fig. 3(a). The key feature of the proposed architecture is that it performs analog beamforming directly after V-I conversion by LNTAs in the current-mode domain [see Fig. 3(a)]. This allows for direct interference cancellation at the transimpedance amplifier (TIA) input before I-V conversion, and thus, before voltage amplification, resulting in high linearity and blocker tolerance. Essentially, a virtual ground is provided at the input of TIA which frequency translates to the LNTA output as well, reducing the voltage swing at internal nodes of the receiver [see Fig. 3(a)]. This not only protects the LNTAs against hard compression but also minimizes the distortion induced by the LNTAs and following TIA circuit. Note that we aim to reject a strong co-channel interferer for which spectral filtering is fundamentally absent.

A fully passive mixer-first realization of the proposed MIMO architecture, as adopted in a single analog beam in [5], can offer even better linearity performance. However, a fully passive architecture does not provide gain, but rather splits in received input signal power to multiple paths. This inherently introduces a noise figure (NF) penalty, which is likely unacceptable (4 paths, 12 dB).

B. Improved Vector Modulator

We propose an improved segmented constant-Gm VM [8], as shown in Fig. 3(b), to realize amplitude weighting and phase shifting for the MIMO receiver of Fig. 3(a). The underlying principle of this power-efficient VM is to slice up an RF front end consisting of an LNTA followed by a four-phase passive mixer into M equal slices that are grouped in a binary format, each group of which can contribute either to the I+, Q+, I-, or Q- baseband output via a phase selection block implemented by static reconfiguration switches in baseband, where parasitic capacitances of the switches are not problematic. This results in a rotated square constellation having $(M + 1) \times (M + 1)$ points, an example of which is shown for M = 1 + 2 + 4 = 7, in Fig. 3(b).

The main bottlenecks of the constant-Gm VM in [8] are its low RF gain and limited RF frequency range. We have addressed these limitations with the proposed current summing at the TIA input, as shown in Fig. 3(b), instead of averaging by charge sharing on the baseband capacitor like in [8]. As the TIA in Fig. 3(b) provides a low input impedance, the LNTA output node experience a low voltage swing, which results in an extended RF frequency range and improved linearity [25], [26]. Moreover, a higher gain that is not limited to the intrinsic gain of the LNTA can be achieved if a TIA with high feedback resistance is adopted. However, this puts a higher gain-bandwidth requirement on the TIA for the virtual ground argument to hold.

For the proposed receiver architecture with four antenna elements, in order to achieve maximum SNR in the absence of strong interferers, the corner points of the constellation (maximum gain) are best used to provide four analog orthogonal beams at u = 0, u = 1/2, u = -1/2, u = 1, where $u = \sin(\theta)$, as shown in Fig. 2, while MIMO functionality can be achieved in the digital domain. In the presence of one strong interference, the equal amplitude points near the biggest circle fitting into the constellation square [Fig. 3(b)] are best used to form a spatial notch in the interfere's angle-ofincidence as explained earlier. Although this results in some SNR degradation, in the presence of an interferer, the system performance would mainly be limited by the interferer instead of noise; therefore, the interference cancellation brings much more benefit than the degradation in noise. In the case of multiple interferes, more complex beam patterns with several deep notches are possible, as the proposed VM provides both phase and amplitude control.

III. CIRCUIT IMPLEMENTATION

A direct-conversion multibeam MIMO receiver with 4 RF inputs and 4 I/Q baseband outputs is implemented in Global-Foundries 22-nm fully depleted silicon-on-insulator (FD-SOI) technology, as shown in Fig. 4. Each VM provides a complex weight to realize flexible analog beams using M = 15 slices, which are grouped in a binary format, i.e., 8 + 4 + 2 + 1 = 15 to simplify digital control. This results in a 16×16 points square constellation having 44 equidistant phase points with equal weights on the biggest circle fitting into the constellation points, which leads to a null depth of approximately 29 dB [8]. An off-chip differential reference signal at twice the local oscillator (LO) frequency is used to generate the 4-phase 25% duty cycle clock signals by an on-chip divide-by-two and logic

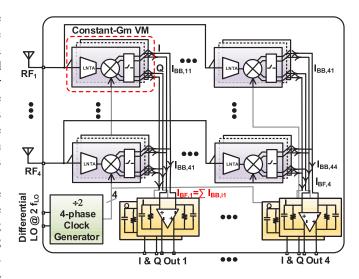


Fig. 4. Circuit implementation of multibeam 4×4 MIMO receiver employing 16 constant-Gm VMs with current summing (interference rejection) at the input of the TIAs.

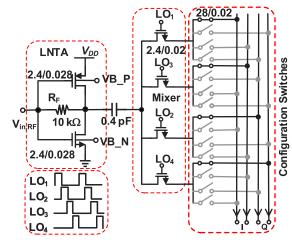


Fig. 5. Unit slice of the VM.

circuits. The resulting quadrature clock signals are distributed throughout the chip to drive the mixer switches.

A. Unit Slice Circuit

Fig. 5 shows the transistor level implementation for the unit slice of the VM, where a self-biased inverter-based LNTA with shunt feedback resistor is followed by a 4-phase passive mixer driven by 25% duty cycle clock signals. For the LNTA, slightly bigger than minimum-channel-length devices are used to increase the LNTA output resistance and minimizing their gate noise. The back gate voltages for both nMOS and pMOS LNTA transistors are available outside the chip and can be used to tune LNTA's transconductance off-chip if needed during the experiments. These back gates have always been tied to ground for all measurements presented in this article. The ac coupling capacitor ensures independent and robust dc biasing of the LNTA and baseband amplifier and blocking of second-order intermodulation products created by LNTA. It is realized using alternative polarity metal oxide metal capacitor to reduce parasitic capacitances at the RF node. DC-level shifting (not shown in Fig. 5) is applied for the LO signals to

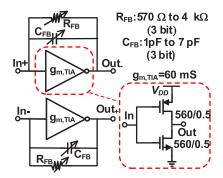


Fig. 6. Implementation of TIA circuit using an inverter amplifier.

maximize drive voltage for mixer switches. The ON-resistance of the reconfiguration switches is designed to be lower than that of the mixer switches because they do not contribute to dynamic power consumption and their parasitic capacitances are absorbed in the baseband capacitors, thereby not affecting high-speed RF performance of the receiver.

B. TIA Circuit

The TIA is implemented using self-biased inverter amplifiers employing transistors with large channel lengths $(L = 0.5 \ \mu \text{m})$ to achieve high open-loop gain and low flicker noise. Both the feedback resistor and capacitor of the TIA are implemented in a programmable way with 3-bit digital control to provide a variable gain and baseband bandwidth for the receiver (Fig. 6).

IV. CIRCUIT ANALYSIS

In this section, a brief analysis is provided for key performance parameters of the proposed front end, including RF bandwidth extension, conversion gain, input matching, noise, and linearity performance.

A. RF Frequency Range Extension

As mentioned in Section II, the conventional constant-Gm VM with charge-sharing on a baseband output capacitor [8] [Fig. 7(a)] poses a limitation in RF frequency range, i.e., in-band gain reduction at high RF/LO frequencies. The proposed VM with current summing at the input of the TIA offers wider RF frequency range [Fig. 7(b)]. We will show this by estimating the pole at the LNTA output caused by parasitic capacitance to ground (C_P) and resistance seen in this node for both scenarios. In Fig. 7(a), the four-phase passive mixer operates in voltage mode. Based on the theory in [27], i.e., $R_{in,mixer} = R_{sh} \approx 4.3R_{out}$, where R_{out} is the output resistance of the LNTA. Then, the 3-dB RF cutoff frequency can be found as

$$f_{-3\,\mathrm{dB,RF}} = \frac{1}{2\pi \left(R_{\mathrm{out}} \| R_{\mathrm{in,mixer}}\right) C_P} \approx \frac{1}{2\pi R_{\mathrm{out}} C_P}$$
(1)

In our design the values of R_{out} and C_P are about 3 k Ω and 20 fF, respectively. Therefore, the maximum achievable RF operating frequency would be limited to 2.7 GHz if charge sharing on a capacitor were to be used. As explained in [28], the capacitance to ground at the RF input of an *N*-path

mixer can have rather complicated effects. According to [28], C_P affects the unconverted harmonics of the signal, resulting in a reduction of R_{sh} , which reduces in-band gain at high RF/LO frequencies. However, for our circuit, the upconverted baseband impedance is much lower than R_{sh} and the pole frequency at the mixer RF port gives an upper limit for the RF/LO frequency at which 3-dB gain reduction occurs. For the proposed VM with current summing [Fig. 7(b)], the TIA provides a low input impedance (R_{BB}) that is translated to the RF domain as well. Therefore, if R_{sh} is neglected, the impedance seen at the mixer input is

$$R_{\rm in,mixer} \approx R_{sw} + \gamma_4 N M R_{\rm BB}$$
 (2)

$$R_{\rm BB} = \frac{1}{g_{m,\rm TIA}} + \frac{R_{\rm FB}}{1 + A_{v,\rm TIA}} \tag{3}$$

where $\gamma_4 = 2/\pi^2$ for a 4-phase passive mixer [27]. γ_4 is related to 4 phases in the passive mixer; therefore, it does not change with the number of antenna elements *N*. $A_{v,TIA}$ is the open-loop gain of the TIA amplifier. R_{BB} in (2) is scaled by *NM* because the TIA is shared between *N* VMs each one having *M* number of slices that add their currents to the TIA input, thus increasing the voltage swing at both the RF and baseband nodes of the mixer. The value of $R_{in,mixer}$ is designed to be less than that of R_{out} , and thus, it dominates the parallel combination of the two resistances, resulting in an RF frequency pole at

$$f_{-3\,\mathrm{dB,RF}} = \frac{1}{2\pi \left(R_{\mathrm{out}} \| R_{\mathrm{in,mixer}}\right)C_P} \approx \frac{1}{2\pi R_{\mathrm{in,mixer}}C_P}.$$
 (4)

With the design parameters, e.g., $R_{sw} = 150 \ \Omega$, $R_{FB} = 2 \ k\Omega$, $A_{v,TIA} = 300 \ V/V$, M = 15, N = 4, and $g_{m,TIA} = 60 \ mS$, the frequency pole $f_{-3 \ dB,RF}$ can be extended up to 18 GHz. Circuit simulations with ideal LO clock signals show that the 3-dB in-band gain reduction due to C_P occurs at 13.5 GHz, which is close to the estimated value of the pole frequency. Note that the achievable RF frequency range in practice would be limited by other factors, such as the limited rise and fall times of mixer clock edges. However, the resulting limitation due to the charge sharing is resolved to a sufficient degree to allow for operation up to 6 GHz. If more antenna elements are used, e.g., an 8- or 16-element array, the RF frequency range still can be improved; however, it requires lower R_{BB} values because R_{BB} in (2) scales with the number of antenna elements N and the number of slices M.

B. Conversion Gain

As shown in Fig. 7(b), the LNTA converts the RF input voltage to a current, i.e., $i_{RF} = g_m V_{in,RF}$. Assuming that $R_{in,mixer} \ll R_{out}$, this current is down converted to the baseband by the 25% duty cycle passive mixer $[i_{BB} = 1/4 \text{sinc}(1/4)i_{RF}]$. The TIA sums up all the baseband currents from VM slices after which I-V conversion across the shunt feedback resistor R_{FB} results in a voltage swing on the baseband output. Therefore, if all the currents are in-phase, i.e., the constellation corners, the differential voltage gain of one VM element can be found

$$A_{\nu,\text{diff}} = \frac{1}{2} \cdot \text{sinc}\left(\frac{1}{4}\right) \cdot M \cdot g_m \cdot R_{\text{FB}} \cdot \tag{5}$$

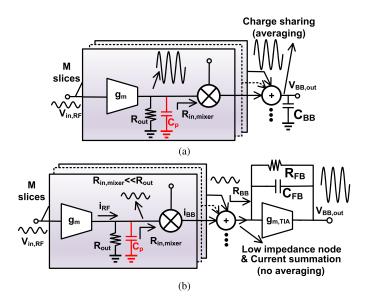


Fig. 7. (a) Constant-Gm VM with averaging by charge sharing results in high impedance node at the LNTA output, and therefore, limited RF bandwidth [8]. (b) In the proposed constant-Gm VM with current summing, the RF pole is pushed to higher frequencies by a low-input impedance provided by the TIA.

With current summing, the voltage gain scales with the number of slices M as indicated in (5), whereas in the VM of Fig. 7(a), the limited intrinsic gain of the LNTA determines the output voltage swing that does not change with the number of slices due to the averaging by charge sharing. Moreover, variable gain control can be realized by a digitally controlled $R_{\rm FB}$.

C. Input Matching

Simple inverter-based LNTAs with shunt feedback resistors are used to provide low-noise input matching for the RF inputs. Each antenna is connected to four VMs, where each VM has M slices. Each segmented VM having M slices gives an input impedance that is determined by the "Miller"effect as

$$R_{\mathrm{in},\mathrm{VM}_i} = \frac{1}{M} \left(\frac{R_F + R_{L,i}}{1 + g_m R_{L,i}} \right) \approx \frac{1}{M} \left(\frac{R_F}{1 + g_m R_{L,i}} \right) \tag{6}$$

where i = 1, 2, ..., 4 and g_m is transconductance of each LNTA slice and $R_{L,i}$ are load resistors of LNTA slices for corresponding VMs [see Fig. 8(a)]. It is assumed that $R_F \gg R_{L,i}$ and the slices of each VM are in-phase, i.e., constellation corners. Neglecting the drain-source output resistance of the LNTA transistors, $R_{L,i}$ are equal to the input impedance of the mixers. Employing an ideal TIA with very small input impedance, each LNTA is only loaded by the ON-resistance of the mixer switch. However, with a nonideal TIA having a finite-input impedance, $R_{L,i}$ also depends on the spatial pattern at the TIA inputs. Hence, the input impedance of the VMs varies, accordingly. Actually, the input impedance of the VMs appears to be different for correlated signal than for uncorrelated noise. As we need both values to do beamforming gain calculations on the one hand and noise calculations on the other, we will obtain the input impedance in these example scenarios.

Consider the first scenario with correlated signals, as shown in Fig. 8(a), when four orthogonal beams are formed. As the

loading impedance of LNTAs depends on the spatial pattern, for the VM looking into the main beam direction, the LNTAs are loaded with R_{sw} in series with the effectively translated baseband impedance ($\gamma_4 4 \ MR_{BB}$). For the other orthogonal beams nulling occurs (i.e., zero TIA-input currents) and the effect of impedance translation is negligible; therefore, only R_{sw} remains. The input impedance of each VM can be found using (6) by substituting the appropriate load impedance for each case and calculating the equivalent impedance of four parallel VMs gives the input impedance for the receiver. Doing this results in the following expression:

$$R_{\rm in} \approx \frac{1}{4M} \frac{R_F}{1 + g_m (R_{sw} + \gamma_4 M R_{\rm BB}).}$$
(7)

Note that this input impedance does not depend on the direction unlike the passive beamforming in [5] that provide a low input impedance in the notch direction not matched to 50 Ω load. Note that if a voltage notch at the LNTA output degrades the input matching, this might affect the functionality of a preceding band selection filter. Or unlike notching with baseband impedance synthesis in [14], where the input impedance is higher in the notch direction, potentially degrading interference robustness of the receiver.

In the second scenario, only one input source is excited, while the other inputs are resistively terminated by the source impedance (50 Ω here) to model the circuit behavior for uncorrelated input signals, e.g., added noise by each antenna, where the coherent addition of signals from different VM elements does not exist. Fig. 8(b) shows the equivalent receiver circuit model in which all the LNTAs see the same load of R_{sw} in series with $\gamma_4 M R_{BB}$. Note that in this scenario, the baseband impedance (R_{BB}) only scales by the number of slices. Therefore, the input impedance is equal to the parallel combination of four equal impedances given by (6), which results readily in the same expression as in (7). Interestingly, both scenarios give the same input impedance. This is because the parallel admittances are simply added to obtain the equivalent admittance, and here, the total sum of the LNTA loads are equal for both scenarios, although the individual VMs contribute differently to the input impedance. It can be shown this is also true for the cases in between the two extremes analyzed here. We have verified these results by simulations using a macromodel and circuit implementation.

D. Noise Performance

To comply with the NF definition in [29] often single-element NF is used to evaluate the noise performance of phased-array receivers. Here, we will obtain the single-element noise factor of the proposed beamforming receiver that is defined as the ratio of the total output noise power from one receiver element to the output noise power caused by the source, i.e., antenna noise [29]. To this end, a simplified noise model of one receiver element is shown in Fig. 9. We only take into account the dominant noise contributors, i.e., thermal channel noise of LNTA transconductance, modeled by a current noise $\overline{I_{n,gm}^2} = 4kT\gamma g_m$ for each slice in Fig. 9, and thermal noise of shunt-feedback resistors ($\overline{V_{n,R_F}^2} = 4kTR_F$), GOLABIGHEZELAHMAD et al.: 0.7-5.7 GHz RECONFIGURABLE MIMO RECEIVER ARCHITECTURE

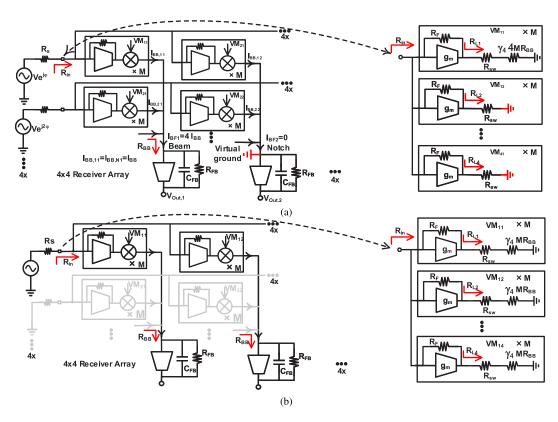


Fig. 8. Equivalent Circuit model of the input impedance in case of: (a) correlated signals assuming four orthogonal beams; (b) uncorrelated input signals (exciting one RF input and terminating the others). Differential I/Q outputs are not shown for simplicity.

neglecting the noise caused by the TIA and mixer switches. R_{in} in Fig. 9 is the input impedance of the receiver and can be calculated from (7). Although bondwire inductance together with the parasitic input capacitance makes a low-pass filter in the RF input, for simplicity we do not include its effect in our analysis.

The receiver's NF also depends on the VM setting because it affects conversion gain but not the uncorrelated added noise of VM slices. To account for this dependence, we define parameter α as the normalized gain of complex constellation points relative to that of the corner point (see Fig. 9). This means that when the VM is set to the corner points $\alpha = 1$, and its value is less than one for the other points. More specifically, α is approximately equal to $1/\sqrt{2}$ for the points near the biggest circle fitting into the constellation square.

Following the above-mentioned assumptions, the singleelement noise factor can be obtained as:

$$F = \left(1 + 3M\frac{R_s}{R_F} + \frac{1}{\alpha^2} \left(\frac{R_s + R_{\rm in}}{R_{\rm in}}\right)^2 \\ \cdot \left(\frac{\gamma}{Mg_m R_s} + \frac{\left(1 + Mg_m \frac{R_s R_{\rm in}}{R_s + R_{\rm in}}\right)^2}{Mg_m^2 R_F R_s}\right) \right) \frac{1}{{\rm sinc}^2(\frac{1}{4})}.$$
 (8)

The $3MR_S/R_F$ term in (8) is contributed by shunt-feedback resistors in VM₂, VM₃, and VM₄ (see Fig. 9) that induce noise current into the input node, which appears at the output of element 1 as well. However, this term will only slightly degrade the NF if a large value is chosen for R_F . Due to the low input impedance of the mixers (R_L s in Fig. 9) and

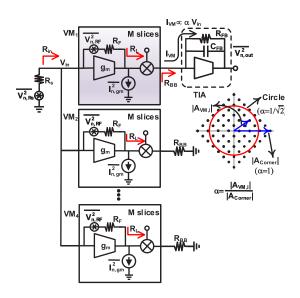


Fig. 9. Single-element noise model of the receiver. For the sake of simplicity, only dominant noise contributors are considered.

 $R_F \gg R_s$, the contribution of the g_m current noises in VM₂, VM₃, and VM₄ is negligible; therefore, it is not included in (8). The remaining terms are contributions of VM₁, scaled by factor $1/\alpha^2$ that represent signal loss due to the VM setting, thereby degrading the NF when moving toward the constellation center. As a result, the best NF can be achieved at the constellation corner where the gain is maximum, i.e., $\alpha = 1$. The $1/\text{sinc}^2(1/4)$ term in (8) accounts for harmonic folding noise of a 4-phase passive mixer [26], which adds extra 0.9 dB to the receiver's NF. Using design parameters: $g_m = 4.2$ mS, $R_F = 10 \text{ k}\Omega$, $R_s = 50 \Omega$, and $R_{\text{in}} = 86 \Omega$ from (7), and assuming $\gamma = 2/3$ (i.e., long channel assumption for CMOS transistors), (8) indicates that a single-element NF of about 3.7 dB can be achieved in the constellation corner, while it degrades to 5.0 dB on the circle points. Note, however, that system NF benefits from noise averaging for MIMO, bringing up to 6-dB NF improvement for 4 elements.

The LNTA's in a single-beam 4×1 array [8] provide higher voltage gain (capacitive output) than the LNTAs terminated with TIAs in this work. This makes some differences in the impedance matching. In a 4×4 array, we need much larger feedback resistors across LNTAs to meet 50 Ω input matching for more parallel receivers. This is beneficial from a noise perspective because the higher resistors will contribute less to the NF. In addition, in a 4×4 MIMO array, R_F s from other VMs, e.g., VM₂, VM₃, and VM₄ connected to the input slightly contribute to NF in VM₁ path as explained earlier. Overall, there is no significant difference in the NF performance between 4×1 and 4×4 implementations. Connecting four times the number of circuits to the input clearly increases the parasitic input capacitance that degrades the input matching at higher frequencies. However, process scaling helps to reduce this parasitic capacitance, improving the input matching at higher RF frequencies.

E. Linearity and Blocker Tolerance

The linearity of a beamforming receiver depends on the angle between interferers and the desired signal as was studied in [8]. We will now provide some insight into achievable linearity performance of the proposed receiver. For a simple scenario in which a two-tone interferer and the desired signal are both in the main beam direction, it is likely that the last stage, i.e., the TIA limits distortion level at the output. Because of the negative feedback loop and the fact that an inverter-based TIA amplifier can provide full swing, a high OIP3 can be achieved. When the two-tone interferer arrives from the notch direction but the desired signal from the main beam angle, if the beamformer is configured to direct a null to the two-tone interferer, the third-order intermodulation (IM3) components created by the nonlinear LNTAs is rejected by the spatial notch as well. Note that the TIA processes the interferer residue after spatial filtering occurs; therefore, not only the ADC dynamic range but also the TIA dynamic range is relaxed. Hence, LNTA nonlinearity, rather than TIA nonlinearity, tends to dominate distortion. Because with every 2-dB improvement in IM3, IIP3 improves by 1 dB and the LNTA IIP3 improves by half of the notch depth; e.g., supposing an IIP3 of +5 dBm for the LNTA and a null depth of 29 dB, in-notch IIP3 of 5 + 29/2 = +19.5 dBm is expected for the receiver.

An interference nulling receiver has to handle a large co-channel blocker. Therefore, the blocker input power level at which the small-signal gain reduces by 1 dB (B1dB) is of interest. As nulling relaxes the dynamic range of the TIA, again the LNTA tends to limit maximum achievable B1dB.

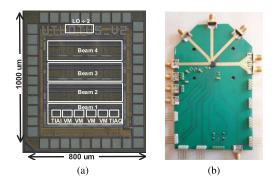


Fig. 10. (a) Die micrograph. (b) Test PCB with mounted QFN package.

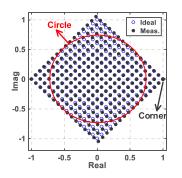


Fig. 11. Measured constellation diagram.

For $g_m = 4.2$ mS and $R_{sw} = 150 \ \Omega$ simulation of the simple LNTA circuit shows B1dB of -6.5 dBm. Although B1dB could be pushed as high as -3.5 dBm choosing a low-ohmic mixer switch, e.g., $R_{sw} = 10 \ \Omega$ for a unit slice, this would result in a drastically increased dynamic LO power consumption, and therefore, was not pursued.

V. EXPERIMENTAL RESULTS

A prototype chip was fabricated in GlobalFoundries 22-nm FD-SOI technology. Fig. 10(a) shows the chip micrograph. The active area of chip is 0.52 mm² and a 40-pin QFN package mounted on a four layer PCB, as shown in Fig. 10(b), was used. Four RF transmission lines on the PCB were designed with equal lengths to minimize phase errors. An external high impedance differential active probe (Lecroy AP033) was used to sense the baseband outputs of the chip.

A. Vector Modulator and Spatial Patterns

The gain and phase accuracy of the implemented VMs is demonstrated with a constellation diagram shown in Fig. 11. The constellation was measured with a vector network analyzer (VNA) using a single-tone RF input at LO frequency of 2.5 GHz and compared with an ideal 16×16 square equidistance constellation. An rms phase error of 1.3° and rms gain error of 0.28 dB was achieved, demonstrating a close to the ideal constellation. The points with equal weights but variable phase nearby the biggest circle fitting into the square constellation are used to create orthogonal beams at arbitrary directions. To measure beam patterns, a four-element antenna array with uniform half-wavelength spacing is emulated using

GOLABIGHEZELAHMAD et al.: 0.7-5.7 GHz RECONFIGURABLE MIMO RECEIVER ARCHITECTURE

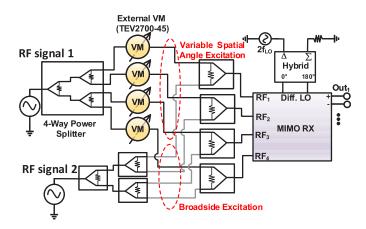


Fig. 12. Block diagram of the four-element phased-array antenna emulation system. Two antenna signals can be emulated one with variable spatial angle and the second one with broadside excitation.

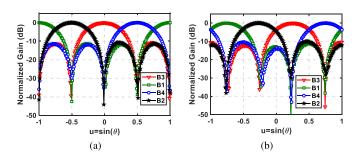


Fig. 13. (a) Measured orthogonal beam patterns @ $f_{LO} = 2.5$ GHz with a notch at u = 0. (b) Shifted pattern patterns with a notch at u = 0.25.

a commercial four-way power splitter and four external VMs (TEV2700-45), as shown in Fig. 12. For calibration of the antenna emulation system, first, we have measured complex gains using a VNA across settings of the external VM for four RF paths. Then, we find close to ideal points on a constant gain circle from 1° to 360°. Later, these data are used during measurements using a lookup table to relate the ideal phases to closest settings. This results in a gain and phase errors of less than 0.2 dB and 1.5°, respectively, for all of the four paths across 360° phase points. Therefore, the low gain and phase errors of the measurement set up are sufficient to measure the targeted null depth of about 30 dB. Fig. 13(a) shows an example of orthogonal beam patterns targeting a notch at broadside $(u = \sin(0^\circ) = 0)$ with $f_{LO} = 2.5$ GHz at 10-MHz baseband. It is seen that a null depth of greater than 29 dB is achieved. Fig. 13(a) looks similar to what a Butler matrix would provide. However, unlike a Butler matrix with hybrids, here we can flexibly shift the entire pattern, as exemplified in the shifted pattern (u = 0.25) in Fig. 13(b).

To evaluate the notch suppression bandwidth, a notch is formed at broadside, and the RF frequency is swept at a fixed LO frequency of 2.5 GHz. A 0.25–6-GHz 4-way power splitter with low amplitude and phase imbalances (ZN4PD1-63HP+) is utilized to emulate antenna signals arriving from broadside across wide RF frequency range. As shown in Fig. 14(a), 20-dB notch suppression bandwidth is about 2.3 GHz. This wideband suppression is possible

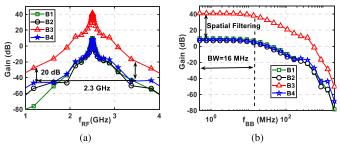


Fig. 14. 20-dB notch suppression bandwidth at broadside (a) Gain versus RF frequency (b) versus baseband frequency, f_{BB} .

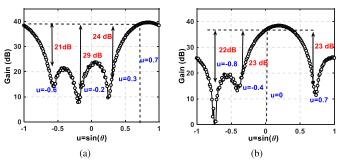


Fig. 15. (a) Example of synthesized beam pattern targeting the desired signal at u = 0.7 and three independent nulls at the specified angles. (b) Another example with the desired signal at u = 0 and other three nulls.

due to the early current-domain beamforming in the receiver, immediately after voltage-to-current conversion by the LNTA and high-linearity current-domain-routing by mixer and reconfiguration switches. Fig. 14(b) shows the same plots as in Fig. 14(a), but the x-axis represents baseband frequency (f_{BB}) in logarithmic scale for demonstrating low-pass filtering at the baseband output (BW = 16 MHz). Feedback resistor around TIA $(R_{\rm FB})$ affects gain; therefore, with higher bandwidth, there would be less gain. We have chosen to have a higher gain to show the merits of our receiver better from a linearity perspective. Choosing $R_{\rm FB} = 2$ kohm, $C_{\rm FB} = 3$ pF results in 41-dB gain and 16-MHz bandwidth. There is some parasitic capacitance around the TIA amplifier (about 2 pF); therefore, total feedback capacitance across the TIA amplifier is more than $C_{\rm FB}$. Maximum measured bandwidth of about 100 MHz is obtained in practice.

Given that the constant-Gm VM provides both phase and amplitude control, more complex beam patterns with several deep notches can be synthesized using a weight synthesis method to cancel multiple interferers simultaneously. For our four-element array system, up to three independent nulls can be created. Two arbitrary examples of resulting spatial patterns with the main beam pointing to the one desired signal direction and three nulls are demonstrated in Fig. 15(a) and (b). A null depth of more than 21 dB is achieved in both examples.

B. Gain, S_{11} , and NF

Fig. 16(a) and (b) demonstrates widely tunable RFperformance of the chip, by plotting total gain and S11. A 1-MHz IF-tone was used, and the LO frequency was

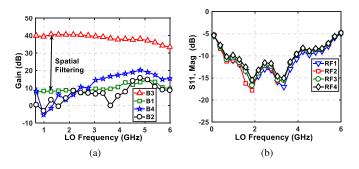


Fig. 16. (a) Total conversion Gain and (b) S_{11} across LO frequency.

swept. The total gain is measured using the same wideband four-way splitter as in notch bandwidth test, emulating broadside excitation. The plot in Fig. 16(a) also shows wideband spatial filtering (note the difference with Fig. 14(a), where RF frequency is swept and LO is fixed, i.e., variable IF-frequency, while here RF and LO are swept together, i.e., fixed IF-frequency). Equivalent single-element double sideband NF (NF_{DSB,eq}) versus LO frequency on the constellation corner is shown in Fig. 17(a). NF DSB,eq of 6-8.8 dB at broadside (u = 0) is measured using the single-excitement method introduced by [12] and [14], improving the noise performance up to 2.4 dB compared with the earlier design in [21]. This improvement is achieved by redesigning the LNTAs, i.e., higher g_m and slightly higher feedback resistance $(R_F \text{ in Fig. 5})$, resulting in an only 6-mW increase in the power consumption. The NF varies to some extent depending on the beam direction, which is mainly due to the gain variations as a result of interaction between RF channels. The noise performance degradation at the low LO frequencies arises from ac coupling capacitors at the LNTA outputs, while the degradation at higher LO frequency most likely is caused by degradation in LO clock signals. The NF is also measured on the biggest circle fitting into the square constellation where the signal gain is reduced, but analog beams and notches can be steered to arbitrary direction, hence degrading the NF by about 2 dB [see Fig. 17(b)]. The best achievable system NF, hence, occurs in the corner points (providing analog beams at u = 0, u = 1/2, u = -1/2, u = 1 and digital beamforming can be performed later at the arbitrary direction in the digital domain). When applying digital processing, taking into account the SNR improvement by up to 6 dB, a sub-3-dB system NF can potentially be obtained. Although the NF degrades by moving to circle points, linearity improves much more, i.e., spuriousfree dynamic range benefits. Fig. 18 shows the measured NF versus baseband frequency at $f_{LO} = 2.5$ GHz. The flicker noise corner is less than 100 kHz.

C. IIP3 and B1dB

The in-beam/in-notch IIP3 versus offset frequency at $f_{\rm LO} = 2.5$ GHz and the bandwidth of about 16 MHz is plotted in Fig. 19(a). The results show +2-dBm out-of-band linearity in the main beam direction, limited by the linearity of the LNTA. At very low offset frequencies, in-band IIP3 of -13 dBm and -19 dBm is measured at a total

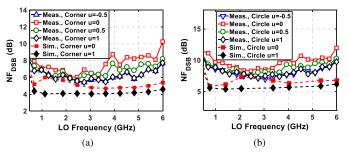


Fig. 17. (a) Measured and simulated $NF_{DSB,eq}$ across LO frequency at the constellation corner and (b) $NF_{DSB,eq}$ on the circle points.

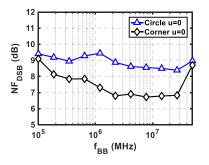


Fig. 18. Measured NF_{DSB,eq} versus f_{BB} at $f_{LO} = 2.5$ GHz.

gain of 35 and 41 dB, respectively, corresponding to OIP3 of +22 dBm independent of the gain. To evaluate in-notch IIP3, it is assumed that two-tone interferers arriving at the notch direction have spatial separation from the desired signal angle-of-arrival, e.g., main beam direction. Since the intermodulation product produced by the LNTA is suppressed by the notch filtering, the in-notch IIP3 is improved from +2 to +20 dBm (at a 35-dB gain) as predicated in Section IV and it degrades to +16 dBm at a 41-dB gain as the nonlinearity of the TIA also starts playing a role at higher gains. This IIP3 remains approximately constant across the offset frequency, which fits the wide 20-dB rejection bandwidth observed in Fig. 14(a). Out-of-band linearity (at an offset frequency of about 500 MHz) versus LO frequency is shown in Fig. 19(b). OOB IIP3 improves up to +6.3 dBm as the LO frequency increases due to reduced LNTA gain because of the lower ac coupling capacitor impedance at higher frequencies. Fig. 20 shows the conversion gain for the desired signal in terms of co-channel, in-beam/in-notch blocker power level; putting a notch at the blocker's angle improves the blocker tolerance about 27 dB, achieving a high B1dB of -11.5 dBm.

D. Performance Comparison

Table I summarizes the performance of the chip and benchmarks it with the state-of-the-art. The receiver is widely tunable, supporting the sub-6-GHz bands. The in-beam OIP3 and in-notch IIP3 values are the highest among MIMO receivers. Moreover, in-notch B1dB of -11.5 dBm at a 41-dB gain is the best achieved blocker tolerance for MIMO receivers. Taking into account 6-dB SNR improvement due to the analog beamforming, the receiver can potentially achieve sub-3-dB NF. The noise performance is slightly worse than digital MIMO chips GOLABIGHEZELAHMAD et al.: 0.7-5.7 GHz RECONFIGURABLE MIMO RECEIVER ARCHITECTURE

Architecture	ISSCC'13 [5]	JSSC'17 [8]	RFIC'16 [11]	ISSCC'16 [12]	ISSCC'17 [14]	This work RFIC'19 [21]	This work
Process	65 nm	65 nm	65 nm	65 nm	65 nm	22 nm FD-SOI	22 nm FD-SOI
Active area (mm ²)	0.97	0.2	3.8	1.69	1.44	0.52	0.52
Supply (V)	1.2	1	1.3-1.5	1.2	1.2	0.8	0.8
Array elements	4x1 MISO	4x1 MISO	4x4 MIMO	4x4 MIMO	4x4 MIMO	4x4 MIMO	4x4 MIMO
RF Frequency (GHz)	0.6-3.6	1-2.5	10	0.1-1.7	0.1-3.1	1-4	0.7-5.7
Total Gain (dB)	-1	12	14	41	43	44.5	41
Single Element NF _{DSB,eq} (dB)	5-8	6	9.5	2.2-4.6	3.4-5.8	$10.9-11.6^{1}$ 8.4-9.5 ²	$\begin{array}{rrrr} 8.3\text{-}11.1^1 & 6.8\text{-}9.2^3 \\ 6\text{-}8.8^2 & 5.5\text{-}7^4 \end{array}$
20 dB Spatial Suppres- sion Bandwidth (MHz)	-	-	100 (1%)	15 (3%)	320 @ 500 MHz (64%)	2000 @ 2.5 GHz (80%)	2300 @ 2.5 GHz (92%)
In-band/in-beam OIP3(dBm)	-	13	-	0	+11	+18.5	+22
In-band/in-notch IIP3(dBm)	+9	+20	-	-7	+1	+17	$+20^{5}$ +16 ⁶
Out-of-band IIP3 (dBm)	+20	+5	-	+11	-5	+3	+0.5+6.3
In-notch B1dB (dBm)	-	-	-	-	-25	-12	-11.5
Power (4 Elements, mW)	66-195 40 mW+43 mW/GHz	26-36 19mW+6.7 mW/GHz	145 (1 Elem.)	148 @ 0.5 GHz	116-147 115mW+10 mW/GHz	75-115 62mW+13.2 mW/GHz	77-139 68mW+12.4 mW/GHz

TABLE I Performance Summary and Comparison With State-of-the-Art

¹ On the circle and broadside (u=0) ² On the corner broadside(u=0) ³ On the circle and endfire (u=1) ⁴ On the corner and endfire (u=1) ⁵ total gain of 35 dB ⁶ total gain of 41 dB

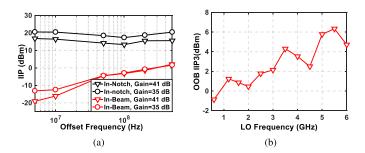


Fig. 19. (a) In-beam/in-notch IIP3 as function of offset frequency of first tone. (b) Out-of-band IIP3 versus LO frequency.

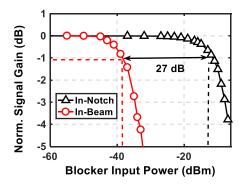


Fig. 20. Conversion gain for desired signal versus co-channel, in-beam/innotch blocker input power.

presented in [12] and [14], but this is compensated by very significant improvements in linearity. The chip consumes 77–139 mW at LO frequency of 0.7–5.7 GHz, operating at faster clock speed compared with the prior art (about $1.8 \times$), demonstrating a power-efficient circuit implementation. With

regard to [21] that consumes 75–115 mW at LO frequency of 1–4 GHz, the static power consumption is slightly increased due to modifications in LNTAs design (about 6 mW more) and the increase in the higher end is related to the faster clock frequency of 5.7 GHz instead of 4 GHz in [21].

E. EVM Measurements

Measurements were performed to show the effectiveness of spatial filtering using EVM as in [30]. To this end, setup in Fig. 12 was used, where the differential receiver output is sensed using an active probe and applied to a Keysight N9030A PXA signal analyzer for digital demodulation by VSA software. To simplify the measurements, only the I-output was used. A 10-MSymbols/s 256-QAM desired signal with -50-dBm power level was generated at $f_{\rm RF} = 2.47$ GHz. A root raised cosine pulse shaping filter with $\beta = 0.35$ was applied; therefore, the bandwidth of the modulated signal is about 13.5 MHz. The baseband bandwidth of the chip was set to 28 MHz for this experiment. A 5-dB weaker modulated interferer is having the same specifications as the desired signal was also generated. The desired signal is arriving from the broadside, while the angle-of-arrival for the interferer can be swept. If the interferer is applied from the same angle as the desired signal, e.g., broadside, digital demodulation fails, as shown in Fig. 21(a). However, if the interferer angle-ofarrival set to be at the notch angle of $+30^{\circ}$, the desired signal can be successfully demodulated, and an EVM of 2.0% is achieved.

Another EVM measurement was performed, while the TIA bandwidth was set to its maximum of about 100 MHz. For this experiment, a 50-MSymbols/s 16-QAM desired signal with input power level of -50 dBm was generated at the center

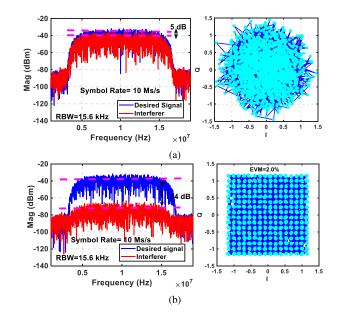


Fig. 21. (a) Output spectrum and constellation when a modulated desired signal and a 5-dB weaker interferer are both arriving from broadside (no spatial filtering). (b) Output spectrum and constellation when the desired signal is arriving from broadside and the interferer from a null angle at 30° (spatial filtering).

RF frequency $f_{\rm RF} = 2.512$ GHz ($f_{\rm BB} = 52$ MHz). A root raised cosine pulse shaping filter with $\beta = 1$ was applied; therefore, the bandwidth of the modulated signal is about 100 MHz. A 5-dB stronger modulated interferer is having the same specifications as the desired signal was also generated. Output spectrum and constellation with no spatial filtering and after spatial filtering have been shown in Fig. 22(a) and (b), respectively. Digital demodulation fails in the presence of a 5-dB stronger interferer when there is no spatial filtering. However, after 27-dB interference rejection, an EVM of 8.9 % is achieved (EVM = -21 dB), which approximately fits to the 22-dB signal-to-interference ratio after spatial filtering. This experiment verifies the wideband spatial interference rejection capabilities of the receiver.

Over-the-air measurements were done using a 4-element dipole antenna array with half-wavelength spacing in the 2.4-GHz ISM-band, and one dipole antennas for transmitting the desired signal and one antenna for the interferer in the laboratory environment. First, EVM is measured when a 1-MSymbols/s 256-QAM desired signal with -50-dBm input power level and a 20-dB weaker interferer signal having the same modulation specifications as the desired signal are combined and radiated over-the-air at 2.47 GHz with one antenna placed at broadside. This makes sure that both the interferer and the desired signal propagate to the receiver antenna array within the same propagation channel. As shown in Fig. 23(a), digital demodulation has failed. Finally, the interferer again at the same power level as before is transmitted using the second transmit-antenna placed at $+30^{\circ}$ for spatial filtering/separation, after which successful demodulation becomes possible, and an EVM of 1.6% is obtained, as shown in Fig. 23(b). With the over-the-air experiment, spatial filtering of 15 dB is obtained, which is less than that of the conductive

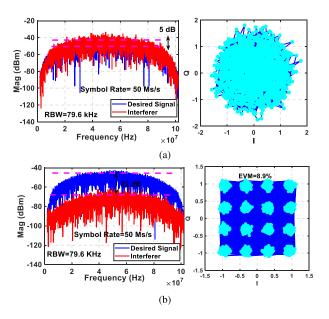


Fig. 22. (a) Output spectrum and constellation when a 50-MSymbols/s 16-QAM desired signal and a 5-dB stronger interferer are both arriving from broadside (no spatial filtering). (b) Output spectrum and constellation when the desired signal is arriving from broadside and the interferer from a null angle at 30° (spatial filtering). For this experiment, a root raised cosine pulse shaping filter with $\beta = 1$ was used; therefore, the modulated signal bandwidth was about 100 MHz.

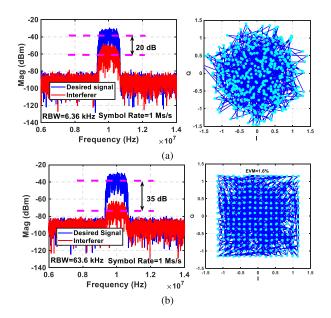


Fig. 23. (a) Over-the-air measured output spectrum and constellation when a modulated desired signal and a 20-dB weaker interferer are both arriving from broadside (no spatial filtering). (b) Output spectrum and constellation when the desired signal is arriving from broadside and the interferer from a null angle at 30° (spatial filtering).

measurements because there are variations in the received power at individual antenna array elements possibly due to multipath propagation and mutual coupling between antenna elements; therefore, the results depend on the measurement setup. However, it is expected that better results become possible utilizing an adaptive spatial filtering solution. We have verified this by manually adapting the beamformer settings. To do so, first, the individual antenna signals received from the interferer transmit antenna were measured. These data are used to compensate the amplitude and phase variations relative to expected ideal line-of-sight antenna signals at 30° by adapting the beamformer weights. This improves the rejection amount to 24 dB.

VI. CONCLUSION

In this article, a highly flexible and reconfigurable MIMO receiver was presented for spatial co-channel blocker rejection. The receiver is tunable up to 6 GHz, supporting sub-6-GHz bands. The main focus of this work is on reconfigurable interference notching MIMO front end to relax the dynamic range of the baseband amplifier and ADCs. Interference suppression early in the receiver chain before voltage amplification improves linearity performance and notch suppression bandwidth. An in-notch IIP3 of +20 and +16 dBm at total gain 35 and 41 dB, respectively, and a highly blocker tolerant performance with B1dB of -11.5 dBm at 41 dB gain are achieved.

ACKNOWLEDGMENT

The authors would like to thank Gerard Wienk for CAD assistance and Arnoud Rop for measurement setup. The authors also thank GlobalFoundries for supporting chip fabrication.

REFERENCES

- J. Mitola and G. Q. Maguire, "Cognitive radio: Making software radios more personal," *IEEE Pers. Commun.*, vol. 6, no. 4, pp. 13–18, Aug. 1999.
- [2] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, "A 1.4 V 5 GHz four-antenna Cartesian-combining receiver in 90 nm CMOS for beamforming and spatial diversity applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 1, Feb. 2005, pp. 210–594.
- [3] R. Tseng, H. Li, D. H. Kwon, Y. Chiu, and A. S. Y. Poon, "A four-channel beamforming down-converter in 90-nm CMOS utilizing phase-oversampling," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2262–2272, Nov. 2010.
- [4] M. C. M. Soer, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, "A 1.0-to-4.0 GHz 65 nm CMOS four-element beamforming receiver using a switched-capacitor vector modulator with approximate sine weighting via charge redistribution," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 64–66.
- [5] A. Ghaffari, E. E. A. M. Klumperink, F. van Vliet, and B. Nauta, "Simultaneous spatial and frequency-domain filtering at the antenna inputs achieving up to +10dBm out-of-band/beam P1dB," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 84–85.
- [6] M. C. M. Soer, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, "1.0-to-2.5 GHz beamforming receiver with constant- G_m vector modulator consuming < 9mW per antenna element in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 66–67.
- [7] S. K. Garakoui, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, "Compact cascadable g m-C all-pass true time delay cell with reduced delay variation over frequency," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 693–703, Mar. 2015.
- [8] M. C. M. Soer, E. A. M. Klumperink, D.-J. van den Broek, B. Nauta, and F. E. van Vliet, "Beamformer with constant-gm vector modulators and its spatial intermodulation distortion," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 735–746, Mar. 2017.
- [9] A. J. Paulraj, D. A. Gore, R. U. Nabar, and H. Bolcskei, "An overview of MIMO communications—A key to gigabit wireless," *Proc. IEEE*, vol. 92, no. 2, pp. 198–218, Feb. 2004.

- [10] J. H. C. van den Heuvel, J.-P.-M. G. Linnartz, P. G. M. Baltus, and D. Cabric, "Full MIMO spatial filtering approach for dynamic range reduction in wideband cognitive radios," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 11, pp. 2761–2773, Nov. 2012.
- [11] S. Jain, Y. Wang, and A. Natarajan, "A 10 GHz CMOS RX frontend with spatial cancellation of co-channel interferers for MIMO/digital beamforming arrays," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, May 2016, pp. 99–102.
- [12] L. Zhang, A. Natarajan, and H. Krishnaswamy, "A scalable 0.1-to-1.7 GHz spatio-spectral-filtering 4-element MIMO receiver array with spatial notch suppression enabling digital beamforming," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Jan. 2016, pp. 166–167.
- [13] H. Krishnaswamy and L. Zhang, "Analog and RF interference mitigation for integrated MIMO receiver arrays," *Proc. IEEE*, vol. 104, no. 3, pp. 561–575, Mar. 2016.
- [14] L. Zhang and H. Krishnaswamy, "A 0.1-to-3.1 GHz 4-element MIMO receiver array supporting analog/RF arbitrary spatial filtering," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 410–411.
- [15] L. Zhang, A. Natarajan, and H. Krishnaswamy, "Scalable spatial notch suppression in spatio-spectral-filtering MIMO receiver arrays for digital beamforming," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3152–3166, Dec. 2016.
- [16] C. Kim, S. Joshi, C. M. Thomas, S. Ha, L. E. Larson, and G. Cauwenberghs, "A 1.3 mW 48 MHz 4 channel MIMO baseband receiver with 65 dB harmonic rejection and 48.5 dB spatial signal separation," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 832–844, Apr. 2016.
- [17] L. Zhang and H. Krishnaswamy, "Arbitrary analog/RF spatial filtering for digital MIMO receiver arrays," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3392–3404, Dec. 2017.
- [18] S. Jang, J. Jeong, R. Lu, and M. P. Flynn, "A 16-element 4-beam 1 GHz IF 100 MHz bandwidth interleaved bit stream digital beamformer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1302–1312, May 2018.
- [19] S. Mondal and J. Paramesh, "A reconfigurable 28-/37-GHz MMSEadaptive hybrid-beamforming receiver for carrier aggregation and multistandard MIMO communication," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1391–1406, May 2019.
- [20] S. Kalia, S. A. Patnaik, B. Sadhu, M. Sturm, M. Elbadry, and R. Harjani, "Multi-beam spatio-spectral beamforming receiver for wideband phased arrays," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 8, pp. 2018–2029, Aug. 2013.
- [21] S. Golabighezelahmad, E. Klumperink, and B. Nauta, "A 1-4 GHz 4×4 MIMO receiver with 4 reconfigurable orthogonal beams for analog interference rejection," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.* (*RFIC*), Jun. 2019, pp. 339–342.
- [22] J. Allen, "A theoretical limitation on the formation of lossless multiple beams in linear arrays," *IRE Trans. Antennas Propag.*, vol. 9, no. 4, pp. 350–352, Jul. 1961.
- [23] J. Butler and R. Lowe, "Beamforming matrix simplifies design of electronically scanned antennas," *Electron. Des.*, vol. 9, no. 8, pp. 170–173, 1961.
- [24] A. Tork and A. Natarajan, "Reconfigurable X-band 4×4 butler array in 32 nm CMOS SOI for angle-reject arrays," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.
- [25] Z. Ru, N. A. Moseley, E. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec. 2009.
- [26] D. Murphy *et al.*, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.
- [27] C. Andrews and A. C. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.
- [28] D. Yang, C. Andrews, and A. Molnar, "Optimized design of N-phase passive mixer-first receivers in wideband operation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 11, pp. 2759–2770, Nov. 2015.
- [29] "IRE standards on electron tubes: Definitions of terms, 1957," *Proc.IRE*, vol. 45, no. 7, pp. 983–1010, Jul. 1957.
- [30] S. Golabighezelahmad, E. Klumperink, and B. Nauta, "EVM-based performance evaluation of co-channel interference mitigation using spatial filtering for digital MIMO receivers," in *Proc. IEEE 92nd Vehicular Technol. Conf. (VTC2020-Fall)*, 2020.



Sajad Golabighezelahmad (Student Member, IEEE) received the B.Sc. degree in electrical engineering from the K. N. Toosi University of Technology, Tehran, Iran, in 2011, and the M.Sc. degree in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2013. He is currently pursuing the Ph.D. degree with the IC Design Group, University of Twente, Enschede, The Netherlands.

His current research is focused on RF front-end design for multiple-input multiple-output (MIMO) and beamforming applications.



Eric A. M. Klumperink (Fellow, IEEE) was born in Lichtenvoorde, The Netherlands. He received the B.Sc. degree from the Hogere Technische School, Enschede, The Netherlands, in 1982, and the Ph.D. degree from the University of Twente, Enschede, in 1997. His Ph.D. thesis was on transconductance-based CMOS circuits: circuit generation, classification and analysis.

He worked in the industry on digital hardware and software, and then joined the University of Twente, in 1984, shifting focus to analog CMOS

circuit research and resulted in several publications. In 1998, he started as an Assistant Professor with the IC-Design Laboratory, University of Twente, and shifted research focus to RF CMOS circuits. He was on sabbatical leave with Ruhr-Universität Bochum, Bochum, Germany. Since 2006, he has been an Associate Professor with the University of Twente, teaching analog and RF IC electronics and guiding Ph.D. and M.Sc. projects related to RF CMOS circuit design with a focus on software-defined radio, cognitive radio, and beamforming. He holds several patents. He has authored and coauthored more than 175 internationally refereed journal and conference articles.

Dr. Klumperink served as the IEEE SSC Distinguished Lecturer from 2014 to 2015 and a member of the technical program committees of the International Solid-State Circuits Conference (ISSCC) from 2011 to 2016. He has been a member of the IEEE RFIC Symposium since 2011. He was a co-recipient of the ISSCC 2002 and the ISSCC 2009 "Van Vessem Outstanding Paper Award." He served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II from 2006 to 2007, the IEEE TCAS—I from 2008 to 2009, and the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2010 to 2014. He was recognized as an ISSCC article contributor for contributing more than 20 articles from 1954 to 2013.



Bram Nauta (Fellow, IEEE) was born in Hengelo, The Netherlands, in 1964. He received the M.Sc. degree (*cum laude*) in electrical engineering and the Ph.D. degree in analog CMOS filters for very high frequencies from the University of Twente, Enschede, The Netherlands, in 1987 and 1991, respectively.

In 1991, he joined the Department of Mixed-Signal Circuits and Systems, Philips Research, Eindhoven, The Netherlands. In 1998, he returned to the University of Twente, where he is currently a Distinguished

Professor and the Head of the IC Design Group, where he served as the Chair of the Department of Electrical Engineering from 2016 to 2020. His current research interest is high-speed analog CMOS circuits, software-defined radio, cognitive radio, and beamforming.

Dr. Nauta is a member of the Royal Netherlands Academy of Arts and Sciences. He served as the President of the IEEE Solid-State Circuits Society from 2018 to 2019. He was in the Technical Program Committee of the Symposium on VLSI circuits from 2009 to 2013. He served in the Steering Committee and the Program Committee of the European Solid-State Circuit Conference from 1999 to 2017. He served as a Distinguished Lecturer of the IEEE for two terms. He was a co-recipient of the ISSCC 2002 and the 2009 "Van Vessem Outstanding Paper Award." He received the Simon Stevin Meester Award (500.000€) in 2014 and the largest Dutch National Prize for achievements in technical sciences. He was the 2013 Program Chair of the International Solid-State Circuits Conference (ISSCC). He also served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II from 1997 to 1999 and the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) from 2001 to 2006. He served as the Editor-in-Chief of the IEEE JSSC from 2007 to 2010.