# 2.4-GHz Highly Selective IoT Receiver Front End With Power Optimized LNTA, Frequency Divider, and Baseband Analog FIR Filter

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***Abstract*— High selectivity becomes increasingly important with an increasing number of devices that compete in the congested 2.4-GHz industrial, scientific, and medical (ISM)-band. In addition, low power consumption is very important for Internet-of-Things (IoT) receivers. We propose a 2.4-GHz zero-intermediate frequency (IF) receiver front-end architecture that reduces power consumption by 2× compared with state-of-the-art and improves selectivity by >20-dB without compromising on other receiver metrics. To achieve this, the entire receive chain is optimized. The low-noise transconductance amplifier (LNTA) is optimized to combine low noise with low power consumption. State-of-the-art sub-30-nm complementary metal–oxide–semiconductor (CMOS) processes have almost equal strength complementary field-effect transistors (FETs) that result in altered design tradeoffs. A Windmill 25%-duty cycle frequency divider architecture is proposed, which uses only a single NOR-gate buffer per phase to minimize power consumption and phase noise. The proposed divider requires half the power consumption and has 2 dB or more reduced phase noise when benchmarked against state-of-the-art designs. An analog finite impulse response (FIR) filter is implemented to provide very high receiver selectivity with ultralow power consumption. The receiver front end is fabricated in a 22-nm fully depleted silicon-on-insulator (FDSOI) technology and has an active area of 0.5 mm$^2$. It consumes 370 $\mu$W from a 700-mV supply voltage. This low power consumption is combined with a 5.5-dB noise figure. The receiver front end has −7.5-dBm input-referred third-order-intercept point (IIP3) and 1-dB gain compression for a −22-dBm blocker, both at maximum gain of 61 dB. From three channels offset onward, the adjacent channel rejection (ACR) is ≥63 dB for Bluetooth Low-Energy (BLE), BT5.0, and IEEE802.15.4.**

***Index Terms*— Analog finite impulse response (FIR) filter, frequency divider, high selectivity, Internet of Things (IoT), low power, low-noise transconductance amplifier (LNTA), receiver.**

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## I. Introduction

LOW-POWER receivers with very high selectivity are a prerequisite for the next-generation IoT applications. It is expected that the number of wireless devices will increase rapidly. Battery lifetime becomes increasingly important because the burden of charging or changing batteries directly increases with the number of devices. An increasing number of devices compete in the already crowded low-GHz spectrum, thereby increasing the receiver's interference rejection requirements, especially in the popular 2.4-GHz ISM-band.

Reduced power consumption and improved selectivity should be achieved without compromising on noise figure (NF). A good NF for state-of-the-art IoT receivers is 5–6 dB [1]–[6]. In IoT receivers, all blocks tend to contribute to the total power consumption [1]–[10]. Therefore, a fully optimized (system) design is required to obtain minimal power consumption.

This article is an extension on [11], where we proposed an IoT receiver front end that combines reduced power consumption with improved selectivity and without compromising on NF or linearity. Power optimization is applied across the entire receive chain: the LNTA, frequency divider with mixer, and baseband filter. The baseband filter is implemented as an analog FIR filter to improve selectivity without increasing the power consumption. The receiver front end is designed for BLE, BT5.0, and IEEE802.15.4 and contains on-chip impedance matching. In this article, we provide an extensive analysis of the optimizations in the LNTA, frequency divider, and baseband filtering architectures. Furthermore, the measurement results are extended, including additional linearity measurements and discussion on the obtained performance.

The structure of this article is as follows. First, the receiver front-end overview is provided in Section II. Followed by a detailed description of the optimizations in the LNTA (see Section III) and frequency divider (see Section IV), including a comparison to other divider approaches. The baseband filter architecture, including an analog FIR filter, is described in Section V. Section VI discusses the measurement results, and the conclusions are provided in Section VII.

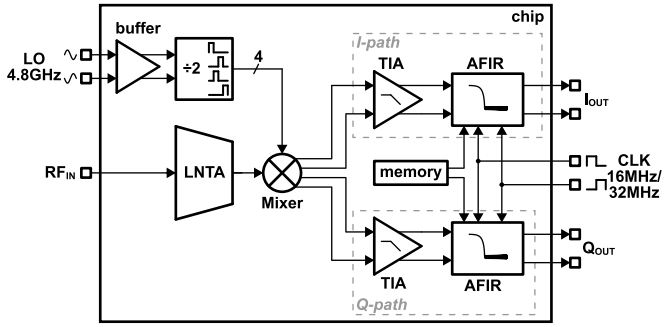


Fig. 1. Proposed receiver front-end architecture.

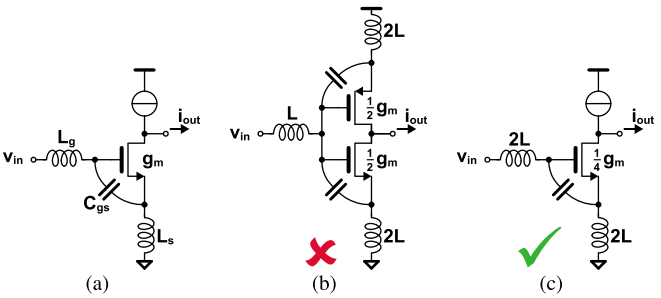


Fig. 2. Inductive degenerated LNTA design. (a) Architecture. (b) Push–pull implementation. (c) $2L$ implementation.

## II. Circuit Implementation

Fig. 1 shows the proposed receiver front end with zero-IF architecture [11]. A single-ended radio frequency (RF) input is converted to current by an LNTA. This current is passed through a four-phase passive mixer to create differential in-phase/quadrature-phase (I/Q) baseband signals. The current is converted to voltage and low-pass filtered by a transimpedance amplifier (TIA). The channel selection is performed by an analog FIR (AFIR) filter, clocked at 16 and 32 MHz for a 1- and 2-Mb/s data rate, respectively. The four-phase clock signals are provided by the divide-by-two frequency divider. For this prototype, the 16-/32-MHz and 4.8-GHz local oscillator (LO) clocks are provided externally, but multiphase clock generation and clock distribution are on-chip.

## III. Low-Noise Transconductance Amplifier

An inductive degenerated LNTA combines a low NF with low power consumption [12]. However, for very low power consumption, the design tradeoffs change. In the 2.4-GHz IoT receiver application targeted in this work, our design goal is minimum power consumption at a reasonable NF.

### A. Ideal Inductors

Fig. 2(a) shows the inductive degenerated topology. The input impedance is

$$Z_{\text{in}} = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s \tag{1}$$

where $g_m$ is the transistor's transconductance. Matching is accomplished at the resonance frequency

$$w_c^2 = \frac{1}{(L_s + L_g)C_{gs}} \tag{2}$$

for which $\text{Im}(Z_{\text{in}}) = 0$ and

$$Z_{\text{in}} = \frac{g_m}{C_{gs}} L_s = Z_0 = 50\ \Omega \tag{3}$$

where $Z_0$ is the source (antenna) impedance, here 50 Ω. The noise performance of the LNTA can be described by its noise factor: the signal-to-noise ratio (SNR) degradation from input to output. Including only the thermal noise of the transistor transconductance, the noise factor is [12], [13]

$$F = 1 + \gamma\, Z_0 \frac{\omega_c^2 C_{gs}^2}{g_m} \tag{4}$$

where $\gamma$ is the transistor's noise excess factor. The noise factor can be rewritten using (2) and the matching condition (3) as

$$F = 1 + \gamma \frac{1}{1+\alpha} \tag{5}$$

with $L_g = \alpha L_s$. The corresponding required transconductance is

$$g_m = \frac{1}{F-1} \cdot \frac{\gamma\, Z_0}{w_c^2 L_{\text{tot}}^2} \tag{6}$$

where $L_{\text{tot}} = L_s + L_g$. Equation (5) provides a possibly somewhat non-intuitive result: $F$ is independent on $g_m$. It is solely determined by the inductor ratio $\alpha$ for a given $\gamma$, assuming impedance matching and ideal inductors. According to (6), the minimal $g_m$ is obtained for a maximum $F$ and maximum $L_{\text{tot}}$. The maximum allowed $F$ is often specified. The maximum inductor value is generally constrained by its self-resonance frequency or chip area requirements. In IoT applications, it is not desirable to have a very high inductor ratio $\alpha$—often applied in ultralow NF designs to obtain minimal NF—but high $L_{\text{tot}}$ should be pursued to minimize $g_m$ and, hence, lower power consumption. The $L_g$ and $L_s$ values are in the same order of magnitude, given the maximum inductor value constraint.

Fig. 2 shows a thought experiment regarding the LNTA design; assuming that $\alpha = 1$ provides a sufficiently low NF, and for simplicity, the current source is ideal. Starting from $L_g = L_s = L$, one could propose a push–pull design [see Fig. 2(b)] since it provides double the $g_m$ for the same bias current [14]. At first sight, this seems favorable that only half the bias current is required. However, two $2L$-sized inductors are required to provide an effective $L_s = L$. When a maximum inductance value of $2L$ is available, the circuit of Fig. 2(c) can also be implemented. This configuration requires only $(1/4)g_m$—in other words, half the bias current of the push–pull architecture—because $g_m \propto 1/L_{\text{tot}}^2$. It also requires a smaller area than Fig. 2(b). This is a non-intuitive result and would mean that the push–pull architectures of [11] and [14]–[16] are unfavorable.

### B. Including $Q_L$

Detailed analysis shows that the circuits in Fig. 2 are oversimplified. Integrated inductors are far from ideal and have a typical quality factor $Q_L$ of 10 in the GHz frequency range.

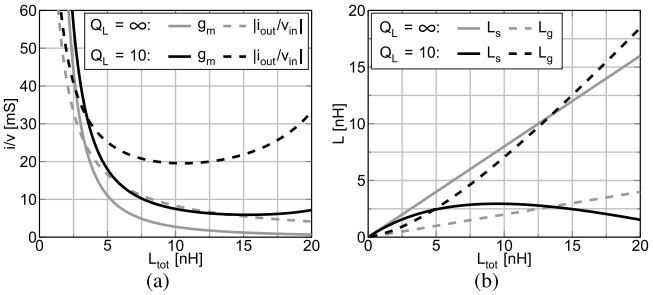


Fig. 3. LNTA parameters of Fig. 2(a) for different $Q_L$'s with $F = 1.8$. (a) Required transconductance and transconductance gain. (b) Inductance.

Including the limited $Q_L$, the noise factor becomes

$$F = 1 + \frac{r_g}{Z_0} + \frac{r_s}{Z_0} + \gamma \frac{1}{1+\alpha}\left(\frac{Z_0 + r_g + r_s}{Z_0}\right)^2 \tag{7}$$

where $r_g$ and $r_s$ are the resistances of $L_g$ and $L_s$, respectively. Not only the two resistive noise terms are added but also the $i_{\text{out}}/v_{\text{in}}$ and $i_{\text{out}}/i_{n,g_m}$ transfers change and, thereby, the $\gamma$ term, which was neglected in [12]. The $\gamma$ term increases for higher $r_g$ and $r_s$ (lower $Q_L$). The $Q_L$ limitation affects the circuit matching only little, but it has a significant effect on the noise factor and, thus, the required $g_m$. Using (7), the required $g_m$ is

$$g_m = \frac{1}{F - \left(1 + \frac{\omega_c L_{\text{tot}}}{Q_L Z_0}\right)} \cdot \frac{\gamma Z_0}{\omega_c^2 L_{\text{tot}}^2}\left(1 + \frac{\omega_c L_{\text{tot}}}{Q_L Z_0}\right)^2 \tag{8}$$

which simplifies to (6) for no inductor losses ($Q_L \to \infty$).

Fig. 3 shows the required $g_m$ and inductances for $Q_L = \infty$ and $Q_L = 10$ as functions of $L_{\text{tot}}$, assuming a desired noise factor of 1.8 and $\gamma \approx 1$. The required $g_m$ is higher for $Q_L = 10$ as expected. Some interesting observations can be made: for $L_{\text{tot}} \geq 10$ nH, the required $g_m$ is roughly constant; higher inductance hardly reduces the required $g_m$, even when neglecting that high-valued on-chip inductors typically have lower $Q_L$. The result is that the chip area can be saved. Furthermore, the required $L_s$ does not increase above 2.9 nH [see Fig. 3(b)]. $g_m$ is no longer proportional to $1/L_s^2$. The push–pull configuration is favorable when the maximum attainable inductor value is $\geq 2L_s$ (here, $\geq$5.8 nH).

Fig. 3(a) shows the LNTA transconductance "gain" $|i_{\text{out}}/v_{\text{in}}|$. A higher $|i_{\text{out}}/v_{\text{in}}|$ will result in smaller noise contribution of subsequent stages. At minimum $g_m$, $|i_{\text{out}}/v_{\text{in}}|$ is also at its minimum. However, it cannot be changed much by changing $L_{\text{tot}}$. By decreasing $L_{\text{tot}}$, $|i_{\text{out}}/v_{\text{in}}|$ increases, but the required $g_m$ increases more rapidly and, thus, the LNTA current consumption when taking into account that $|i_{\text{out}}/v_{\text{in}}|$ is squared regarding the noise contribution for subsequent stages. $|i_{\text{out}}/v_{\text{in}}|$ increases slightly for high inductor values, but the $Q_L$ and self-resonance frequency will decrease significantly for very large inductors ($L > 8$ nH).

The abovementioned analysis provides insight into the design complexity of the inductive degenerated LNTA. It concludes that $L_g$ and $L_s$ should be in the same order of magnitude, and a push–pull architecture can become favorable when including $Q_L = 10$ in the analysis. The LNTA transconductance gain cannot be increased much to reduce the noise contribution of subsequent stages because this would result in a large increase in power consumption or impractically large inductors.

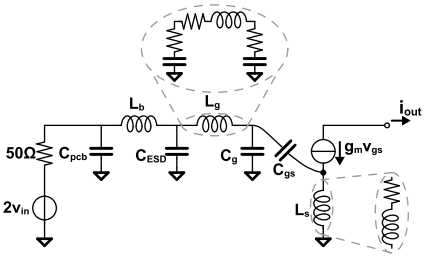


Fig. 4. Small-signal model for brute-force optimization of the LNTA.

### C. Brute-Force Search Model

Including the limited $Q_L$ is insufficient to fully optimize the LNTA design. This requires the more complex circuit of Fig. 4 to model the LNTA's small-signal behavior. Parasitic capacitors are included: $C_{\text{pcb}}$ the printed circuit board (PCB) parasitic, $C_{\text{ESD}}$ the electrostatic discharge (ESD) diodes' capacitance, including pad parasitics, and $C_g$ the parasitic to ground at the gate. $L_b$ is the bondwire inductance, which has an estimated $Q$-factor of 35. $L_s$ is modeled with $Q_L = 10$. $L_g$ is not connected to ground and requires more extensive $\Pi$-model. The $L_g$ $\Pi$-models are derived from the $S$-parameters at 2.44 GHz, which is sufficient to optimize for our target application. A design space for $L_s$, $C_{gs}$, and $g_m$ is estimated from the results of the simplified analysis. About 20 different $L_g$ designs were characterized using momentum simulations. All resistors and $g_m$ have an associated noise source.

Based on this design space, brute-force search is applied to find the minimal required $g_m$ for NF and $S_{11}$ <15 dB in the 2.4-GHz ISM-band requirements—optimizing the design. A push–pull architecture is selected because the required $L_s$ is sufficiently low at 3.6 nH. $L_g$ is 4.3 nH, and the inductors are approximately equal as expected to minimize $g_m$.

In addition to minimum $g_m$ for a given NF, the linearity requirement has to be satisfied. The main non-linearity sources are the transistor transconductance and output impedance. The output impedance non-linearity contribution depends on mixer/TIA design. Typically, the TIA input impedance is limiting in-band while out-of-band (OOB) the mixer switch-ON resistance. The transconductance non-linearity can be changed by the biasing conditions. A larger overdrive voltage improves the linearity at the cost of transconductance efficiency $g_m/I_{\text{dc}}$ and, hence, power consumption. An alternative measure would be to increase $L_s$ (the transconductance feedback), but the desired $L_s$ is already high.

### D. LNTA and Mixer Topology

Fig. 5 shows the proposed LNTA, including the passive mixer switches. In this design, both FETs are nominally biased at roughly half supply to allow for maximum voltage swing and minimize large-signal clipping given the supply headroom. The OOB IIP3 is slightly limited by drain voltage swing induced non-linearity in the LNTA due to the large mixer switch resistance values, which have been optimized to save

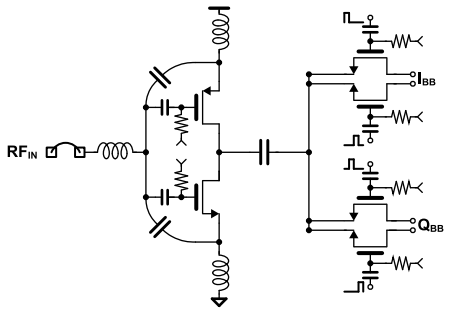


Fig. 5. Proposed LNTA including mixer.

power. The OOB IIP3 could be improved by 4 dB, according to simulation, by reducing the mixer switch resistance. The simulated output impedance magnitude of the LNTA is 3.3 kΩ. The linearity is the state of the art for a BLE receiver (IIP3 > −10 dBm) combined with a low mixer load to the frequency divider. Constant $g_m$-biasing is employed to maintain the LNTA NF, matching, and IIP3 specifications across process voltage temperature (PVT) variations.

## IV. Frequency Divider

A significant part of the power consumption is consumed by the frequency divider and mixer clock buffers in an IoT receiver, e.g., one-third in [5]. The proposed receiver front end employs 25% duty-cycle clocks to downconvert the single-ended LNTA output RF current to differential I/Q baseband currents. In this section, a minimum logic gate design strategy to minimize power consumption is explained, followed by a novel "Windmill" frequency divider architecture to achieve very low power consumption [11]. Finally, the Windmill divider performance is evaluated by comparison to multiple prior art designs.

### A. Minimum Logic Gate Design Strategy

Fig. 6 shows a chain of multiple (inverter) buffers; $P_n$ is the power provided by the supply, and $P_{\text{in},n} = P_{\text{out},n+1}$ is the power required to drive stage $n$. The fundamental required power to drive the (mixer) load is

$$P_{\text{load}} = f_m C_{\text{load}} V_{\text{DD}}^2 = P_{\text{out, 1}} \tag{9}$$

where $f_m$ is the mixer clock frequency and $V_{\text{DD}}$ the supply voltage. All other powers are "lost" —in the output parasitics of the buffer, as crowbar current or in driving the buffer. Therefore, the power dissipation of a single-buffer stage is

$$P_{\text{diss},n} = P_n - P_{\text{out},n} + P_{\text{in},n} \tag{10}$$

and the total dissipated power of an $N$ stage buffer is

$$P_{\text{diss}} = \sum_{n=1}^{N} P_n - P_{\text{out, 1}} + P_{\text{in},N} = \sum_{n=1}^{N} P_{\text{diss},n}. \tag{11}$$

The total random time deviation $\sigma_t$, either by phase noise and/or mismatch, is the sum of the variances

$$\sigma_t^2 = \sum_{n=1}^{N} \sigma_{t,n}^2 \tag{12}$$

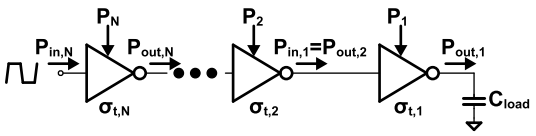


Fig. 6. Power consumption of multiple buffers driving a capacitive load.

assuming that the individual random timing deviations are uncorrelated. Equations (11) and (12) show that minimum $P_{\text{diss}}$ and $\sigma_t^2$ are obtained when the most efficient buffers—in terms of minimum $P_{\text{diss}}$ and $\sigma_t^2$—are used with a minimal number of stages. Therefore, a minimum number of efficient gates, e.g., CMOS logic gates, is a strong starting point to optimize the frequency divider.

### B. Windmill Frequency Divider

Fig. 7 illustrates the design procedure of the 25% duty-cycle frequency divider starting from the minimum—single—gate design strategy. Typically, differential 50% duty-cycle $LO$ signals are available at $2f_m$ or $4f_m$ to generate the mixer clocks [5]–[9], [17], [18]. At minimum, one selective gate is required to create the 25% duty-cycle mixer phases. Here, we start with $2f_m$ clocks. This results in less power consumption in the buffers that create the square wave $LO$ from the sinusoidal voltage-controlled oscillator (VCO) signals.

The available signals of the design are the input signals $LO+$ and $LO-$, 50% duty-cycle at $2f_m$, and the output signals $Q_x$ ($x = 1..4$), 25% duty-cycle at $f_m$, as shown in Fig. 7 (top left). The second illustration shows the single-gate implementation using a NOR-gate. A NOR-gate is chosen because it provides selectivity on high pulses as required. NOR-gates are a very efficient in modern CMOS technologies where n-channel field-effect transistors (NFETs) and p-channel field-effect transistors (PFETs) are approximately equal strength. $LO-$ is inverted through the NOR-gate to create $Q_1$. Every other $LO-$ low should be passed to $Q_1$, which requires a memory element to count the $LO-$ lows. The memory element is implemented, as shown in Fig. 7 (bottom left), by a NOR SR-latch. Signals $Q_2$ and $Q_4$ create an enable signal $E_1$, which is low for every other $LO-$ low. This structure is repeated in the last illustration for every output to create the "Windmill" divider—indicating the rotating nature of the gate enable signals $E_x$ and outputs $Q_x$. The latches toggle the $LO-$ and $LO+$ to $Q_1/Q_3$ and $Q_2/Q_4$, respectively.

Only the large transistors in the large NOR gates contribute to the output edges and have to be scaled to the drive mixer load. All other transistors can be the minimal size as long as the divider meets the speed requirement. Furthermore, only those large transistors contribute to phase noise and mismatch. In this way, very low power consumption is achieved while also realizing good phase noise and mismatch as only a single-gate propagation delay contributes to timing uncertainty. The top PFET of the opposite large NOR gates is shared, via nodes $a$ and $b$, to reduce the uncorrelated phase noise contributions that degrade the receiver's NF [19], [20]. In addition, since the PFET is shared, a single PFET is used to create two rising edges, reducing the power consumption of the preceding buffers. The phase relation of the outputs is independent of the startup condition as verified by the I/Q mismatch simulations.

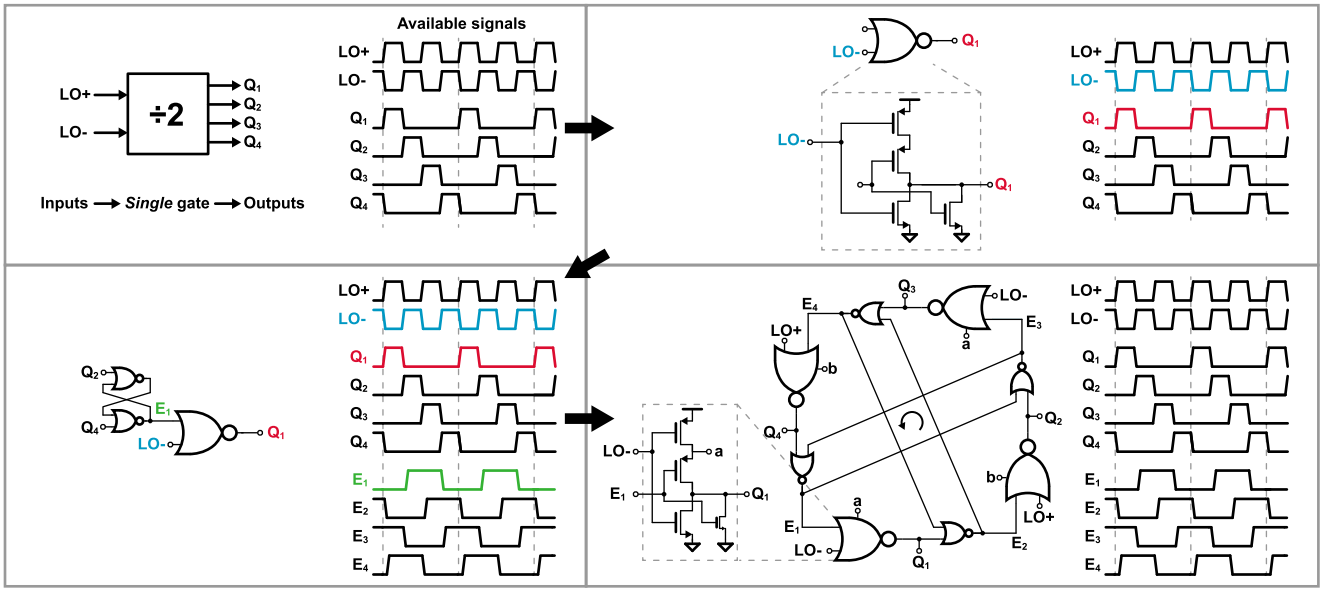


Fig. 7. Step-by-step design of the 25% duty-cycle "Windmill" frequency divider.

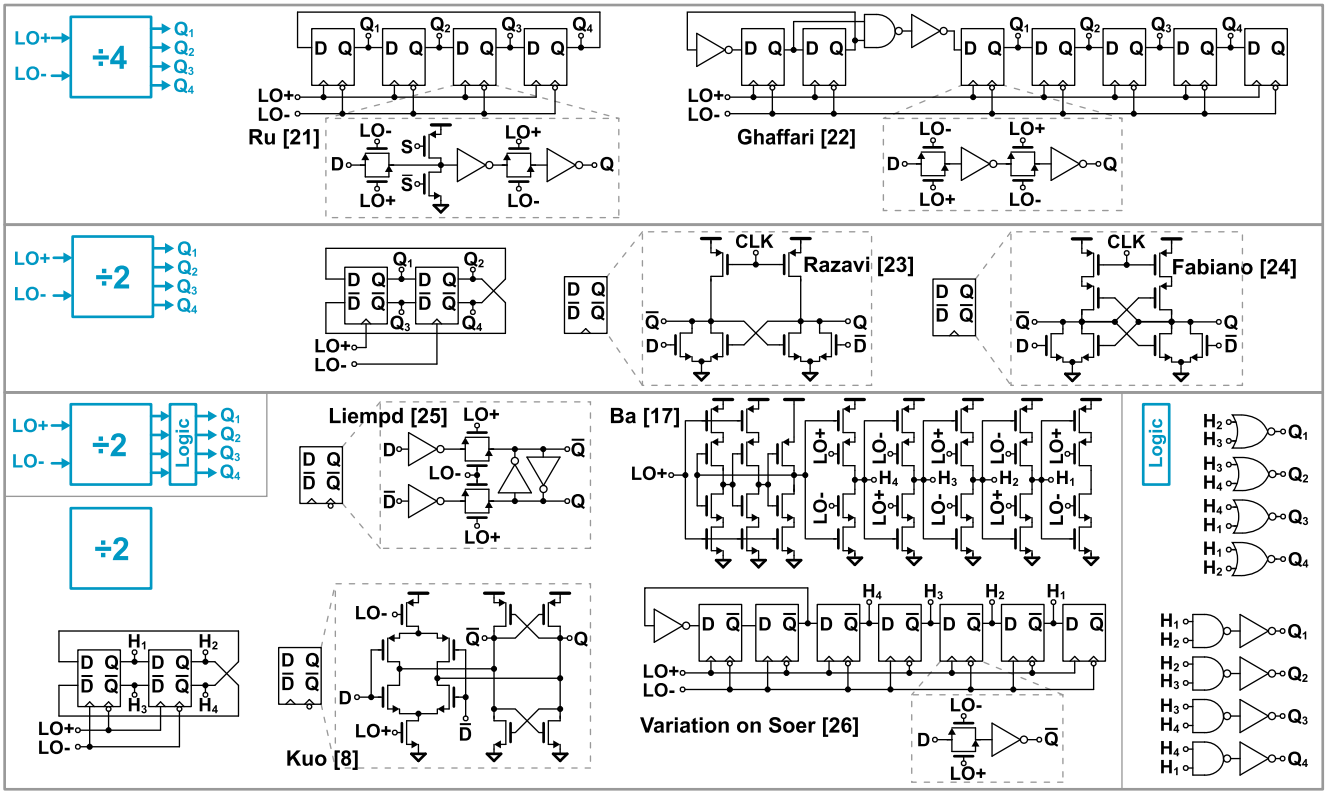


Fig. 8. Prior art divider architectures to create 25% duty-cycle clocks.

### *C. Divider Comparison*

In this section, we provide a comparison between published divider architectures that create 25% duty-cycle clock signals. Three approaches can be distinguished, as illustrated in Fig. 8.

1) *Direct Divide-by-4:* Divide a differential $LO$ at $4f_m$ by four to create 25% duty-cycle clock signals [21], [22].
2) *Direct Divide-by-2:* Divide a differential $LO$ at $2f_m$ by two to create 25% duty-cycle clock signals; the Windmill divider (see Fig. 7) [23], [24].
3) *Divide-by-2 With Logic:* Divide a differential $LO$ at $2f_m$ by two to create 50% duty-cycle clock signals at $f_m$ and use subsequent logic to create 25% duty-cycle outputs [8], [17], [25] and a variation on [26] without the extra intermediate inverters to reduce its power consumption.

The dividers, all designed in 22-nm FDSOI, are compared by simulation with the assumptions, as summarized in Fig. 9. $C_{\text{load}}$ is 4 fF for each $Q_x$-output—equal to the mixer switch that is optimized by using 3× the minimal finger gate pitch to reduce its parasitic capacitance and contact resistance by

TABLE I

SIMULATED PERFORMANCE COMPARISON OF 25% DUTY-CYCLE CLOCK DIVIDERS IN 22-nm FDSOI

| | Windmill | Ru [21] | Ghaffari [22] | Razavi [23] | Fabiano [24] | Kuo [8] | | Liempd [25] | Ba [17] | Soer [26] inspired |
|---|---|---|---|---|---|---|---|---|---|---|
| Division factor | 2 | 4 | 4 | 2 | 2 | 2 | | 2 | 2 | 2 |
| 50% → 25% duty-cycle | - | - | - | - | - | AND | NOR | AND | AND | AND |
| $P_{DC}$ [µW] | **36.1** | 41.7 | 53.1 | 187.0 | 57.4 | 62.9 | 63.9 | 59.7 | 59.7 | 57.9 |
| $P_{diss}$ [µW] | **27.3** | 47.1 | 70.0 | 172.5 | 51.1 | 53.5 | 54.5 | 48.7 | 57.1 | 49.2 |
| Phase Noise, white [dBc] (@100MHz) | **-159.0** | -157.0 | -157.0 | -155.3 | -154.5 | -154.9 | -156.7 | -155.4 | -154.6 | -154.9 |
| Phase Noise, 1/f region [dBc] (@10kHz) | **-135.0** | -132.8 | -132.9 | -132.5 | -134.5 | -130.4 | -132.2 | -130.9 | -130.0 | -129.9 |
| $\sigma_{IQ}$ [%] | 0.60 | 0.82 | 0.84 | 0.71 | **0.55** | 1.0 | 0.75 | 1.0 | 1.1 | 1.1 |

The assumptions for this comparison are shown in Fig. 9.

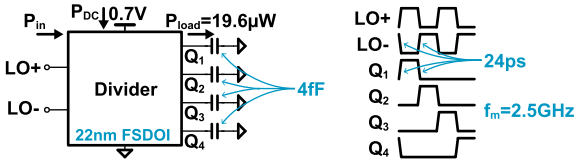


Fig. 9. Assumptions (highlighted) for simulation-based 25% duty-cycle divider comparison. The LO signals are shown for the divide-by-2 case.

increasing the number of sources and drain contacts. The output frequency is 2.5 GHz, which means an input frequency of 10 and 5 GHz for the divide-by-4 and divide-by-2 cases, respectively. The required power to drive the mixer load is 19.6 $\mu$W for a 700-mV supply. The $LO$ rise time (5%→95%) and fall time (95%→5%) are 24 ps. The transistors are sized such that the outputs $Q_x$ have equal rise and fall times as the inputs: 24 ± 0.3 ps. All designs are optimized in terms of scaling, e.g., in [22], the first divider is minimal size as these transistors do not contribute to the phase noise or mismatch. The dividers of [17], [22], and [26] contain a dummy device to avoid I/Q-offsets.

The schematic simulation results are summarized in Table I, where the best performance per specification is highlighted by bold text. The dividers are compared on power dissipation ($P_{\text{diss}}$), as defined in (10), phase noise in the white, and $1/f$ regions and I/Q-mismatch ($\sigma_{\text{IQ}}$). The I/Q mismatch is of little concern in the proposed zero-IF architecture but included for a complete comparison of the dividers. The divider dc power consumption ($P_{\text{dc}}$) is also included for completeness.

The power dissipation of the Windmill divider is 42% reduced or more compared with the other architectures. The Windmill divider has the lowest phase noise by 2 dB or more in the white noise region. The $1/f$-noise is less dominant because the noise corner is at a low offset frequency of about 2 MHz. Only the work in [24] has a slightly better I/Q-mismatch than the Windmill divider at a significantly higher power dissipation. For [8], the two different logic architectures are compared. The NOR-based design has lower phase noise and I/Q-mismatch at a similar power dissipation. The NOR-gate benefits from the equal NFET-PFET strength in modern CMOS processes

*Some Remarks:* Ru *et al.* [21] require startup circuitry, controlled by $S$ and $\overline{S}$, which can introduce possible startup issues.

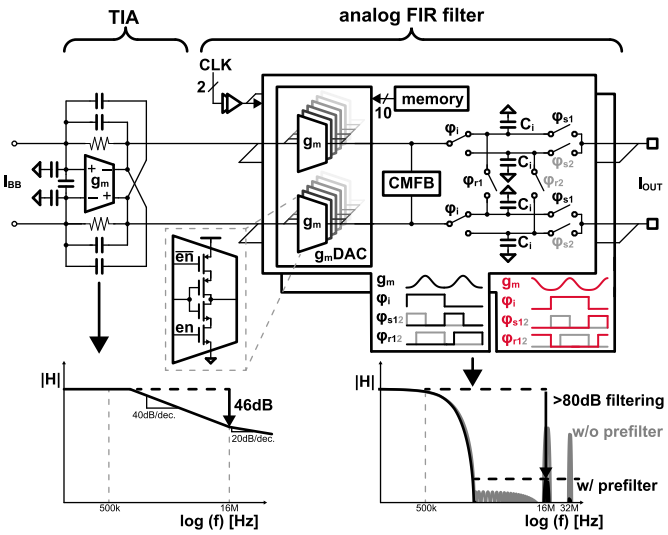


Fig. 10. Baseband filter consisting of TIA and analog FIR filter.

Razavi *et al.* [23] and Fabiano *et al.* [24] have clock overlap because the rising edge of $Q_{x+1}$ triggers the falling edge of $Q_x$. Ba *et al.* [17] have an additional static 1.2% I/Q-offset because the rising edge of $H_4$ is relatively slow. During $H_4$'s rising edge, the input of the tri-state inverter is not at ground because of charge injection of the previous stage, while the input node is floating. Furthermore, Ba *et al.* [17] have a significantly asymmetric load to the driver of the divider.

All in all, the Windmill divider consumes almost half the power and has 2 dB less phase noise. The Windmill divider is the only design with only a single gate involved in creating both rising and falling output edges and has outstanding performance. Moreover, it does not have any of the (potential) issues mentioned earlier. These results are not IoT application-specific—all designs can be scaled for more drive power or to reduce phase noise and/or I/Q-mismatch.

## V. BASEBAND ANALOG FIR FILTER

High selectivity is achieved by the baseband analog FIR filter as shown in Fig. 10. It contains two time-interleaved paths to double the sample-rate for the same filter bandwidth [27], [28]. The transconductor is implemented as a 10-bit pseudo-differential transconductance DAC ($g_m$DAC).

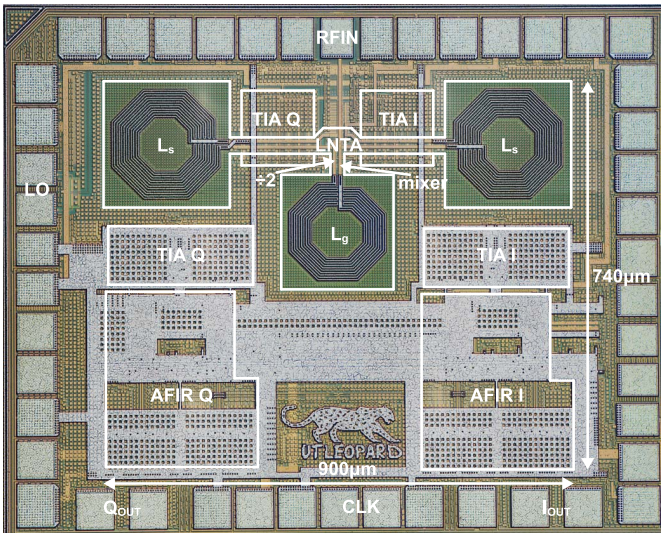


Fig. 11. Die micrograph indicating the major blocks.

A detailed explanation of the analog FIR filtering operation is described in [27] and [28]. Low power consumption is obtained by push–pull transconductors, 5-bit thermometer coding of the $g_m$DAC, and a low update rate of the $g_m$DAC. The push–pull transconductors have low input-referred noise for given supply current. The 5-bit thermometer coding of the $g_m$DAC reduces the number of transitions in the $g_m$DAC because the filter code turns fully on/off only once per integration cycle, much slower than the $g_m$DAC update frequency. Furthermore, the partially thermometer coding of the $g_m$DAC reduces the effect of transconductor mismatch on the filter stopband—in this design, limited to −60 dB [28].

The $g_m$DAC update rate is 16 MHz instead of 64 MHz [27], [28] to further reduce the power consumption [11]. This comes at the cost of a closer filter alias and proportionally reduced attenuation of the filter alias. The inherent sinc windowed integration provides now only 34 dB of attenuation of this alias. The TIA is employed to provide a prefilter that mitigates the remaining alias. The TIA provides second-order filtering by feedforward capacitors for about one decade [29]. In this way, 46 dB of filtering is achieved at the alias frequency, resulting in 80 dB of total attenuation of the analog FIR alias. The exact cutoff frequency of the TIA is relatively relaxed because it only has to provide prefiltering of the alias. Furthermore, the filtering characteristic is determined by the $g_m$DAC-code and clock signals—making the baseband filtering PVT insensitive [28]. Back-biasing is employed to compensate for the differential dc-offset in the TIAs. In this way, the dc-offset can be compensated without a significant increase in power consumption or noise—in contrast to current injection. The differential dc-offset of the $g_m$DACs is very small, well below 1 mV referred at the output.

## VI. Experimental Results

The receiver front end was designed and fabricated in a 22-nm FDSOI process and wire-bonded in a 40 × 40 pin quad-flad no-leads (QFN) package. The die has an active area of 0.5 mm$^2$, and the supply voltage is 700 mV. Fig. 11 shows the die micrograph.

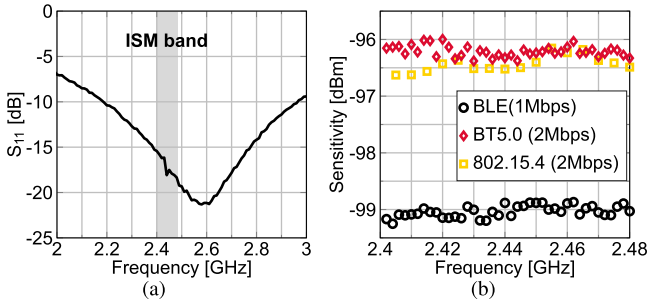


Fig. 12. Measured receiver front-end performance. (a) $S_{11}$. (b) Sensitivity.

The measurement setup is published in [11]. The package is placed in a zero insertion force (ZIF) socket (Ironwood SG-MLF). Impedance matching is realized on-chip—no external matching components are used. The capacitor output voltage is measured using an active probe (Teledyne LeCroy AP033), and the charge sharing loss is de-embedded as in [28]. The measurements are performed in BLE (1 Mb/s) mode unless stated otherwise.

### A. Matching and Sensitivity

The measured $S_{11}$ is shown in Fig. 12(a). Good matching ($S_{11} < -10$ dB) is achieved between 2.2 and 2.9 GHz. The receiver's $S_{11}$ is below −15 dB in the ISM-band, which is used in the targeted applications.

The measured noise figure is 5.5 dB. The measured sensitivity for <0.1% bit error rate (BER) is shown in Fig. 12(b) for each channel. The transmitted signal is a pseudorandom bit-stream (PRBS)-9 sequence. The received signal is demodulated using MATLAB CPM demodulator (BLE, BT5.0) and minimum-shift keying (MSK) demodulator (802.15.4). For BLE, the MATLAB CPM demodulator requires roughly 8-dB SNR to achieve 0.1% BER, which is about 2 dB less than a coherent receiver with threshold detection. The sensitivity is flat across the measured band. The 802.15.4 standard is characterized at 2-Mb/s half-sine shaped offset quadrature phase shift keying (HS-OQPSK) raw data rate without despreading as in [3] and [4].

### B. Linearity

The large-signal in-band linearity is characterized by the compression point. The in-band gain is shown in Fig. 13(a). The maximum gain is 61 dB, roughly 30 dB in both the front end up to the TIA and analog FIR filter. The output-referred 1-dB compression point ($OP_{1\,dB}$) is 5.0 dBm, corresponding to a 1.1-$V_{pp}$ differential output voltage.

The small-signal nonlinearity is characterized by the third-order modulation (IM3) product, as shown in Fig. 13. The IIP3 is −7.5 dBm for a 4.01-MHz offset at a maximum gain of 61 dB. The IIP3 is approximately flat from a 3-MHz offset frequency. The simulation shows that this is limited by the LNTA.

Fig. 14 shows the measured blocker 1-dB compression point ($B_{1\,dB}$), the blocker input power for which the in-band gain is 1 dB compressed. The $B_{1\,dB}$ is approximately −22 dBm for a frequency offset ≥ 3 MHz.

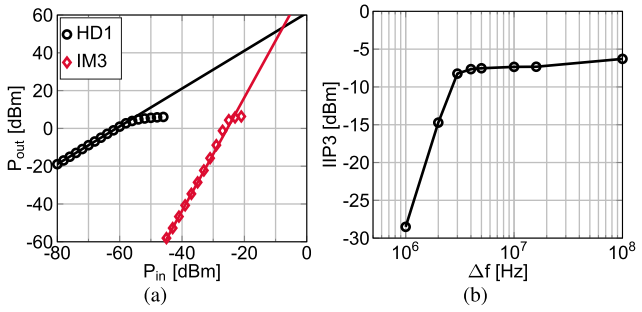


Fig. 13. Measured linearity. (a) In-band gain and out-of-band IM3 (for $\Delta f = 4.01$- and $2\Delta f = 7.98$-MHz input tones). (b) IIP3 versus frequency offset.

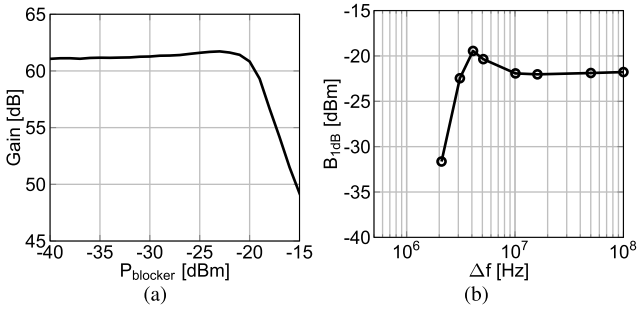


Fig. 14. Measured receiver front-end performance in presence of a blocker. (a) Gain for a blocker at 4.1-MHz offset. (b) $B_{1\,dB}$ versus frequency offset.

### C. Adjacent Channel Rejection

The receiver's performance in the presence of a blocker is characterized by the ACR. The ACR is measured with the desired signal strength at sensitivity + 3 dB and a blocker signal, modulated using the same standard with PRBS-15 sequence, at various offset frequencies. The wanted signal and blocker are generated with an R&S SMW200A and R&S SMBV100A, respectively. Fig. 15 shows the measured ACR.

The ACR is ≥63 dB for BLE (1 Mb/s) at a frequency offset ≥3 MHz. BT5.0 with double the data rate has double the filter bandwidth. This shows in the ACR as ≥65 dB ACR at ≥6 MHz, double the frequency offset of BLE. The 802.15.4 ACR is ≥67 dB for frequency offsets of ≥15 MHz. 802.15.4 does not use the Gaussian filtering of the transmitted signals and has, therefore, more transmitted spectral leakage in neighboring channels, which limits the maximal achievable ACR as confirmed here by the measurements. The filter alias at 16 MHz/32 MHz for 1 Mb/s/2 Mb/s is just visible by a small perturbation in the ACR rejection profile—indicating that the prefilter operates as desired.

In the following, we provide a short discussion regarding the ACR. From Fig. 15, we conclude that the ACR for BLE is limited to about 70 dB. Various sources can constrain the ACR performance.

1) *Limited Blocker Attenuation:* The (small-signal) filtering.
2) *Reciprocal Mixing:* Because of LO phase noise.
3) *Blocker Gain Compression:* Related to $B_{1\,dB}$.

The demodulation algorithm requires an SNR as derived from

$$\begin{aligned} \mathrm{SNR_{min}} &\approx 174 + \mathrm{Sensitiviy} - \mathrm{NF} - 10\log(\mathrm{BW}) \\ &\approx 10\ \mathrm{dB} \end{aligned} \tag{13}$$

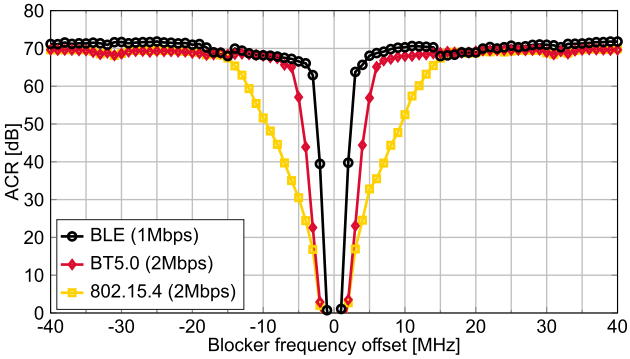


Fig. 15. Measured adjacent channel rejection for different standards.

where NF is the measured noise figure and BW is the bandwidth. Therefore, 70 dB of ACR requires about 80 dB of attenuation to still demodulate the wanted signal. The phase noise of the mixer clock will result in an in-band reciprocal mixing product. The receiver's blocker noise figure (BNF) can be estimated as [30]

$$\mathrm{BNF} \approx -174 + P_b + \mathcal{L}(\Delta f) \tag{14}$$

where $P_b$ is the blocker input power, which is

$$P_b = \mathrm{Sensitivity} + 3 + \mathrm{ACR} \tag{15}$$

at a given ACR level. From (13)–(15) the maximum allowed phase noise to achieve 70 dB ACR is derived as

$$\begin{aligned} \mathcal{L}_{\max}(\Delta f) &\approx -\mathrm{SNR_{min}} - 10\log(\mathrm{BW}) - \mathrm{ACR} \\ &\approx -140\ \mathrm{dBc/Hz} \end{aligned} \tag{16}$$

neglecting the circuit induced noise, i.e., BNF = NF + 3 dB, as in [30]. The minimal required $B_{1\,dB}$ for 70 dB ACR is

$$\begin{aligned} B_{1\,\mathrm{dB,\,min}} &\approx \mathrm{Sensitivity} + 3 + \mathrm{ACR} \\ &\approx -26\ \mathrm{dBm}. \end{aligned} \tag{17}$$

From a frequency offset of 5 MHz onward, the BLE ACR is roughly constant at 70 dB. Although the analog FIR filter has constant rejection, the prefilter has more attenuation for larger frequency offsets. Hence, the ACR is not limited by the filter attenuation in this region. The simulated phase noise of the Windmill divider is –153.6 dBc/Hz at the 1-MHz offset, which means that the phase noise also is not limiting. The ACR is most likely limited by blocker gain compression of −22 dBm, which is somewhat more severe for a modulated blocker. This also explains that the 2-Mb/s ACR is slightly worse because these standards have 3 dB higher sensitivity and, thus, less "headroom" toward blocker gain compression.

At 2-MHz offset, the ACR is 39 dB—requiring a $B_{1\,dB}$ of approximately −57 dBm, which is much less than the measured −31 dBm. The required filtering is roughly 49 dB. The expected attenuation at 2 MHz is about 70 dB (10-dB TIA + 60-dB analog FIR [27], [28]). However, the blocker is modulated with 1 Mb/s, covering a bandwidth of 1 MHz, so that the filter attenuation from 1.5- to 2.5-MHz offset is relevant. The worst case attenuation at 1.5 MHz is only 46 dB (6-dB TIA + 40-dB analog FIR [27], [28]) because of the steep FIR filter profile. At 3-MHz offset, the expected filtering is 76 dB (16-dB TIA + 60-dB analog FIR [27], [28]).

TABLE II
RECEIVER PERFORMANCE SUMMARY AND COMPARISON

| | This Work | | | [9] ISSCC'20 | | [18] ISSCC'20 | [10] TMTT'19 | [1] ISSCC'18 | [2] ISSCC'18 | | [3][h] ISSCC'15 | | [7] ISSCC'13 | [5] CICC'17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Standard** | BLE | BT5.0 | 802.15.4[d] | BLE | BT5.0 | BLE | BLE | BLE | BLE | BT5.0 | BLE | 802.15.4[d] | BLE | BLE |
| **Data rate [Mbps]** | 1 | 2 | 2 | 1 | 2 | 1 | 1 | 1 | 1 | 2 | 1 | 2 | 1 | 1 |
| **On-chip Matching** | Yes | | | Yes | | Yes | No | Yes | Yes | | No | | Yes | Yes |
| **$P_{DC}$ [mW]** | 0.37 | 0.40 | 0.40 | 0.89[e] | - | 5.3[g] | 1.44[e] | 1.2[e] | 1.1[e] | - | 1.95[e] | - | 1.7 | 0.7[e] |
| **NF [dB]** | 5.5 | | | - | | - | 7.2 | 6 | 5.9 | | 6.1 | | 8.5 | 5.2 |
| **Sensitivity [dBm]** | -99[b] | -96[b] | -96.5[b] | -96.4 | -93.5 | -94 | -92 | -94 | -95 | -92 | -94 | -91 | - | -95.8 |
| **ACR 2nd/3rd channel[a]** | 39/63[b,c] | 44/65[b,c] | 52/67[b,c] | 36.1/41.0[f] | 36.3/45.0[f] | 40/42[f] | 29/42[f] | 31/36[f] | 18/30[f] | 18/29.5[f] | 25/35[f] | 24/35[f] | - | - |
| **IIP3 [dBm]** | -7.5 | | | -13.1 | | - | -17 | - | - | | - | | -6 | -19.7[i] |
| **$B_{1dB}$ [dBm]** | -22 | | | - | | - | - | - | - | | - | | - | - |
| **Gain [dB]** | 61 | 57 | 57 | 43.1 | | - | 42 | 68 | - | | - | | 57 | 47-72 |
| **Supply Voltage [V]** | 0.7 | | | 0.5 | | 0.8 | 1.2 | 1 | 0.8 | | 1 | | 0.6&1.2 | 1 |
| **Active Area [mm²]** | 0.5 | | | 1.9[g] | | 0.89[g] | 0.7 | 1.64[g] | 0.8[g] | | 1.3[g] | | 0.22 | 0.7[g] |
| **Technology** | 22nm FDSOI | | | 22nm FDSOI | | 40nm CMOS | 130nm CMOS | 65nm CMOS | 40nm CMOS | | 40nm CMOS | | 65nm CMOS | 40nm CMOS |

[a]Channel spacing: BLE 1MHz; BT5.0 2MHz; 802.15.4 5MHz. [b]Demodulated using Matlab CPM demodulator (BLE, BT5.0) and MSK demodulator (802.15.4), both using a Viterbi algorithm with traceback depth of 16. [c]Measured with wanted signal at sensitivity +3dB. [d]Verified with 2Mbps raw data rate HS-OQPSK without de-spreading as in [3,4]. [e]Power consumption is estimated from power breakdown, e.g. w/o VCO/PLL. [f]Measured with wanted signal at -67dBm. [g]Includes more than RX path. [h]Some specifications of this work are found in [4]. [i]At minimal gain of 47dB.

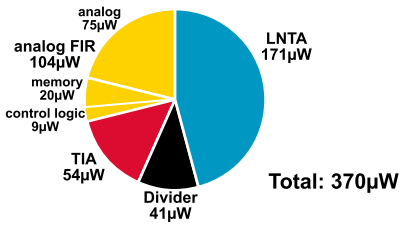


Fig. 16. Power consumption breakdown.

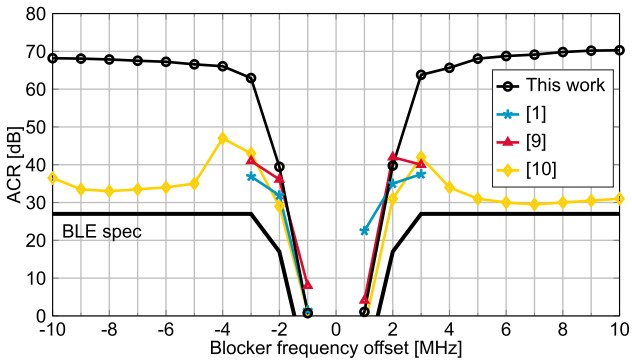


Fig. 17. Comparison of the measured ACR for BLE (1 Mb/s).

Therefore, the measured ACR of 39 dB/63 dB for 2-/3-MHz offset can be explained by taking into account the blocker bandwidth. Consequently, the filter profile limits the ACR performance below approximately 5 MHz offset when also taking into account the divider phase noise mentioned earlier.

The receiver's frequency response was not measured here, as it is constrained by compression above 5 MHz. Instead, we report ACR performance because this is what ultimately matters. The analog FIR filter response can be found in [28].

### *D. Power Consumption*

The total power consumption is 370 $\mu$W, as shown in Fig. 16. The frequency divider power consumption is only 41 $\mu$W, excluding the preceding buffer.

### *E. Comparison*

The ACR in BLE-mode is compared with state-of-the-art IoT receivers in Fig. 17. The proposed receiver front end has $>$20 dB improved ACR for frequency offsets $>$2 MHz. The prior art is measured with the wanted signal at $-$67 dBm, which is similar to placing a 29-dB attenuator in front of the proposed receiver front end. Alternatively, the feedback resistor can be reduced to avoid gain compression. The TIA feedback resistor is tunable in this design—allowing a 20-dB gain reduction. Note that this is not an industrial product design but rather an academic research article that has a broader scope: software-defined ultralow-power radio front ends. Rather than choosing a standard specific sensitivity, we, instead, use a more general standard independent criterion: (actual NF-based) sensitivity of + 3 dB.

Table II summarizes the proposed receiver's performance and compares it to state-the-of-art 2.4-GHz IoT receivers—only comparing the front end. The power consumption of the receive chain is reduced by 2$\times$ or more while achieving a similar noise figure. The ACR is improved by more than 20 dB at the third channel offset. The IIP3 linearity is similar or higher than the prior art.

### *F. Full Receiver Discussion*

In this section, the proposed design's performance is placed in the perspective of a full receiver design—including phase-locked loop (PLL) and analog-to-digital converter (ADC).

In this design, all the channel filtering requirements are achieved by placing the high-order analog FIR filter after the

TIA. This architecture choice significantly relaxes the dynamic range, sample rate, and power consumption requirements of the ADC, and down-stream digital signal processing functions, which only has to support demodulation and symbol detection.

In an application, the LO comes from an on-chip PLL with VCO, and its phase noise could result in significant blocker induced noise, which cannot be filtered—constraining the ACR. The phase noise of a state-of-the-art 0.5-mW 5-GHz VCO is $-140$ dBc/Hz at 10-MHz offset [31]. This corresponds to $-140$ dBc/Hz at 5-MHz offset when divided down to 2.5 GHz using the frequency divider, which is sufficiently low for the achieved ACR.

It is useful to estimate the total power consumption of the entire receiver. A state-of-the art all-digital phase-locked loop (ADPLL) consumes 673 $\mu$W [32] and will consume roughly 910 $\mu$W when implementing the low-phase-noise VCO design of [31] to obtain the ACR performance. The sampled output of the analog FIR filter, at 1 Msample/s, can be used for ADC conversion. The ADC power consumption will be negligible if a successive-approximation register (SAR) ADC is used. For example, the 1-Msample/s 10-bit SAR ADC in [33] consumes only 3.2 $\mu$W, more than sufficient for demodulation. Hence, the total power consumption, excluding demodulation, is estimated as $0.91 + 0.37 = 1.3$ mW.

## VII. Conclusion

A 2.4-GHz IoT receiver front end is proposed and characterized for BLE, BT5.0, and IEEE802.15.4. The entire receive chain is optimized to minimize power consumption and improve selectivity.

Several techniques are proposed that achieve a 370-$\mu$W power consumption—almost $2\times$ lower than the state of the art—in combination with a competitive 5.5-dB NF. The LNTA has a push–pull inductive degenerated common-source architecture and is optimized using brute-force search on a simplified, though accurate, model. A single-gate Windmill frequency divider has almost half the power dissipation concurrent with a phase noise improvement of 2 dB or more compared with the prior art. An analog FIR filter is implemented with prefilter. Its 10-bit transconductor digital-to-analog converter (DAC) contains push–pull transconductors, 5-bit thermometer coding, and a low (16 MHz for BLE) FIR-coefficient update rate to optimize its power consumption while also achieving very sharp transition band. The receiver has $\geq$63-dB ACR at $\geq$3 channels offset improving the state of the art by $>$20 dB.

The proposed architecture and implementation techniques result in very low power consumption combined with outstanding selectivity, which makes the receiver front-end design ready for future IoT standards.

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