Introduction to the Special Issue on the 2020 IEEE International Solid-State Circuits Conference (ISSCC)

I. Introduction

THIS Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is dedicated to a collection of the best articles selected from the 2020 IEEE International Solid-State Circuits Conference (ISSCC) that took place on February 16–20, 2020, in San Francisco, CA, USA. This Special Issue covers articles from the Wireline, Digital Circuits, Digital Architectures and Systems (DASs), Machine Learning and AI, and Memory Committees.

II. Wireline Articles

Data centers continue to drive the demand for ultra-high-speed interconnects. Consequently, we have recently witnessed the first demonstration complete 56-Gb/s transceivers and 112-Gb/s individual transmitters and receivers that extend bandwidth and channel reach with a combination of analog circuit techniques and greater reliance on digital signal processing for long reach.

In this ISSCC 2020 Special Issue, the trend continues with the first complete transceiver design at 112 Gb/s and two high-speed transmitters using nanometer CMOS and FinFET technologies as well as 3-D integration.

The first article by Im *et al.* presents the first complete 112-Gb/s PAM-4 wireline transceiver. It demonstrates superior performance and robustness with better than 1E-8 BER over long-reach channels with more than 37-dB insertion loss. The analog receiver front-end takes advantage of inverter-based Gm/inverse-Gm load cells, enabling 40% power-efficiency improvement and 60% silicon area reduction compared with conventional RC-degenerated architectures.

The next article by Li *et al.* describes a 3-D integrated 112-Gb/s PAM-4 optical transmitter using silicon photonic microring modulators, on-chip laser, and co-packaged CMOS driver. The 3-Vpp thermal controlled driver utilizes a LUT-based PAM-4 nonlinear equalizer to address both static and dynamic microring modulator nonlinearities.

The third and final article by Groen *et al.* presents a flexible multi-protocol DSP-DAC-based H-bridge transmitter operating from 10 to 112 Gb/s. The lookup-table-based DSP provides flexible equalization while the soft switching driver provides up to 1.2-Vpp signal swing to achieve high SNR without exceeding the 7-nm devices breakdown voltages.

III. Digital Circuits Articles

Three articles have been selected from Digital Circuits sessions. The first article by Kundu *et al.* presents a self-calibrated 2-bit time-period comparator-based synthesized fractional-N MDLL in 22-nm FinFET CMOS. A replica DCO-based coarse DTC automatically tracks the DCO period and adjusts its gain. Any residue error in the DTC gain is corrected by a loop operating in the background. The proposed MDLL achieves the best power efficiency and lowest reference spur compared to the state-of-the-art inductor-less fractional-N frequency synthesizers. The second article by Jia *et al.* proposes a compute-adaptive elastic clocking technique that leverages instruction and operand-based dynamic timing enhancement for an array of processing elements (PEs). The technique provides up to a 19% performance gain and saves up to 34% energy when running machine-learning applications. The third paper by Yoon *et al.* presents an ultra-low-power mixed-signal oscillator-based neuroSLAM accelerator implementing a biologically inspired localization and mapping algorithm. A test-chip in 65-nm CMOS demonstrates correct SLAM operations and successful loop closure with a peak energy efficiency of 8.79 TOPS/W where the power consumption is 23.82 mW.

IV. Digital Architectures and Systems Articles

In the DAS category, five articles from three sessions have been selected. The first article by Vivet *et al.* presents a 96-core processor with six chiplets 3-D stacked on an active interposer with 3-Tb/s/mm^2 interchiplet interconnects. The second article by Berry *et al.* introduces a 12-core 5.2-GHz IBM z15 microprocessor. The third article by Wu *et al.* develops a fully integrated genetic variant discovery SoC for next-generation sequencing, while the fourth article by Chung *et al.* introduces a 1.5-μJ/task path-planning processor for 2D/3D autonomous navigation of microrobots. The last article by Das *et al.* presents EM and power SCA-resilient AES-256 in 65-nm CMOS for security applications.

V. Machine Learning and AI Articles

Two articles from the Machine Learning sessions of ISSCC 2020 have been selected. The first article by Shan *et al.* presents an always-on keyword spotting (KWS) chip for audio wake-up systems. In order to significantly reduce the memory footprint and computational load, several techniques are introduced such as a binarized depthwise-separable CNN and Mel frequency spectrum coefficient circuit, achieving 510 nW with 2-kB on-chip memory in 28-nm CMOS. The second article by Yamamoto *et al.* describes a high-performance annealing

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processor for solving combinatorial optimization problems. It supports 512-spin fully-connected graphs and can update multiple states of fully connected spins simultaneously by introducing stochastic cellular automata annealing. The prototype chip fabricated in 65-nm CMOS technology achieves the best performance among the state-of-the-art processors for ground-state search.

VI. Memory Articles

This Special Issue includes expanded versions of five significant articles on memory. The first article by Chang *et al*. describes a 5-nm 135-Mb SRAM array implemented with EUV and high-mobility transistor technology achieving a record 30-Mb/mm^2 bit density. Second, an article by Sinangil *et al.* elaborates on a 4b-input $\times$ 4b-weight CIM utilizing standard 8T SRAM bitcells and a Flash ADC in a 7-nm CMOS FinFET technology. The third article by Chun *et al.* details a 16-GB HBM2E in a second-generation 10-nm class DRAM process achieving 640 GB/s. Fourth, an article by Chi *et al.* presents a 12-Gb LPDDR5 in a second-generation 10-nm class DRAM process with low power and speed-boosting techniques. The fifth and final article by Kouchi *et al.* describes a 128-Gb 1b/cell 3-D flash memory using 96-word-line-layer technology that delivers 4-μs read latency.

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Friedel Gerfers (Member, IEEE) received the Dr.Ing. degree from the Albert-Ludwigs-University of Freiburg, Freiburg im Breisgau, Germany, in 2005.

Since 2003, he has gained his first industrial research and development experience at Philips Semiconductor, Munich, Germany. In 2006, he joined Intel Research, Santa Clara, CA, USA, as Post-Doctoral Research Fellow, working on new types of piezoelectric MEMS sensors and their readout circuits. His entrepreneurial spirit led him in the years 2007–2011 to the start-up companies Alvand Technologies Inc., Santa Clara, and Aquantia, San Jose, CA, USA. In the role of a Technical Director, he led the mixed-signal departments, which were crucial for the successful market positioning of these companies in the field of high-speed data transmission systems that operate close to the Shannon limit. In 2009, he was the Co-Founder of the technology start-up, NiederRhein Technologies, Mountain View, CA, USA. More recently, he was responsible for the worldwide development of high-precision analog-to-digital converters for integrated device technology (IDT). The team was later acquired by Apple Inc., Cupertino, CA, USA, in 2014. In 2018, he co-founded IC4X GmbH, Berlin, Germany, which is specialized in the development of high-performance analog and mixed-signal circuits and systems. Since 2015, he has been a Full Professor with the Technische Universität Berlin, Berlin, where he is currently the Director and the Head of the Chair of Mixed Signal Circuit Design (MSC). He is also a Scientific Advisory Board Member of Mentor Siemens, Fremont, CA, USA, and the Leibniz-Institute–Innovations for High-Performance Microelectronics (IHP), Frankfurt, Germany. He is the author of the book *Continuous-Time Sigma-Delta A/D Conversion, Fundamentals, Error Correction and Robust Implementations*. He has authored or coauthored several other book chapters and holds more than 15 patents.

Dr. Gerfers is also a Technical Program Committee Member of the IEEE International Solid-State Circuits Conference (ISSCC), IEEE European Solid-State Circuits Conference (ESSCirC), the European Microwave Week (EUMW), and the Optical Fiber Communications Conference and Exhibition (OFC). In recognition of this achievement in this field, he was awarded the Einstein-Professorship for Mixed Signal Circuit Design from the Einstein Foundation, in 2019.

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Dr. Marković received the NSF CAREER Award in 2009, the 2014 ISSCC Lewis Winner Award for Outstanding Paper, and the 2007 David J. Sakrison Memorial Prize for his Ph.D. degree. He was a co-recipient of the ISSCC Jack Raper Award for Outstanding Technology Directions in 2010. He served as an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2011 to 2015, the Technical Program Committee of ISSCC from 2015 to 2020, and the VLSI Circuits Symposium from 2016 to 2019.

Jun Deguchi (Member, IEEE) received the B.E. and M.E. degrees in machine intelligence and systems engineering and the Ph.D. degree in bioengineering and robotics from Tohoku University, Sendai, Japan, in 2001, 2003, and 2006, respectively.

In 2004, he was a Visiting Scholar with the University of California at Santa Cruz, Santa Cruz, CA, USA. In 2006, he joined Toshiba Corporation, where he was involved in the design of analog/RF circuits for wireless communications, CMOS image sensors, high-speed I/O, and accelerators for deep learning. From 2014 to 2015, he was a Visiting Scientist with the MIT Media Lab, Cambridge, MA, USA, where he was involved in research on brain/neuroscience. In 2017, he moved to Kioxia Corporation (formerly Toshiba Memory Corporation), Tokyo, Japan, where he has been a Research Lead of an advanced circuit design team working on high-speed I/O and deep learning/in-memory accelerators.

Dr. Deguchi has been serving as a member for the International Technical Program Committee (TPC) of the IEEE International Solid-State Circuits Conference (ISSCC) since 2016 and the IEEE Asian Solid-State Circuits Conference (A-SSCC) since 2017. He has also served as the TPC Vice-Chair for the IEEE A-SSCC 2019 and a Review Committee Member for the IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS) 2020.

Eric Karl (Member, IEEE) received the B.S.E., M.S.E., and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2002, 2004, and 2008, respectively.

In the past, he has been responsible for the design and validation of lead vehicles for process technology development across nearly a dozen Intel technology programs spanning from 32- to 3-nm process technologies. Before joining Intel's Technology Development organization in 2008, he held positions at Intel Circuit Research Lab, IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, and Sun Microsystems. He is currently a fellow and the Director of Advanced Design at Intel Corporation, where he is responsible for design technology co-optimization and IP development spanning standard-cell logic libraries, embedded memories, high-speed DDR, SERDES I/O, PLLs, and embedded fuse. He is also the Director of Embedded Memory Technology and Circuits with Intel Corporation, where he is responsible for technology definition, bitcell design, and circuit-technology strategy.

Dr. Karl received the Senior Scholar Award and the GAANN Teaching Fellowship at the University of Michigan, the Intel Achievement Award, and the Company's Highest Technical Honor in 2012 for the development of circuits technology enabling the world's first high-volume production FinFET SRAM process. He has been serving as a Technical Program Committee Member for the IEEE International Solid-State Circuits Conference (ISSCC) since 2019. He served as a Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS in 2020.