

# Energy Efficient Startup of Crystal Oscillators Using Stepwise Charging

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**Abstract**—Crystal oscillators can be started up quickly by using energy injection techniques. However, the generation of the injection waveform, as well as driving the large capacitive load formed by the crystal, costs a large amount of energy. This article applies the concept of stepwise charging to reduce the energy required to drive the crystal. The energy required to generate the injection waveform by self-timed injection is reduced by using a discrete-time dynamic-bias comparator which uses a simple offset calibration method. Furthermore, the bridge switch resistance is varied dynamically through self-timed control logic to alleviate the accuracy-speed tradeoff. A prototype was manufactured in a 65-nm (triple-well) CMOS technology, which was tested with various crystals ranging from 24 to 50 MHz, improving upon the state of the art in energy consumption.

**Index Terms**—Capacitive load, crystal oscillators, duty cycling, energy injection, Internet of Things (IoT), low power, startup energy, startup time, stepwise charging.

## I. INTRODUCTION

ENERGY is scarce in low-power wireless systems, such as wireless sensor nodes for Internet of Things (IoT), since they are usually powered from, e.g., a battery or energy harvester. To maximize battery life—or achieve a battery size reduction for the same lifetime—it is important to minimize the system's (average) power consumption. One method to minimize the power consumption is duty cycling, in which the device spends most of the time in a low-power sleep mode, only waking up briefly for transmit/receive events [1]. The required time to wake-up and the associated energy consumption can be a significant part of the overall energy consumption, especially if the transmit/receive events are short. One of the circuit blocks that has to be started when the device wakes up is the crystal oscillator that serves as a frequency reference. While the high-quality factor of a crystal resonator allows excellent phase noise, it also implies a long startup time. Even though the startup time of practical crystal oscillators has been pushed toward the lower limit in the recent literature, their startup energy consumption is still large.

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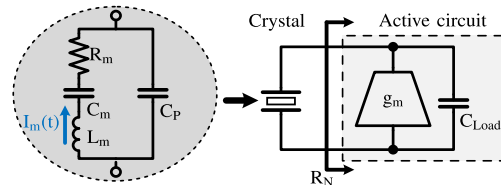


Fig. 1. Generic crystal oscillator.

This article presents techniques to reduce the energy required to start up crystal oscillators.

A generic crystal oscillator is shown in Fig. 1. The fundamental resonance mode of the crystal is usually modeled as a series  $RLC$  circuit that represents the mechanical resonance mode, in parallel to a capacitance  $C_P$  that models the crystal parasitics. The active circuit provides a capacitive load  $C_{Load}$  as specified by the crystal manufacturer, as well as a transconductance  $g_m$  to realize a negative resistance  $R_N$  that is large enough to compensate the crystal losses as to sustain oscillation. When the oscillator is started, the amplitude  $\hat{I}_m$  of the motional current  $I_m(t)$  grows from its initial value  $I_m(0)$  to the steady-state amplitude  $\hat{I}_{m,ss}$ , provided that the magnitude of  $R_N$  is larger than the crystal  $R_m$ . Up to recently, startup was typically achieved with a relatively low magnitude of  $R_N$  and from a small initial condition  $I_m(0)$  (circuit noise). This results in lengthy startup times in the order of milliseconds [2]–[7].

The startup time can be decreased by increasing the magnitude of  $R_N$  by changing  $g_m$  and/or  $C_{Load}$  during startup. The minimum startup time that can be achieved in this way is normally limited by  $C_P$  [7]–[11]. This limit can be overcome by making the active circuit appear inductive to (partially) cancel  $C_P$ . This can be achieved by capacitive loading of the internal nodes of a multistage amplifier [9], [10], [12], [13] or adding an active inductor circuit [14]. Although these solutions can achieve very low startup energy, it is difficult to exactly compensate  $C_P$ , resulting in relatively long startup times.

The fastest and most energy efficient circuits use an injection source to pre-energize the crystal, as shown in Fig. 2(a). By applying a voltage at exactly the resonance frequency for a duration  $T_{inj}$ , the amplitude  $\hat{I}_m(t)$  increases with every cycle, as shown in Fig. 3, ideally reaching the desired steady-state swing after  $T_{inj}$ . To achieve this, the injection signal should be in phase with the motional current  $I_m(t)$  during the entire injection period  $T_{inj}$ . Any injection frequency error leads to a phase shift building up over time, which reduces the motional current growth rate and maximum achievable amplitude.

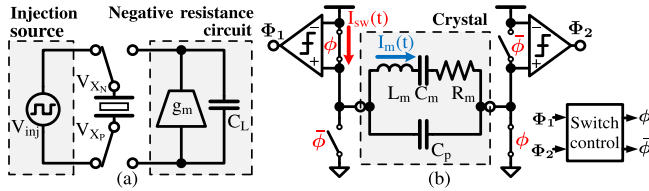


Fig. 2. (a) Energy injection concept. (b) Self-timed injection concept.

The injection source is usually a separate oscillator, with various techniques applied to achieve sufficient frequency accuracy over process, voltage and temperature (PVT) variations. Early publications attempt to calibrate the injection oscillator [15], [16]. Deliberately spreading the injection frequency over a certain bandwidth by chirping [8], [9] or dithering [14], [17], [18] guarantees crystal excitation over injection frequency variations. However, most of the energy is wasted as it is not within the crystal bandwidth. A more efficient method is to reduce the accumulated phase difference over time by injecting for a short time [19]. The resulting small crystal output voltage is then used to realigning the injection source to supply a further burst of energy once [20] or multiple times [21], [22].

Another method that does not require any precise injection oscillator is self-timed injection [23], as shown in Fig. 2(b). This technique uses comparators to detect the zero crossings of the motional branch current of the crystal, and uses this information to switch the voltage over the crystal. This ensures that the phases of  $V_{inj}$  and  $I_m$  are aligned and do not drift over time.

Regardless of the technique used for energy injection, in the most energy efficient implementations in the literature, more than 75% of the startup energy stems from driving the crystal [19], [20], [23]. Part of this energy is actually stored in the crystal oscillation, but most of it is lost. A small part of these losses stems from the switch drivers, as well as a negligible energy loss in the motional resistance. Most of the energy, however, is wasted in driving the large capacitive load at the crystal terminals, consisting of, e.g.,  $C_{Load}$ ,  $C_P$ , and parasitics.

To reduce this overhead,  $C_{load}$  can be disabled during startup [14], [23], and careful design minimizes the parasitics consisting of, e.g., on-chip and printed circuit board (PCB) traces or electrostatic discharge (ESD) protection. Nevertheless, the crystal  $C_P$  (typically in the order of pFs) is always charged and discharged at least hundreds of times during startup, wasting energy in each switching cycle.

Another way to reduce these  $CV^2$  losses is reducing the injection voltage. However, a large supply voltage is desirable, since the rate at which  $\hat{I}_m$  grows is proportional to  $V_{DD}$ , and hence startup time reduces. The drawback, however, is that the energy consumption scales with the supply voltage *squared*.

In this article, we propose a technique to reduce the energy required to drive the crystal by charging and discharging the output load in multiple steps. This technique is termed stepwise charging [24]. Furthermore, we propose improvements to the self-timed injection technique. This allows quick startup by using a large injection voltage without the associated energy

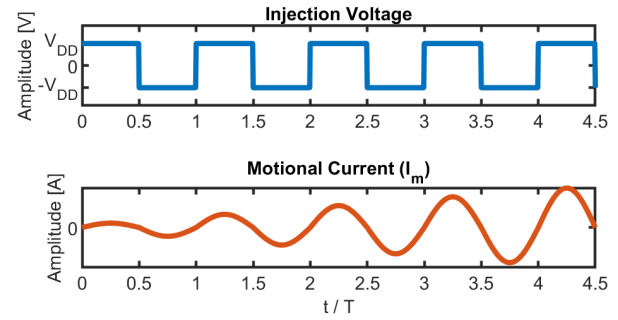


Fig. 3. Ideal energy injection waveforms [22].

penalty. Section II covers the theory of stepwise charging and its application to crystal oscillator startup. Section III covers the integration of the technique with a self-timed injection circuit, along with the improvements. Measurements on the manufactured prototype are covered in Section IV, then Section V discusses the results, and finally concluded by Section VI.

## II. CRYSTAL OSCILLATOR STARTUP WITH STEPWISE CHARGING

To achieve the injection waveforms shown in Fig. 3, both crystal terminals are alternately connected to the supply voltage and ground, as shown in Fig. 4(a). In each switch cycle, energy is injected into the crystals motional branch, consisting of  $L_m$ ,  $C_m$ , and  $R_m$ . However, each switch cycle also charges various capacitors, including  $C_P$ ,  $C_{Load}$ , and parasitic capacitances from, e.g., the PCB, ESD protection, and bondpad capacitances, as illustrated in Fig. 4(b).

This circuit can be simplified by realizing that, from a switching point of view, the motional branch can be seen as an open due to the large inductance of  $L_m$  (typically in the mH range). Furthermore, all capacitors can be lumped into two single-ended capacitances  $C_{SE}$  to ground at each terminal, as well as a differential capacitance  $C_{Diff}$ , as shown in Fig. 4(c).

Charging these capacitors costs energy. At every switch cycle (every  $T/2$ ), one of the  $C_{SE}$  is discharged and the other is charged to  $V_{DD}$ , such that an amount of charge equal to  $\Delta Q = C \Delta V = C_{SE} V_{DD}$  is drawn from the supply. Furthermore,  $C_{Diff}$  is charged from  $-V_{DD}$  to  $+V_{DD}$ , costing an amount of charge  $\Delta Q = C_{Diff} \Delta V$ , with  $\Delta V = 2V_{DD}$ . By adding the individual contributions, the energy delivered by the supply to charge  $C_{SE}$  and  $C_{Diff}$  in each *half* crystal cycle can be calculated as  $E = \Delta Q V_{DD} = (C_{SE} + 2C_{Diff}) V_{DD}^2$ .

### A. Stepwise Charging

The energy required to alternately charge and discharge a capacitor can be reduced by stepwise charging [24]. If, instead of directly charging a capacitor from 0 to  $V_{DD}$ , the capacitor is charged and discharged in  $N$  sequential steps of size  $V_{DD}/N$ , the energy consumption is reduced from  $CV^2$  to  $CV^2/N$ . This technique was successfully applied in several fields, including ADCs [25], [26], ultrasonic transceivers [27], touch-screen readout circuits [28], and class-D amplifiers [29].

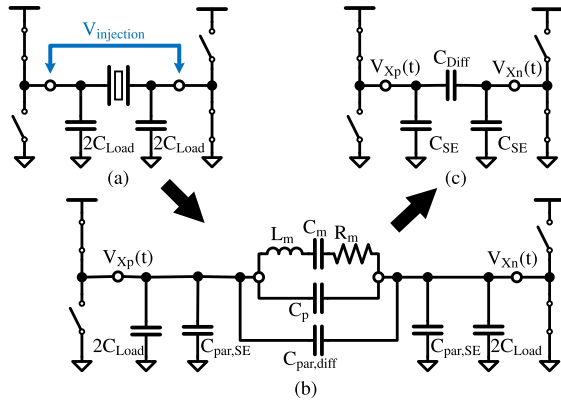


Fig. 4. (a) H-bridge. (b) Model including parasitic capacitors. (c) Equivalent model of capacitors during switch cycle.

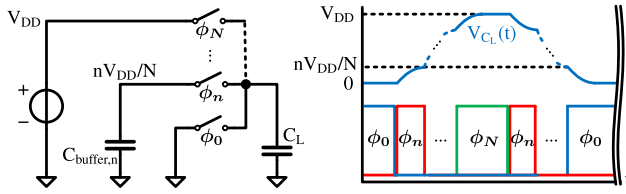


Fig. 5. Stepwise charging concept.

To understand this technique, consider a capacitor  $C_L$  that is periodically charged to  $V_{DD}$  and discharged to 0, as shown in Fig. 5. Before being fully charged to  $V_{DD}$ ,  $C_L$  is sequentially charged through each of the intermediate steps of size  $V_{DD}/N$  from (large) buffer capacitors  $C_{buffer,n}$  (with  $n = [1, N - 1]$ ), assuming they are charged to  $n(V_{DD}/N)$ . In this case, the supply  $V_{DD}$  only has to supply an amount of charge equal to  $C_L \Delta V = C_L V_{DD} N$ , which is  $N$  times less than if it would be directly charged to  $V_{DD}$ , and hence  $N$  times less energy.

If  $C_{buffer,n}$  is charged to  $n(V_{DD}/N)$ , the amount of charge on  $C_{buffer,n}$  is balanced over an entire cycle, as a packet of charge equal to  $C_L V_{DD} N$  is removed from each  $C_{buffer,n}$  every time  $C_L$  is charged, but the same amount of charge is added every time  $C_L$  is discharged.

When  $C_{buffer,n}$  is initially empty, it delivers no charge in the first stepwise charging cycle. However, a packet of charge is dumped onto  $C_{buffer,n}$  in the discharge cycle, thereby increasing the amount of charge stored on  $C_{buffer,n}$ . In this way, the voltage on  $C_{buffer,n}$  ( $V_{C_{buffer,n}}$ ) converges toward  $nV_{DD}/N$  with each consecutive cycle in what is essentially a self-stabilizing process [24]. It takes a time in the order of  $N(C_{buffer,n}/C_L)$  for  $V_{C_{buffer,n}}$  to stabilize to  $n(V_{DD}/N)$  [30].

$C_{buffer,n}$  should not be too large, as it would take a long time before  $V_{C_{buffer,n}}$  settles toward  $nV_{DD}/N$ , which would compromise energy saving in the first few cycles. On the other hand,  $C_{buffer,n}$  should be large enough ( $C_{buffer,n} \gg C_L$ ) to be able to fully charge  $C_L$  to  $n(V_{DD}/N)$  as to save a factor  $N$  in energy.

Note that the stepwise charging process requires no additional energy; no net charge is delivered by the supply, except when making the final step to  $V_{DD}$  [24]. All energy that is used to charge  $C_{buffer,n}$  is recycled from  $C_L$ , which energy would otherwise have been wasted by dumping its charge to ground.

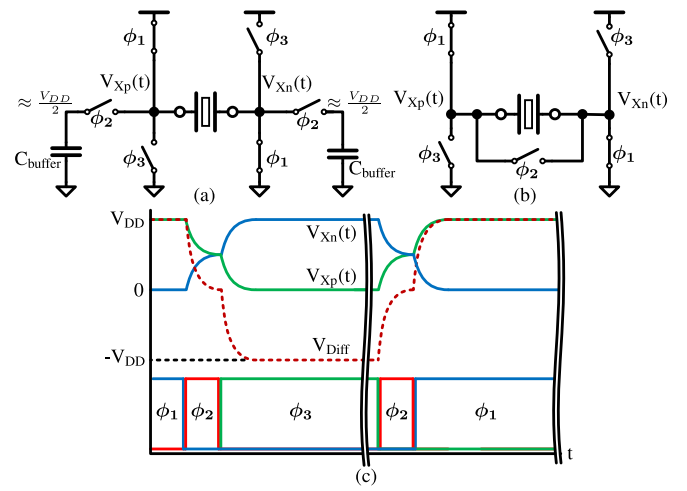


Fig. 6. (a) Two-step charging. (b) Simplified two-step charging. (c) Timing diagram.

### B. Application to XO Startup

The stepwise charging concept can be applied to crystal oscillators in several ways, since part of the capacitive load is differential and part of it is single ended, as discussed in the previous section. A few possible implementations of stepwise charging are discussed in Section II-A.

1) *Two-Step Charging*: Consider the case shown in Fig. 6(a), where the crystal is (dis)charged in two discrete time steps. The crystal node is connected to a voltage  $V_{DD}/2$  before it is connected to the supply. Applying the model shown in Fig. 4(c), the energy to charge  $C_{SE}$  can be calculated as  $E_{SE} = C_{SE} V_{DD}^2/2$ , while  $C_{Diff}$  only has to be charged from 0 to  $V_{DD}$ . This results in  $E_{Diff} = C_{Diff} V_{DD}^2$ , saving a factor 2 compared with the conventional case.

Note that in this case, one of the crystal terminals is charged, while the other is discharged, and  $C_{diff}$  is effectively short-circuited. Therefore, the schematic can be simplified to Fig. 6(b), shorting the crystal terminals by a single switch and leaving out the buffer capacitors to save switch and capacitor area for the same energy reduction.

2) *Four-Step Charging*: Although (dis)charging in two steps halves the energy consumption, the supply still has to charge  $C_{Diff}$  from 0 to  $V_{DD}$  in a step equal to  $V_{DD}$ . The energy consumption can be further reduced by increasing the number of time steps to 4, by first charging  $C_{Diff}$  to  $V_{DD}/2$ , as shown in Fig. 7.  $C_{SE}$  still experiences the same voltage steps  $\Delta V$ , and hence equal energy consumption, but the supply is charging  $C_{diff}$  only from  $V_{DD}/2$  to  $V_{DD}$ , costing only  $E_{diff} = C_{Diff} V_{DD}^2/2$ . Please note that the time that the crystal is connected to  $C_{buffer}$  is much shorter than the time that it is connected to  $V_{DD}$ .

By using stepwise charging, all energy stored in  $C_{Diff}$  and  $C_{SE}$  is redistributed before making the final step that charges either  $X_P$  or  $X_N$  toward the supply voltage. A comparison of the theoretical energy consumption using the proposed charging techniques is listed in Table I. Note that the total reduction factor for four-step charging depends on the ratio  $C_{SE}/C_{Diff}$  since a factor 2 is saved in charging  $C_{SE}$  but a factor 4 in  $C_{Diff}$ .





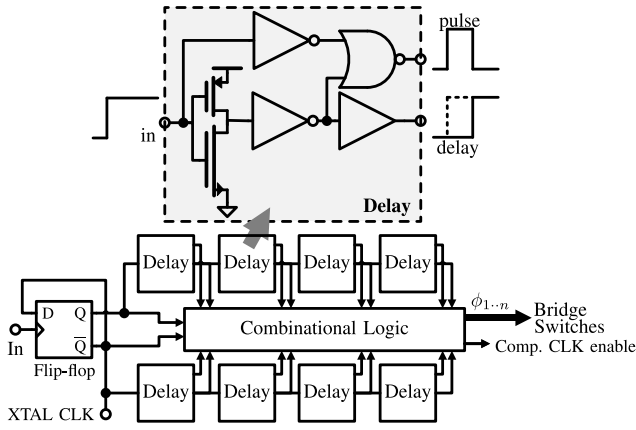


Fig. 10. Delay line block and timing diagram.

offset calibration that runs at the beginning of each startup event. Note that any residual low-frequency noise components might slightly shift the phase of the injected waveform in the beginning, but this phase error does not accumulate over time.

By tuning the body potentials of the input differential pair, the offset can be reduced [32], [33]. In this work, both comparator inputs are shorted to  $V_{DD}$  during calibration, and depending on the comparator output, using a triple-well structure, one of the body potentials is increased, such that the offset converges toward zero. The number of clock cycles for offset calibration is programmable, and is set high enough to cancel the expected worst case offset. The calibration is run every time the crystal oscillator is started as to ensure that the offset is affected by neither temperature variations nor leakage of the capacitors that store the body potential. Monte-Carlo simulation without and with offset cancellation shows a reduction of the  $1\text{-}\sigma$  offset from 7.5 mV to only 72  $\mu\text{V}$ .

### B. Delay Line

Fig. 10 shows the block diagram of the delay line. Each positive comparator decision triggers the D flip-flop, which toggles the bridge output with intermediate stepwise charging. Delay elements consisting of inverters with long channel length generate pulses and delayed signals [25], which are used to generate the non-overlapping timing signals  $\phi_{1...n}$  for the bridge through combinational logic.

### C. Bridge

Fig. 11 shows the schematic of the bridge. In addition to the switch timing, as shown in Fig. 7, large switches (“UP Fast Left” and “UP Fast Right”) to  $V_{DD}$  are briefly enabled to quickly pull up the crystal nodes before the relatively high-resistance sensing switches take over. These sensing switches are binary tunable in a binary fashion over a range of 18–600  $\Omega$  and enable measurement of the motional current  $I_m(t)$ .

The switches that connect the crystal to  $C_{buffer}$  are bootstrapped to achieve low switch resistance. The voltage at the crystal node is lower than  $V_{C_{buffer}}$  (typically  $\sim V_{DD}/2$ ) during stepwise charging, but higher during stepwise discharging.

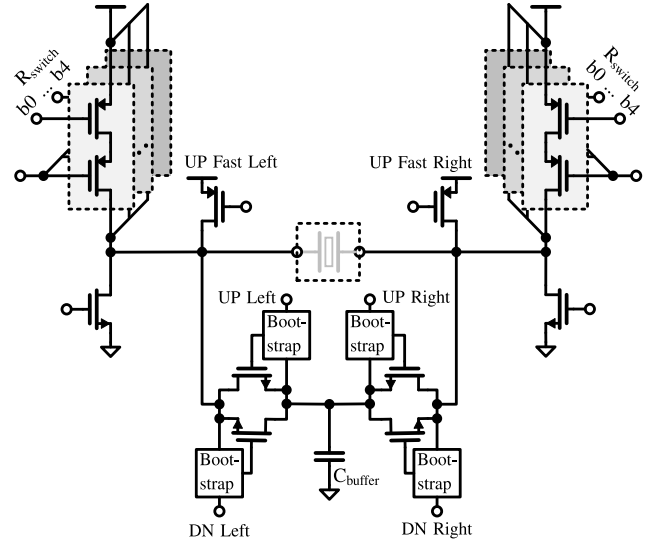


Fig. 11. Bridge schematic.

If the switch would be bootstrapped with respect to a fixed terminal this could cause the voltage over the gate oxide to become higher than  $V_{DD}$ , which could cause breakdown of the gate oxide. To prevent this, the stepwise charging switches are implemented as two pairs of bootstrapped switches that are bootstrapped with respect to  $V_{C_{buffer}}$  and the crystal nodes for the charge and discharge cycle, respectively.

The analysis on stepwise charging in Section II-B assumes full settling of the crystal node when stepwise charging and discharging. This can be achieved with very large switches, which, however, not only requires large drivers and hence increased power consumption but also introduces a significant OFF-state leakage current. This current flows through the measurement resistor, generating an offset for the zero-crossing detection of  $I_m$ . This imposed an upper limit on the switch size.

The switch size also has an influence on the energy reduction. The theoretical energy reduction calculations presented in Section III-B assume full settling to the stepwise voltages. Assuming that  $C_{buffer}$  is much larger than the capacitive loading ( $C_{buffer} \gg C_{diff}$  and  $C_{SE}$ ), the intermediate steps settle exponentially with a time constant  $\tau = R_{stepwise} C_{eff}$ , where  $R_{stepwise}$  is the resistance of the bootstrapped switches and  $C_{eff}$  is the effective capacitive load  $C_{eff} = C_{SE} + C_{diff}$  at one of the crystal terminals.

For a settling time  $t_{step}$ , when charging from 0 to  $V_{DD}/2$ , instead of reaching  $V_{DD}/2$ , only  $(V_{DD}/2)(1 - e^{-(t_{step}/\tau)})$  is reached. More charge is drawn from the supply, and the energy saving is reduced to  $1/2(1 - e^{-(t_{settle}/\tau)})$ . Suitable values for the settling time are 2–4 time constants [24].

As discussed in Section II-B,  $C_{buffer}$  should neither be too large, as it would take a long time before it is charged and energy is saved, nor too small, as it would not be able to fully charge the load. The optimum depends on the number of startup cycles, output load, and overhead, and can be found by simulation. However, the total energy consumption is only weakly dependent on the size of  $C_{buffer}$ , which is

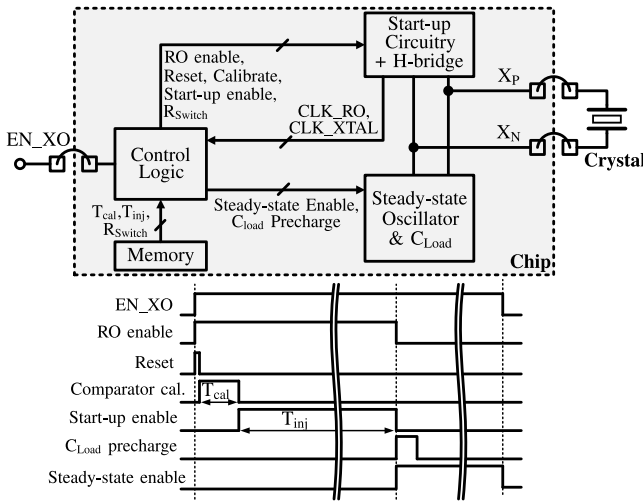


Fig. 12. Circuit block diagram and timing diagram.

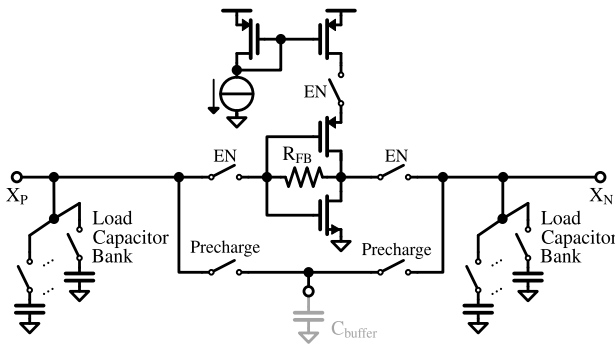


Fig. 13. Steady-state oscillator schematic.

implemented as a fixed capacitor of 137 pF in our design. For the 32-MHz crystal,  $C_{\text{buffer}}$  is charged to 90% of its final value in 20 cycles. MOS and metal-oxide-metal (MOM) capacitors are stacked on top of each other to minimize chip area. Note that the load capacitor bank can be partially reused for this purpose. MOS leakage discharges  $C_{\text{buffer}}$  with a time constant of about 17 ms. Because of the relatively long time of inactivity between successive startup events, this means that  $C_{\text{buffer}}$  is (almost) completely discharged every time the crystal oscillator is started.

#### D. Full-Chip Overview

A block diagram of the entire chip, as well as a timing diagram of the startup sequence, is shown in Fig. 12. A single enable signal starts the crystal oscillator. When this signal (EN\_XO) is enabled, the control logic block resets all timers and enables the RO. Comparator offset calibration is active for a programed amount of cycles of the RO,  $T_{\text{cal}}$ . After this, the self-timed injection startup circuitry is enabled to inject energy in the crystal. The value of  $R_{\text{switch}}$  is varied through programed values during the first 16 cycles of startup, reducing  $R_{\text{switch}}$  as the amplitude of the oscillation  $I_m$  grows. This alleviates the tradeoff between current detection sensitivity and delay encountered in [23]. After a programed amount of cycles

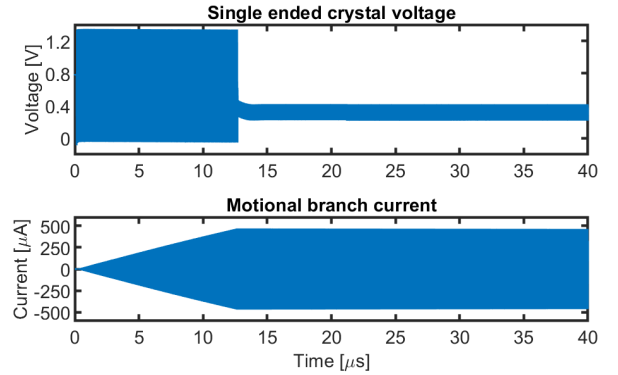


Fig. 14. Simulated waveforms for a 32-MHz crystal, injecting for 400 cycles.

TABLE II  
SIMULATED ENERGY BREAKDOWN FOR A 32-MHz  
CRYSTAL FOR 400 DRIVE CYCLES

Technique	w/o stepwise charging	Stepwise charging	
		Same $T_{\text{inj}}$	Same Amplitude
$T_{\text{inj}}$ (us)	10.36	10.36	12.66
Bridge (nJ)	7.98	4.63	5.99
Switch drivers + bootstrap (nJ)	0.20	0.48	0.59
Crystal ( $\hat{I}_m$ ) (nJ)	1.35	0.91	1.35
Capacitive load (nJ)	6.43	3.24	4.05
Startup circuits (nJ)	1.63	1.65	2.01
Total (nJ)	9.61	6.28	8.00

of the crystal, as counted from CLK\_XTAL, the steady-state oscillator is enabled.

The steady-state oscillator core is a Pierce oscillator, as shown in Fig. 13. Switches enable the bias current and (dis)connect the oscillator core to the crystal. The 31-pF load capacitor bank consists of 1-pF unit elements to accommodate crystals with various load capacitances. To reduce the time required to (dis)charge  $C_{\text{load}}$ , the output nodes are briefly connected to  $C_{\text{buffer}}$  to quickly charge these nodes to approximately  $V_{\text{DD}}/2$  when the steady-state oscillator is enabled.

#### E. Simulation Results

Fig. 14 shows transient simulation results for a 32-MHz crystal, showing swift settling to steady state after injecting energy for 400 programed cycles. Full-chip transient noise simulations over 100 different noise seeds show a worst case variation of  $\hat{I}_m(T_{\text{inj}})$  within 3.1% of its nominal value, with a  $1-\sigma$  of 1.1%. This shows that neither comparator noise nor other noise sources significantly affect the startup process. Monte-Carlo simulation over mismatch shows a variation of  $\hat{I}_m(T_{\text{inj}})$  with  $\sigma = 1.4\%$  and a worst case deviation less than 5%, which demonstrates robustness against mismatch. Simulations over process corners show, without changing any settings, less than 15% variation of  $\hat{I}_m(T_{\text{inj}})$ .

Table II shows the simulated energy breakdown, with and without stepwise charging. To simulate the case without stepwise charging, the delay line is modified to skip stepwise charging. The rest of the circuitry is identical and includes the proposed improvements to self-timed

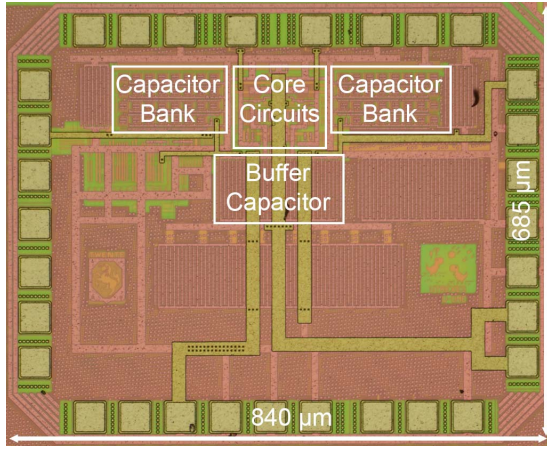
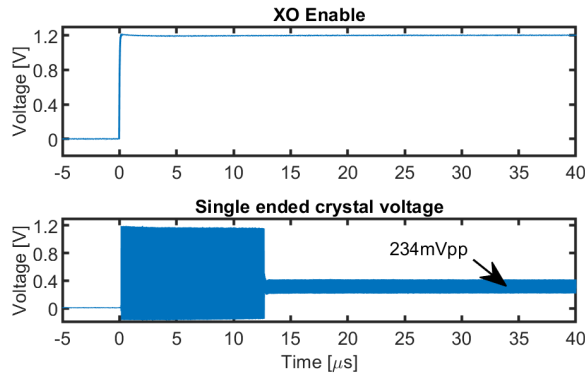
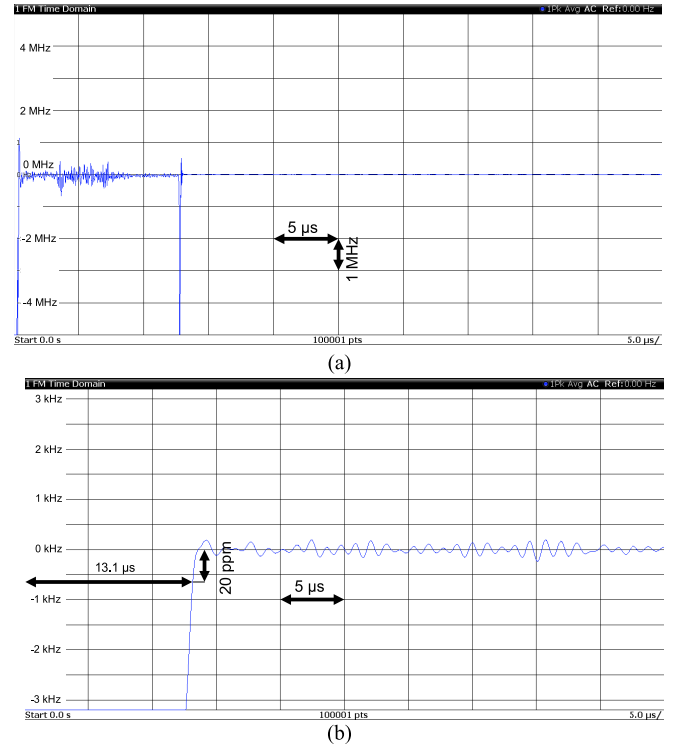


Fig. 15. Chip photograph.

Fig. 16. Measured single-ended output for a 32-MHz crystal, injecting for 400 cycles at  $T = 20^\circ\text{C}$ .

injection. The contribution of the bridge energy to the total energy consumption is divided into three parts. First is the overhead of switch drivers and bootstrap circuits. Second, the energy that is stored in the crystal calculated as  $\frac{1}{2}L_m \dot{I}_m^2$ , and lastly, the energy required to drive the capacitive load.

For an equal number of drive cycles, the capacitive losses are reduced by a factor  $> 2$ . However, the amplitude at the fundamental frequency of the injection waveform is lower than  $(4/\pi)V_{DD}$  due to the time required for stepwise charging. Therefore, for the same  $T_{inj}$ , the reached amplitude and crystal energy are lower when using stepwise charging compared with conventional injection. A larger number of drive cycles are required, to reach the same amplitude, as shown in the third column of Table II. The increased injection time costs additional energy in startup circuitry as well as more cycles of driving the capacitive load. Nonetheless, the overall energy consumption is lower when using stepwise charging. Combined with the other proposed techniques, this results in a low startup energy consumption. This work aims for minimum  $E_{start}$  and, therefore, implements the four-step charging technique. If chip area is of importance, the two-step charging technique that was proposed in Section II-B can be used instead, at the expense of saving less energy.

Fig. 17. Measured frequency settling for a 32-MHz crystal, for 400 drive cycles at  $T = 20^\circ\text{C}$ . (a) Coarse frequency scale. (b) Fine frequency scale.

#### IV. MEASUREMENT RESULTS

Fig. 15 shows a photograph of the prototype as fabricated in a 65-nm CMOS process. The chip was wirebonded to a QFN package and clamped to a PCB, on which the crystal voltages are buffered by off-the-shelf amplifiers (LTC6268) in unity-gain configuration. The circuit was tested with various crystals in the range of 24–50 MHz in various package sizes, showing reliable startup. The presented measurements are performed using a 24 MHz (TXC 7V-24.000MAAE-T), a 32-MHz crystal (Murata XRCGB32M000F2P00R0), and two different 50-MHz crystals (Abracon ABM3-50.000MHZ-D2Y-F-T and TXC 7M-50.000MAHV-T), respectively.

Fig. 16 shows the measured startup transient for the 32-MHz crystal in a  $2 \times 1.6 \text{ mm}^2$  package. At  $t = 0$ , the oscillator enable signal is triggered, and after a brief comparator calibration time of approximately 130 ns, energy injection starts. After the programed 400 drive cycles, the oscillator quickly settles to its steady state.

Fig. 17(a) shows the measured frequency settling, showing frequency variations around the fundamental frequency due to comparator noise during injection. Nevertheless, the frequency converges toward the crystal frequency as the amplitude grows. As with any injection technique, slight frequency variations are visible after switching to steady state, caused by excitation of the crystal spurious tones during injection. Assuming that a phase-locked loop (PLL) would normally filter out these spurs, the frequency settling of the fundamental tone can be measured by choosing the center frequency and demodulation bandwidth such that the spurious tones fall out of band. This measurement is shown in Fig. 17(b), showing quick settling to a frequency error less than 20 ppm.

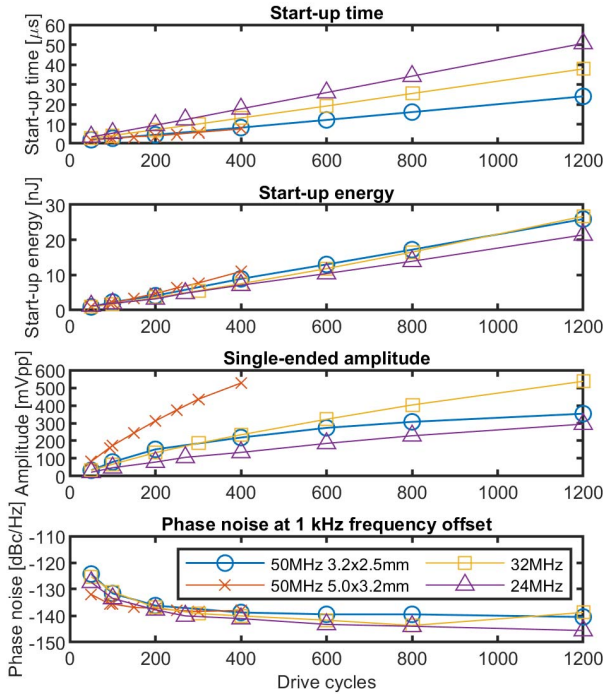


Fig. 18. Measured startup time and energy as well as steady-state amplitude and phase noise against number of drive cycles at 20 °C.

TABLE III  
MEASURED ENERGY BREAKDOWN FOR DIFFERENT  
CRYSTALS FOR 400 DRIVE CYCLES

Crystal (MHz)	$E_{\text{total}}$ (nJ)	$E_{\text{bridge}}$ (nJ)	$E_{\text{start-up}}$ (nJ)
24	4.1	3.5	0.6
32	7.1	5.3	1.8
50	7.5	5.5	2.0

Fig. 18 shows the measured performance as function of the number of programmed drive cycles for a few crystals, showing increased amplitude and improved phase noise, at a cost of increased energy consumption. Crystals in larger packages generally have a lower  $L_m$  [17], but a larger  $C_p$ . A lower  $L_m$  implies a larger slope  $d\hat{I}_m(t)/dt$ , and the required injection time to reach a given steady-state motional current  $\hat{I}_{m,ss}$  scales proportional with  $L_m$  [19]. Larger crystals, therefore, require a shorter injection time compared with smaller crystals, thereby reducing startup time. On the other hand, the increased  $C_p$  implies a larger energy consumption per injection cycle. To reach an equal output amplitude, however, the overall startup energy is lower due to the reduced injection time. Since a fixed delay is used for the generation of the stepwise charging pulses, the effective phase shift of the injection waveform is larger for higher frequency crystals. Hence, the growth in amplitude drops off faster for the 50-MHz crystal, while the amplitude growth of the 24-MHz crystal is closer to linear.

Fig. 19 shows the measured startup time and energy over temperature variations, where the settings are kept constant, except for the data points at 60 °C and higher, for which the switch resistance setting is lowered to achieve reliable startup.

The measured energy breakdown is listed in Table III, where  $E_{\text{Bridge}}$  is the energy consumed by the bridge, and  $E_{\text{Start-up}}$

TABLE IV  
PERFORMANCE OVER SAMPLES FOR A 32-MHz CRYSTAL  
FOR 200 DRIVE CYCLES

Sample	$T_{\text{start}}$ (μs)	$E_{\text{start}}$ (nJ)	Single-ended Amplitude (mVpp)	Phase noise @ 1kHz (dBc/Hz)
1	7.0	3.6	128	-139.5
2	7.2	3.5	133	-139.9
3	7.1	3.6	129	-139.4
4	7.0	3.7	125	-139.4

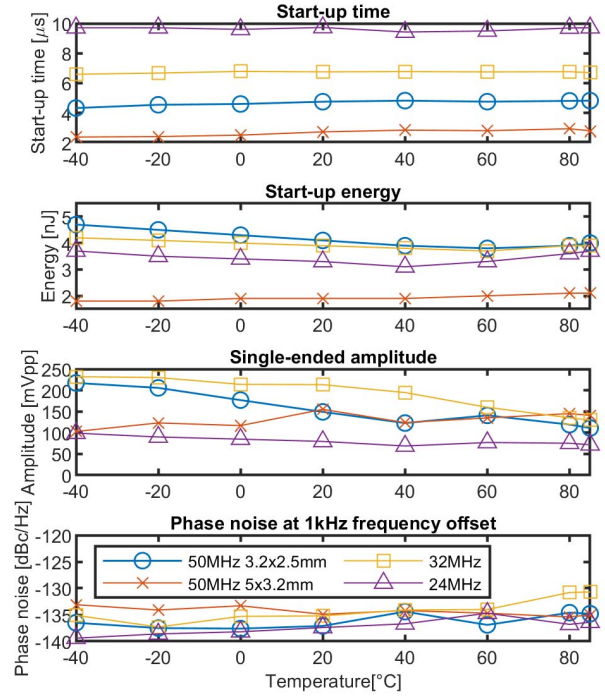


Fig. 19. Measured startup time and energy as well as steady-state amplitude and phase noise over temperature, for an injection time of 200 cycles (93 for the 50-MHz  $5 \times 3.2 \text{ mm}^2$  crystal).

comprises the energy consumption by all other blocks (startup circuitry, RO, enable logic, etc.). The number of drive cycles was set to 400 to allow comparison to the simulation results in Table II. To demonstrate robustness over samples, four different dies were tested using identical settings, except for the number of drive cycles, which was set to 200. Table IV lists the measured performance, showing a marginal variation between samples. The spread originates mostly from the steady-state settling time. To demonstrate robustness against RO frequency, performance is measured over RO bias, as shown in Fig. 20.

## V. COMPARISON

A fair comparison between different startup techniques is difficult since the startup energy is dependent on the number of drive cycles, which in turn depends on the steady-state swing,  $L_m$ ,  $C_{\text{Load}}$ , and injection amplitude. To enable fair comparison with the state of the art, the prototype was tested using the same crystal as in [19] and [23] (50 MHz). Lechevallier *et al.* [23] used a 7-pF  $C_{\text{load}}$  compared with 9 pF in [19], which resulted in a (9/7) times higher steady-state amplitude



TABLE V  
COMPARISON WITH PRIOR ART

	JSSC'19 [20]	ISSCC'19 [21]	JSSC'18 [19]	ESSCIRC'19 [12]	CICC '20 [13]	JSSC'19 [23]	This work			
CMOS process (nm)	65	55	65	65	65	22 FD-SOI	65			
Supply voltage (V)	1.0	1.2	1	1.2	1.2	0.8	1.15	1.2	1.2	1.2
Core area (mm <sup>2</sup> )	0.07	0.05	0.09	0.006	0.046	0.02	0.07			
Frequency (MHz)	54	32	50	16	20	50	24	32	50	50
Package size (mm)	N/A	N/A	5.0x3.2	N/A	N/A	5.0x3.2	3.2x2.5	2.0x1.6	3.2x2.5	5.0x3.2
Load capacitance (pF)	6	6	9	8	4	7	12	6	8	7
Differential steady-state amplitude (V <sub>pp</sub> )	0.7	0.75	0.25	0.6	N/A	0.32	0.16	0.26	0.30	0.32
Steady-state power consumption (μW)	198	N/A	195	70	169	51	19	70	36	32
Phase noise at 1 kHz offset (dBc/Hz)	-139.5	N/A	N/A	N/A	-146.6 @ 10kHz	-123	-137.4	-136.9	-136.2	-135.5
Start-up time (μs)	19	23	1.95	150	30	6	9.7	7.2	4.7	2.8
Temperature range (°C)	-40–85	-40–140	-40–85	N/A	-20–100	-40–85	-40–85			
Start-up time variation over temperature	±1%	±11%	10%	N/A	N/A	23%	3.1%	2.8%	10.3%	18.9%
Start-up time (cycles)	1026	736	98	2400	600	300	233	230	235	138
Start-up Energy (nJ)	35 <sup>†</sup>	20	9.4	10.5	11.1	3.7	3.3	3.6	4.1	1.9
Technique	2-step energy injection	Synchronized energy injection	Precisely timed injection	Negative resistance boost (NRB)	NRB + DPW injection	Self-timed injection	Self-timed injection + stepwise charging			

<sup>†</sup> ESTIMATED BY MULTIPLYING STEADY-STATE POWER CONSUMPTION AND START-UP TIME

<sup>‡</sup> INCLUDING CLOCK BUFFER POWER

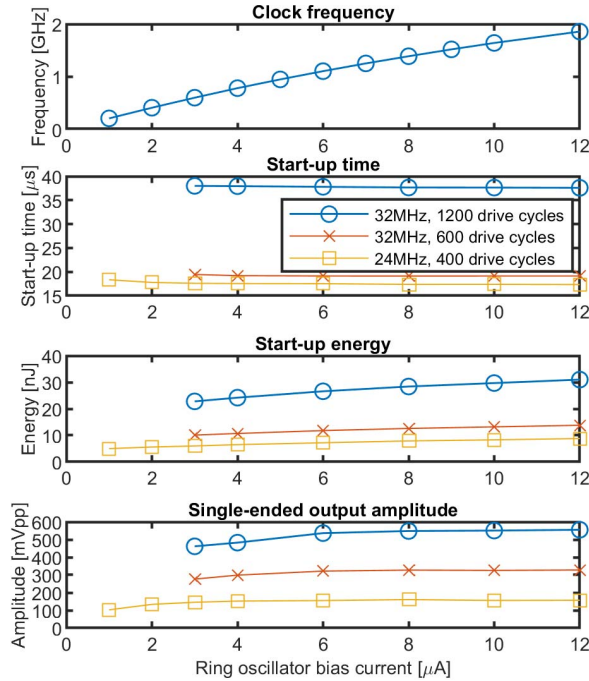


Fig. 20. Measured performance against RO bias current at 20 °C.

compared with [19], while startup was not affected since  $C_{load}$  is disconnected during startup. In this work, we used the same  $C_{load}$  and output amplitude as [23] in the measurements on the 50-MHz  $5 \times 3.2$  mm<sup>2</sup> crystal. Although this work uses 65-nm technology with a 1.5 $\times$  higher supply voltage than [23] that used 22-nm technology, startup requires almost 2 $\times$  less energy and startup is more than 2 $\times$  faster. Table V compares

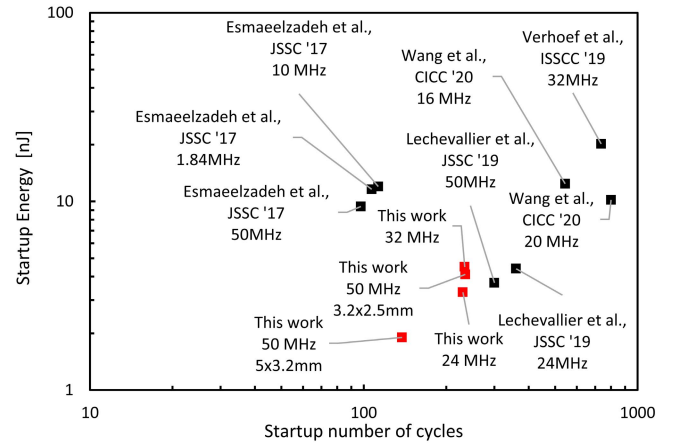


Fig. 21. Startup energy versus startup time of the state of the art.

the proposed work with the state of the art. Fig. 21 compares the startup time and energy of crystal oscillators having low startup time (<1000 cycles) and energy (<100 nJ). This work is among the lowest startup times for the lowest energy consumption.

## VI. CONCLUSION

This article presented several techniques to reduce the startup energy of crystal oscillators using energy injection. By using the concept of stepwise charging, the energy consumption associated with (dis)charging the capacitive load is reduced. In addition, the self-timed energy injection technique is improved by the use of a discrete-time, dynamic-bias comparator. This reduces energy consumption and injection delay

and allows a simple offset calibration scheme to be applied. Furthermore, the self-timed control logic with dynamic switch resistance relaxes the speed-accuracy tradeoff. Together, these techniques enable energy efficient generation of the injection signal in self-timed injection. The manufactured proof-of-concept achieves the state-of-the-art performance, starting up in just 2.8  $\mu\text{s}$  for only 1.9 nJ.

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