

A 16-Gb/s -11.6 -dBm OMA Sensitivity 0.7-pJ/bit Optical Receiver in 65-nm CMOS Enabled by Duobinary Sampling

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Abstract—High-speed, low-power optical interconnects, such as intensity modulation direct detection (IMDD) optical links, are increasingly deployed in data centers to keep pace with the growing bandwidth requirements. High-sensitivity low-power optical receivers (RXs) are the key components that enable energy-efficient IMDD optical interconnects. This article presents a low-power nonreturn-to-zero (NRZ) optical RX using a combination of a limited-bandwidth trans-impedance amplifier (TIA) and duobinary sampling to improve RX sensitivity at high data rates. Duobinary sampling leverages the well-controlled TIA inter-symbol interference (ISI) to recover the transmitted data, making it much more hardware efficient than canceling the ISI using a decision feedback equalizer (DFE). The proposed optical RX employs a CMOS-based analog front-end (AFE) to achieve high linearity and excellent power efficiency. Fabricated in 65-nm CMOS process, the prototype RX achieves optical modulation amplitude (OMA) sensitivity of -11.6 dBm at 16 Gb/s with 0.7-pJ/bit efficiency.

Index Terms—CMOS, duobinary sampling, high-sensitivity, intensity modulation direct detection (IMDD) optical links, optical receiver (RX), photodiode (PD), sense amplifiers (SAs), trans-impedance amplifier (TIA), variable-gain amplifier (VGA).

I. INTRODUCTION

LOW-POWER, high-density, low-cost, and high-speed short-reach interconnects are needed in modern hyperscale data centers. According to [1] and [2], the interconnection network consumes around 23% of the total data-center IT power consumption. Intensity modulation direct detection (IMDD) optical links are used to meet the bandwidth requirements in an energy-efficient manner [3]. Fig. 1 shows a typical high-throughput optical interconnect in which N_{CH}

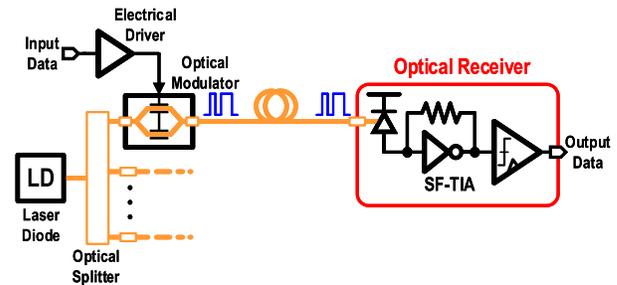


Fig. 1. High-throughput optical interconnect.

parallel IMDD optical links share a single laser diode (LD) source. Each IMDD optical link consists of an optical modulator that converts data in the electrical domain into an optical domain, an optical fiber, and an optical receiver (RX) that converts the received optical signal back into the electrical domain. Because of the low insertion loss of an optical cable, IMDD optical links can communicate over relatively long distances without increasing power consumption. While the optical fiber itself is almost lossless, imperfect optical coupling between various link components and the inefficiency associated with transmitter modulation causes signal attenuation. The minimum required LD optical power (P_{LD}) is dictated by such losses (L) and the optical RX sensitivity ($P_{RX,S}$) and can be calculated using the following equation:

$$P_{LD|dB} = 10 \log(N_{CH}) + P_{RX,S|dB} - L|dB. \quad (1)$$

From (1), we note that high-sensitivity optical RXs (small $P_{RX,S}$) help to: 1) reduce LD optical power, which is a significant source of power dissipation in an optical link, or 2) increase the number of parallel channels (N_{CH}) when the LD is operated at its maximum output power. Thus, a high-sensitivity low-power optical RX greatly enhances overall link energy efficiency. The design of such optical RXs is the focus of this article.

An optical RX consists of a photodiode (PD) followed by a trans-impedance amplifier (TIA) and a decision circuitry, as shown in Fig. 1. PD generates a current proportional to the received optical power, which is converted into a voltage by the TIA. The following decision circuitry recovers the

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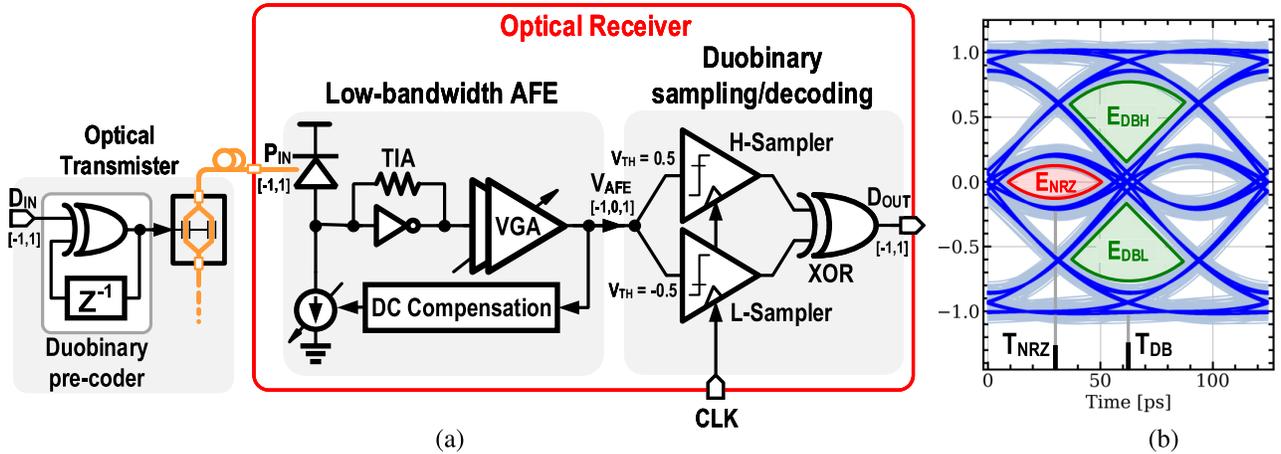


Fig. 2. (a) Proposed duobinary sampling-based optical RX. (b) AFE output eye diagram (V_{AFE}).

received data from the TIA output. TIA dictates the overall RX bandwidth and sensitivity. Shunt feedback TIA (SF-TIA) topology, compared to other architectures such as the common gate, offers better noise performance and is, therefore, most commonly used [4], [5]. However, its performance, especially at high data rates, degrades due to debilitating tradeoff between bandwidth and noise from the feedback resistor (R_F) [4]–[7]. Because TIA bandwidth must be at least 60% the data rate (9.6 GHz for 16 Gb/s) to not introduce substantial inter-symbol interference (ISI) [5], R_F must be reduced at higher data rates at the expense of increased TIA noise.

Ideally, this tradeoff can be alleviated by using an equalizer at the output of a low-bandwidth TIA [4]–[7], in which noise is reduced by increasing R_F , and an equalizer suppresses the ISI resulting from reduced TIA bandwidth. Following this line of argument, Ahmed *et al.* [5] achieved 3-dB sensitivity improvement by using TIA with a bandwidth of only 25% the data rate and a decision feedback equalizer (DFE) that incurs minimal noise penalty compared to a continuous linear equalizer (CTLE) [8]. However, implementing DFE at high data rates is challenging due to the difficulty in closing the first-tap feedback loop [9]. Speculation can alleviate the timing constraint [4], [9], but it requires additional high-speed samplers and data multiplexer that increase power/area and hardware complexity. In addition, DFE is susceptible to error propagation, especially when the first post-cursor ISI is large, which is the case with a low-bandwidth TIA [4].

Given these drawbacks, this article presents a high-sensitivity low-power optical RX using duobinary sampling in conjunction with a low-bandwidth TIA. Instead of canceling the ISI arising from the low-bandwidth TIA, duobinary sampling that leverages the well-controlled ISI [10], resulting from well-defined frequency response [11], is used to improve RX sensitivity. Low-latency feedback loops are automatically eliminated due to the duobinary data recovery; error propagation is mitigated by using simple pre-coding. Both these features allow optimization of the RX for low power. Because duobinary sampling mandates higher linearity (similar to DFE) compared to nonreturn-to-zero (NRZ) sampling, a CMOS-based analog front-end (AFE) is employed. Fabricated in a 65-nm CMOS

process, the prototype 16-Gb/s optical RX, implemented using a 4-GHz (25% data rate) bandwidth TIA, achieves a sensitivity of -11.6 -dBm optical modulation amplitude (OMA) (bit error rate (BER) $< 10^{-12}$) while consuming only 11.2 mW (0.7 pJ/bit), which represents more than $2.7\times$ energy efficiency improvement compared to [5].

The rest of this article is organized as follows. The proposed optical RX architecture is presented in Section II and its circuit implementation details are described in Section III. Experimental results obtained from the prototype optical RX test chip are provided in Section V. The key contributions of this work are summarized in Section VI.

II. PROPOSED ARCHITECTURE

A simplified block diagram of the proposed optical RX is shown in Fig. 2(a). It consists of a low-bandwidth TIA and a variable-gain amplifier (VGA), which form the AFE, followed by a duobinary sampling/decoding back end. Low-bandwidth TIA introduces significant amount of ISI, resulting in a minimal voltage margin when sampled in the middle of the output eye (E_{NRZ}) at T_{NRZ} , as shown in Fig. 2(b). Another way to recover the data is by sampling the TIA output at 0.5 UI away from the middle (at T_{DB}) using two samplers that produce a three-level signal from which the data can be recovered using a classical duobinary decoder implemented using an XOR gate, as shown in Fig. 2. In other words, low-bandwidth TIA exhibits duobinary response, $H_{TIA}(z) = 1 + z^{-1}$. The two samplers' thresholds are placed in the middle of the top and bottom duobinary eyes (E_{DBH} and E_{DBL}). While the NRZ eye (E_{NRZ}) at T_{NRZ} has a very little vertical eye opening, the duobinary eyes (E_{DBH} and E_{DBL}) at T_{DB} have a much larger vertical opening. Note that duobinary sampling leverages the well-controlled ISI at T_{DB} , instead of canceling it at T_{NRZ} as is the case in a DFE equalized RX [4]–[7]. AFE bandwidth of about one-quarter of the input data rate (25%) results in near-optimal duobinary response [12], at which point both the horizontal and the vertical duobinary eye openings are maximized [see Fig. 2(b)]. The transmitted data can be duobinary pre-coded with minimal area/power overhead [12], [13].

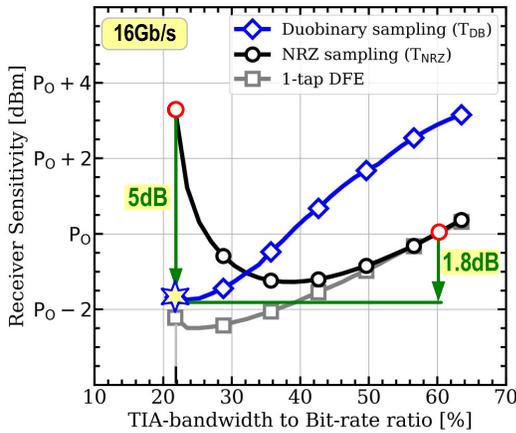


Fig. 3. Simulated RX sensitivity versus TIA bandwidth to data rate ratio.

Fig. 3 shows the simulated RX sensitivity versus TIA bandwidth to data rate ratio of the proposed duobinary sampling, conventional NRZ sampling, and one-tap DFE equalized optical RXs. In these simulations, an SF-TIA with the second-order Butterworth frequency response is used, and its two main noise contributors, namely, the feedback resistor and the feed-forward amplifier, are included. To perform fair comparison, SF-TIA design parameters are optimized for each TIA bandwidth condition such that TIA noise (\bar{i}_n^2) is minimized ($\bar{i}_n^2 \propto \text{BW}_{\text{TIA}}^3$) using design equations from [5] and [14]. The simulation results illustrate that the proposed duobinary sampling technique achieves nearly the same sensitivity improvement as a one-tap DFE when the TIA bandwidth is 25% the data rate (4 GHz for 16 Gb/s). As for the AFE, the limited bandwidth of the post-amplifiers has minimal effect on the duobinary sampling sensitivity performance as long as the overall AFE bandwidth is 25% the data rate. It is also important to note that most of the post-cursor ISIs appear in the form of the first post-cursor when the AFE bandwidth to data rate ratio is 25% [4], which makes duobinary sampling the most hardware efficient way of mitigating ISI.

III. IMPLEMENTATION DETAILS

A detailed block diagram of the proposed optical RX is shown in Fig. 4. It consists of a multi-stage SF-TIA (MS-SF-TIA) [5], a single-to-differential (S2D)-ended conversion stage, and a differential VGA, which form the AFE followed by a quarter-rate duobinary sampling back end. The RX was intended to be wire-bonded to a p-i-n PD that has 120-fF capacitance. PD input dc current is canceled with a resolution of 0.5 μA using a 7-bit current digital to analog converter (DAC) located at the TIA input. The dc offset-compensation (DCOC) loop is employed in the signal path to compensate for device mismatches. The AFE is implemented using CMOS-based amplification stages to achieve almost rail-to-rail output swing, high linearity, and low power while operating with the low supply voltage.

Duobinary sampling back end uses quarter-rate architecture. High-sensitivity samplers (HSSs) are implemented using a cascade of sense amplifiers (SAs) followed by a symmetric SR

latch [15]. High- and low-threshold voltages for the duobinary samplers (V_{THH} and V_{THL}) are generated using two 7-bit voltage DACs. Four quarter-rate clock phases are obtained from an external differential half-rate clock using quadrature divider-by-two. Phase correction circuitry is implemented to ensure the quadrature-phase spacing between the four clock phases. Circuit implementation details of the RX building blocks are discussed next.

A. Multi-Stage SF-TIA and S2D

The MS-SF-TIA schematic is shown in Fig. 5. It is implemented using a three-stage CMOS inverter-based feed-forward amplifier with a gain and a bandwidth of 30 dB and 7 GHz, respectively, and consumes 2-mW power. Assuming a total input capacitance of 180 fF, a TIA bandwidth of 4.3 GHz is achieved using an 8.8-k Ω feedback resistor (R_F). Out of 180 fF, 120 fF is assumed to come from PD junction capacitance, 40 fF from the pad and routing parasitic capacitance, and 20 fF due to TIA input capacitance. The three-stage feed-forward amplifier reduces R_F noise contribution to only 3% and helps achieve superior noise performance compared to a TIA implemented using a single-stage feed-forward amplifier [5]. The overall noise performance is dominated by the noise contribution from the feed-forward amplifier, which contributes about 65% of the total noise. R_F is implemented using a 3-bit resistor bank to tune the overall AFE bandwidth to 4 GHz (TIA + VGA) and guarantee optimum duobinary response across process and temperature variations. Fig. 6 shows the AFE pulse response at 16 Gb/s obtained from post-layout simulations, including 250-pH PD-TIA bond-wire inductance, across different process corners with and without bandwidth trimming using R_F . RX sensitivity simulation results shown in Fig. 3 were for an SF-TIA with the second-order transfer function and the implemented three-stage MS-SF-TIA whose phase margin was about 65 $^\circ$ also exhibits a similar Butterworth response.

The S2D stage converts the single-ended TIA output into a differential signal using an inverter loaded by a matched diode-connected inverter [11], as shown in Fig. 5. Unlike the dummy TIA-based S2D conversion used in [5], this implementation avoids the additional noise penalty. Furthermore, due to the limited common-mode rejection ratio of the following VGA at high frequencies, driving it with a fully differential signal results in a constant VGA output common mode, which greatly improves samplers' performance, as discussed in Section III-E. S2D simulation results show that the unity-gain complementary path introduces 1.5% total harmonic distortion (THD) for a 400-mV_{pp} 1-GHz input tone and less than 5-ps group delay until its 3-dB bandwidth (17.6 GHz) while consuming only 0.4 mW. Also, AFE simulation results show that the maximum output common-mode ripple is only 25 mV when the differential-mode output swing is 570 mV.

PD cathode terminal (PD_C) is biased using an on-chip resistor, $R_{C, \text{PD}}$, and capacitor, $C_{C, \text{PD}}$ (see Fig. 5) to couple the TIA ac ground to the PD cathode terminal. This internal PD biasing technique eliminates ground loops at the TIA input that can cause high-frequency ringing and significant degradation

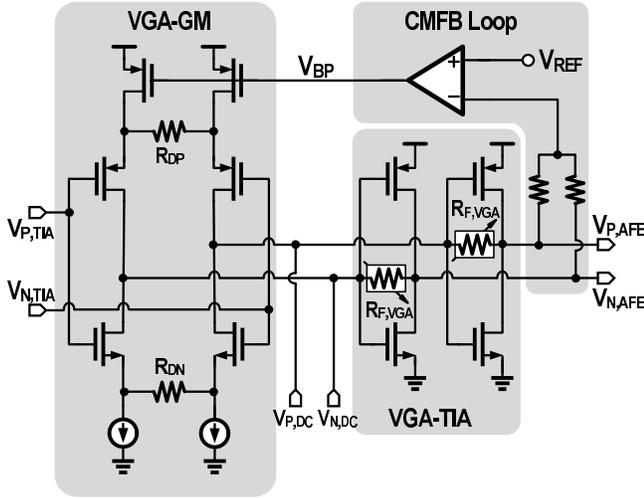


Fig. 7. Schematic of the differential VGA.

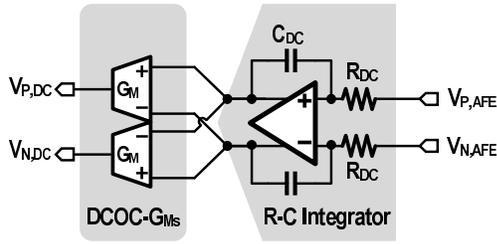


Fig. 8. Schematic of the DCOC circuitry.

voltage equal to a reference SF-TIA input common-mode voltage (V_{REF}) by controlling the VGA-GM's tail current source. VGA has a programmable gain in the range from -6 to 9.5 dB, which is achieved using a transconductance of 20 mS and a variable $R_{F,VGA}$ (250 – 1500 Ω). It is important to note that: 1) the dynamic range of the prototype RX is limited by the maximum input dc current cancellation DAC rather than by the VGA and 2) VGA noise contribution is minimal because of the high gain of the proceeding MS-SF-TIA ($R_F = 8.8$ k Ω). For best power efficiency, VGA was designed to have an output-pole dominant second-order transfer function. VGA consumes 1.6 mW and has a bandwidth of 10 GHz. Out of 1.6 mW, VGA-GM and VGA-TIAs consume 0.3 and 1.3 mW, respectively. Accounting for the 4.3 -GHz front-end TIA bandwidth, VGA causes overall AFE bandwidth to be about 4 GHz.

C. DCOC

The DCOC circuitry is shown in Fig. 8. AFE output offset voltage is sensed using a differential RC integrator and corrected by drawing unbalanced currents from the VGA-TIA inputs ($V_{P,dc}$ and $V_{N,dc}$). Two transconductance amplifiers (DCOC- G_{Ms}), implemented using current-mirror operational transconductance amplifiers (OTAs), provide the offset-compensation currents. DCOC- G_{Ms} capacitive loading has minimal impact on the VGA bandwidth because of low VGA-TIA input impedance and the output capaci-

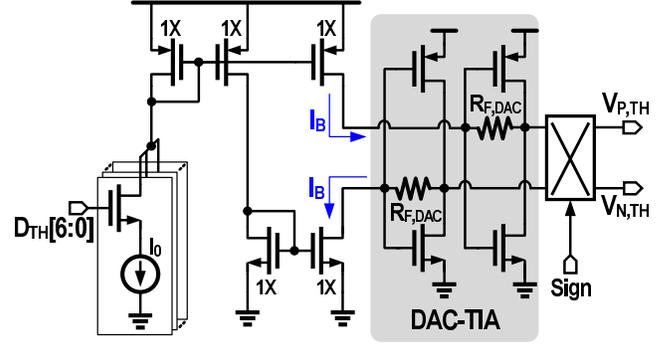


Fig. 9. Schematic of the samplers threshold generation voltage DACs.

tance of the DCOC- G_{Ms} is small compared to VGA-TIAs input capacitance. The gain–bandwidth product (GBW) of the DCOC loop is given by

$$GBW_{DCOC} \approx \frac{G_M \times R_{F,VGA}}{2\pi \times C_{dc} \times R_{dc}} \quad (2)$$

where G_M is the DCOC- G_{Ms} transconductance and R_{dc} and C_{dc} are the integrator resistance and capacitance, respectively. The DCOC loop introduces a high-pass cutoff frequency (F_C) in the AFE transfer function, which equals its open-loop GBW. F_C must be much smaller than the input data rate to avoid baseline wander or data-dependent jitter. The implemented DCOC loop has F_C of 80 kHz. It is important to note that the DCOC loop does not impact the AFE noise performance because it corrects the AFE offset at the VGA-TIAs inputs where the received signal is already amplified by the front-end TIA and the VGA-GM.

D. Samplers Threshold Generation

Threshold voltages for the duobinary slicers (V_{THH} and V_{THL}) are generated using the TIA-based differential DAC scheme shown in Fig. 9. Equal and opposite currents (I_B and $-I_B$) are drawn from two SF-TIAs (DAC-TIAs) to generate a differential output voltage ($V_{D,TH}$) with a common mode ($V_{C,TH}$) of $V_{DD}/2$. $V_{D,TH}$ can be expressed as

$$V_{D,TH} \approx 2 \times I_B \times R_{F,DAC}. \quad (3)$$

I_B is generated using a 7-bit current DAC and mirrored to the two DAC-TIAs. Fig. 10 shows the simulated TIA-based DAC output voltages ($V_{P,TH}$ and $V_{N,TH}$) along with their differential-mode ($V_{D,TH}$) and common-mode ($V_{C,TH}$) components. The threshold voltage resolution is about 2.5 mV, achieved using 5 -k Ω feedback resistor and a 7-bit current DAC, which has a unit-cell current of 0.5 μ A. DAC-TIAs are downsized replicas of the VGA-TIAs to better track AFE common-mode PVT variations, which helps sampler operation as discussed later. The threshold generation DACs' codes are set manually during measurement.

E. Duobinary Sampling and Decoding

A quarter-rate architecture is employed in the duobinary sampling back end in which each channel consists of two HSSs and an XOR gate. Each HSS is implemented using a

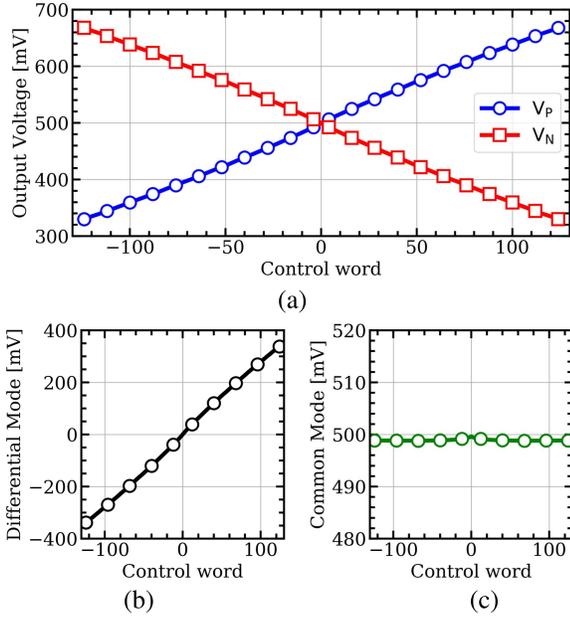


Fig. 10. Simulated TIA-based DAC's output (a) positive and negative voltages ($V_{P,TH}$ and $V_{N,TH}$) and (b) differential-mode ($V_{D,TH}$) and (c) common-mode ($V_{C,TH}$) output voltages.

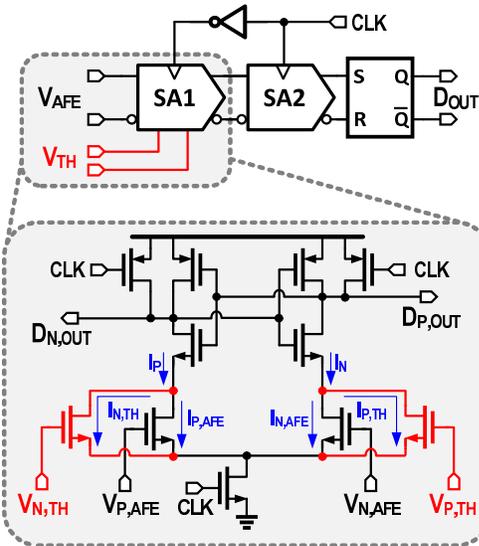


Fig. 11. Schematic of the HSS and the SA.

cascade of offset-compensated SAs (SA1 and SA2) followed by a symmetric SR latch [15], as shown in Fig. 11. Such a series combination of SAs significantly improves sampler sensitivity at the expense of half clock cycle additional latency. The first SA (SA1) is considered as a pre-amplifying stage for the second SA (SA2) for small AFE output. Note that there are no stringent timing constraints on the samplers as in the DFE case because of the feed-forward duobinary decoding. The SA schematic is also presented in Fig. 11. SA offset compensation is performed using two capacitor banks at its output. SA1 uses a differential-difference input stage to control the sampler trip point using the voltage provided by the threshold generation DACs. SA1 output trips when the positive and negative currents (I_P , I_N) drawn from its cross-coupled

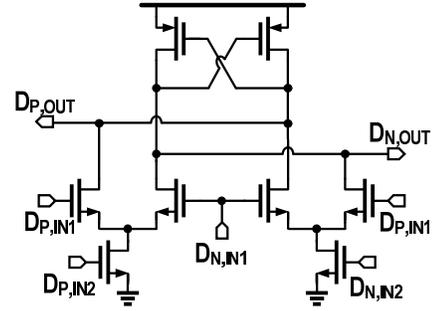


Fig. 12. Schematic of the high-speed differential XOR gate.

latch are equal. I_P and I_N are expressed as

$$\begin{aligned} I_{P|N} &= I_{P|N,AFE} + I_{N|P,TH} \\ &= \frac{k}{2} \left((V_{P|N,AFE} - V_T)^2 + (V_{N|P,TH} - V_T)^2 \right) \end{aligned} \quad (4)$$

where $V_{P|N,AFE}$ and $V_{P|N,DAC}$ are the AFE and DAC positive and negative outputs, respectively. By equating I_P and I_N from (4), the sampler differential trip point ($V_{D,AFE}$) can be expressed in terms of the AFE common-mode voltage ($V_{C,AFE}$) and DAC's differential and common-mode output voltages ($V_{D,TH}$, $V_{C,TH}$) as

$$V_{D,AFE} = V_{D,TH} \times \frac{V_{C,TH} - V_T}{V_{C,AFE} - V_T}. \quad (5)$$

Equation (5) shows that the sampler trip point ($V_{D,AFE}$) equals $V_{D,TH}$ only when $V_{C,AFE} = V_{C,TH}$. Because of the inability of the SA-based sampler in rejecting the common-mode input signal, any mismatch between common-mode voltages of AFE and DAC causes the sampler trip point to deviate from $V_{D,TH}$, as shown by (5). Due to the proposed TIA-based threshold generation DACs, common-mode voltages of DAC ($V_{C,TH}$) and AFE ($V_{C,AFE}$) are matched across PVT variations, thus resulting in a trip point condition of $V_{D,AFE} = V_{D,TH}$, as desired. More importantly, the constant AFE output common-mode voltage ($V_{C,AFE}$), resulting from driving the VGA with a fully differential signal generated by the S2D, guarantees a fixed sampler trip point ($V_{D,AFE}$) independent of the received data, thus significantly improving the RX sensitivity performance. High-speed differential XOR gate is implemented using differential cascode voltage switch logic (DCVS), as shown in Fig. 12 [17].

IV. EXPERIMENTAL RESULTS

Fig. 13 shows the complete block diagram of the implemented optical RX. The prototype RX was fabricated in a 65-nm CMOS technology and wire-bonded to an external p-i-n PD with a responsivity of 0.8 A/W and a capacitance of 120 fF. The RX occupies an active area of 0.088 mm², and its micrograph is shown in Fig. 14. The optical test setup is shown in Fig. 15. The laser output is modulated by a duobinary pre-coded data using a LiNbO₃ Mach-Zehnder modulator and coupled to the PD via a single-mode fiber. The pre-coded data was loaded to the pattern generator (Keysight M8040A). A variable attenuator is used to set the optical signal to the desired level at the PD input for sensitivity measurements.

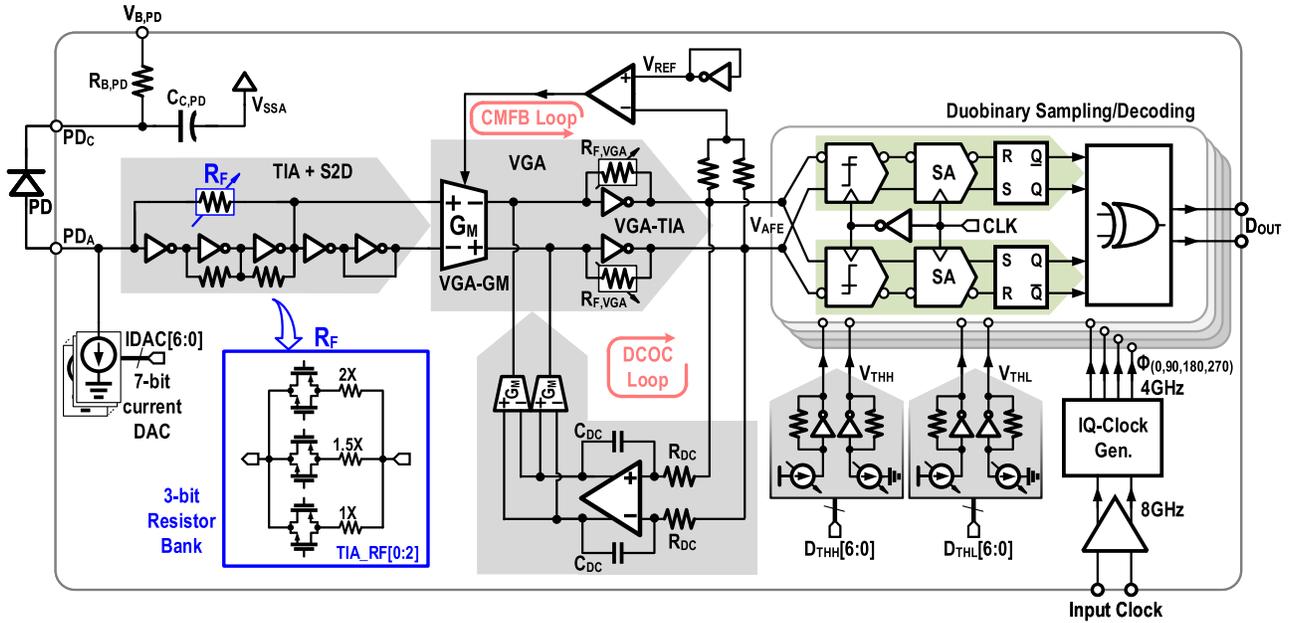


Fig. 13. Block diagram of the prototype optical RX.

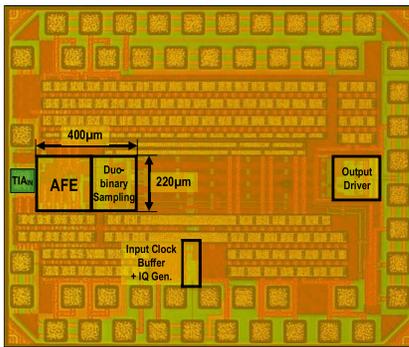


Fig. 14. Die micrograph of the prototype optical RX.

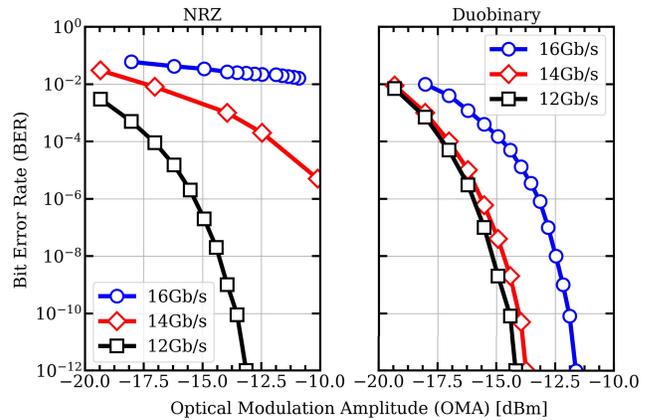


Fig. 16. Measured BER versus OMA at 12, 14, and 16 Gb/s for PRBS15 input pattern for NRZ (left) and duobinary sampling (right).

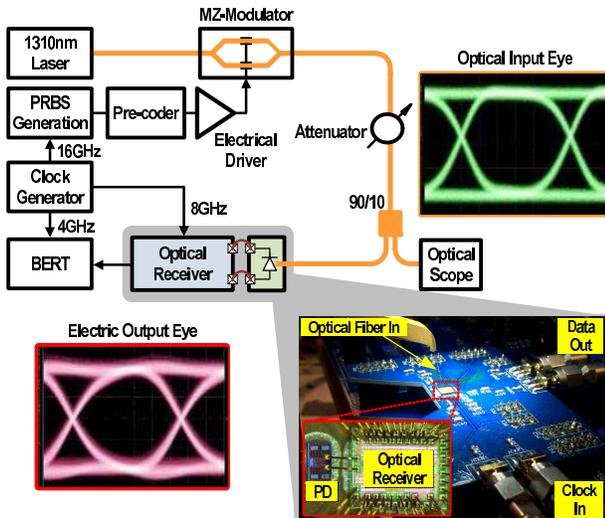


Fig. 15. Optical test setup and micrograph of the RX bonded to the external p-i-n PD.

The optical signal received by the PD is ISI free and has an extinction ratio of 10 dB (see Fig. 15).

Fig. 16 shows the measured BER performance for the proposed duobinary and conventional NRZ sampling cases.

TABLE I
RX POWER BREAKDOWN AT 16 GB/S

Building Block	Power [mW]
TIA+S2D	2.4
VGA	1.6
Samplers	6.8
Others	0.4
Total	11.2

With PRBS15 data, the RX achieves the OMA sensitivities of -14.1 , -13.7 , and -11.6 dBm at 12, 14, and 16 Gb/s, respectively, at 10^{-12} BER using the proposed duobinary sampling. However, using the conventional NRZ sampling, the error-free operation is achieved only at 12 Gb/s with the OMA sensitivity of -13 dBm. The measurement results demonstrate more than 33% data rate enhancement using the duobinary sampling compared to the NRZ sampling for the same RX AFE. Post-layout simulation results show that the maximum RX sensitivity degradation for the duobinary sampling due to

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART OPTICAL RXs

Reference	A. Cevrero [4]	A. Sharif [6]	Proesel [7]	S. Palermo [18]	M. Ahmed [5]	This work	
Technology	14-nm FinFET Bulk	65-nm CMOS	90-nm CMOS	90-nm CMOS	65-nm CMOS	65-nm CMOS	
Architecture	TIA + 1-tap DFE	TIA + IIR DFE	Res. + IIR DFE	Integrating Double Sampler	TIA + 4-tap DFE	TIA + duobinary Sampling	
Data rate [Gb/s]	64	20	9	16	12	12	16
Rx C _{in} [fF]	69	200	140	440	100	180	
PD Responsivity [A/W]	0.52	0.5	0.55	0.5	0.75	0.8	
Power [mW]	91	14.1	8.4	23	23	9.5	11.2
Efficiency [pJ/Bit]	1.4	0.705	0.93	1.43	1.9	0.79	0.7
Sensitivity OMA [dBm]	-5.5	-5.8	-5	-2.4	-16.8	-14.1	-11.6

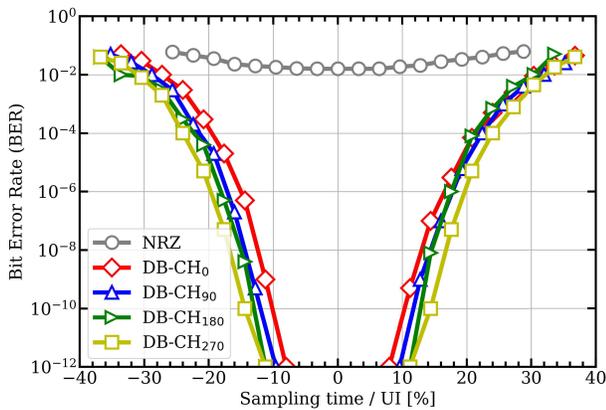


Fig. 17. Measured bathtub curves for NRZ and duobinary sampling at 16 Gb/s.

the PVT variations is 1.6 dB and occurs in the SS process corner.

Bathtub curves measured at 16 Gb/s with an input OMA of -9.6 dBm are shown in Fig. 17. The measured results show that a timing margin of 25% UI at $\text{BER} < 10^{-9}$ is achieved in all quarter-rate RX channels. The total power consumption at 16 Gb/s is 11.2 mW (0.7 pJ/bit) and the power breakdown is shown in Table I. The RX performance summary and comparison with the state-of-the-art clocked optical RXs is shown in Table II. Compared to [5], the proposed RX achieves $2.7\times$ energy efficiency improvement and roughly the same sensitivity at 12 Gb/s after accounting for $1.8\times$ less PD capacitance in [5].

V. CONCLUSION

High-sensitivity optical RXs are the key components that enable low-power operation in modern data-center interconnects. This article demonstrated a high-sensitivity low-power optical RX by using duobinary sampling in conjunction with a low-bandwidth TIA. Duobinary sampling leverages well-controlled ISI introduced by the low-bandwidth TIA, instead of canceling it, as in the case of a DFE, to improve RX sensitivity. The proposed duobinary sampling technique achieves nearly the same sensitivity improvement as a one-tap DFE when the TIA bandwidth is only 25% the data rate

(4 GHz for 16 Gb/s). A prototype of the proposed RX was fabricated in a 65-nm CMOS process and wire-bonded to a p-i-n PD. The measured OMA sensitivity at 12 and 16 Gb/s was -14.1 and -11.6 dBm, respectively, the highest reported sensitivity in 65-nm CMOS technology at 16 Gb/s with 0.7-pJ/bit energy efficiency.

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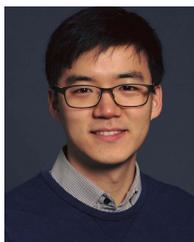
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