New Associate Editors

T IS with great pleasure that I welcome Meng-Fan Chang, Yunzhi Dong, Arun S. Natarajan, and Patrick Reynaert to the editorial board of the IEEE JOURNAL OF SOLID-STATE CIRCUITS as new Associate Editors. Chang is an expert on memories and digital circuits. Dong brings expertise in data converters and analog circuits. Natarajan is an expert in RF and mm-wave circuits. Reynaert brings expertise in THz circuits and power amplifiers.

Edith Beigne, Jonathan Chang, Azita Emami, Jeffery Gealow, and Alyosha Molnar have retired as Associate Editors. We thank them for their dedicated service to the journal.

PAVAN KUMAR HANUMOLU, *Editor-in-Chief* Electrical and Computer Engineering University of Illinois Urbana—Champaign, IL 61801 USA e-mail: jssc@illinois.edu



Meng-Fan Chang (Fellow, IEEE) received the M.S. degree from The Pennsylvania State University, State College, PA, USA, in 1996, and the Ph.D. degree from National Chiao Tung University, Hsinchu, Taiwan, in 2005.

He is currently a Distinguished Professor at National Tsing Hua University (NTHU), Hsinchu, and the Director of Corporate Research at TSMC, Hsinchu, Taiwan. Prior to 2006, he worked in industry for over ten years. This included the design of memory compilers (Mentor Graphics; 1996–1997) and the design of embedded SRAM and Flash macros (Design Service Division of TSMC; 1997–2001). In 2001, he co-founded IPLib, Taiwan, where he developed embedded SRAM and ROM compilers, flash macros, and flat-cell ROM products until 2006. His research interests include circuit design for volatile and nonvolatile memory, ultra-low-voltage systems, 3-D memory, circuit-device interactions, spintronic circuits, memristor logics for neuromorphic computing, and computing-in-memory for artificial intelligence.

Dr. Chang was a recipient of several prestigious national-level awards in Taiwan, including the Outstanding Research Award of MOST—Taiwan, the Outstanding Electrical Engineering Professor Award, the Academia Sinica Junior Research Investigator Award, and the Ta-You Wu Memorial Award. He has been serving as an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE (VLSI) INTEGRATION, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, and IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS and a Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: REGULAR PAPERS, and IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS. He has also been serving for the Executive Committee of IEDM, as well as Subcommittee Chairs of ISSCC, IEDM, DAC, ISCAS, VLSI-DAT, and ASP-DAC. He is a Distinguished Lecturer for IEEE Solid-State Circuits Society (SSCS) and Circuits and Systems Society (CASS) as well as the Chair of the Nano-Giga Technical Committee of CASS, and an Administrative Committee (AdCom) Member of the IEEE Nanotechnology Council. He has been serving as the Program Director of the Micro-Electronics Program at the Ministry of Science and Technology in Taiwan as well as the Chair of the IEEE Taipei Section, and the Associate Executive Director of Taiwan's National Program of Intelligent Electronics (NPIE) and NPIE Bridge Program.



Yunzhi (**Rocky**) **Dong** received the B.Sc. degree (Hons.) in microelectronics from Fudan University, Shanghai, China, in 2005, the M.Sc. degree (*cum laude*) in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2008, and the Ph.D. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2012.

In 2012, he joined the High-Speed Data Converter Group (HCG), Analog Devices (ADI), Toronto, ON, and later relocated to ADI's New Jersey Designer Center (NJDC), Somerset, NJ, USA, in 2015, and ADI's headquarter in Wilmington, MA, USA, in 2017. From 2012 to 2018, he developed high-speed continuous-time (CT) delta-sigma ADCs, CT MASH ADCs, and CT pipeline ADCs for 4G-LTE and 5G macrocellular base stations and broadband satellite systems. Beginning of 2019, he has been serving as a Chip Architect to lead the definition and development of ADI's direct-RF sampling transceiver platform for digital beamforming arrays, instrumentation test platforms, as well as ultra-wideband communication systems.

Dr. Dong served as a member of the Technical Program Committee of the 2017–2021 Custom

Integrated Circuit Conference (CICC) and a member of the industrial board of the 2018 International Symposium on Circuits and Systems (ISCAS). He has been an Associate Editor for the newly established IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS (OJCAS) since 2019.



Arun S. Natarajan received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Madras, Chennai, India, in 2001, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 2003 and 2007, respectively.

From 2007 to 2012, he was a Research Staff Member with IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, where he worked on millimeter-wave (mm-wave) phased arrays for multi-Gb/s data links and airborne radar and on self-healing circuits for increased yield in submicron process technologies. In 2012, he joined Oregon State University, Corvallis, OR, USA, where he is currently an Associate Professor with the School of EECS. His research focuses on RF, mm-wave, and sub-mm-wave integrated circuits and systems for high-speed wireless communication and imaging.

Dr. Natarajan was a recipient of the National Talent Search Scholarship from the Government of India (1995–2000), the Caltech Atwood Fellowship in 2001, the IBM Research Fellowship

in 2005, the 2011 Pat Goldberg Memorial Award for the best paper in computer science, electrical engineering, and mathematics published by IBM Research, the CDADIC Best Faculty Project Award in 2014 and 2016, the NSF Career Award in 2016, the Oregon State University Engelbrecht Young Faculty Award in 2016, and the DARPA Young Faculty Award in 2017. He was a Distinguished Lecturer for the IEEE Solid-State Circuits Society. He has served for the Technical Program Committee (TPC) of the IEEE International Solid-State Circuits Conference (ISSCC) and IEEE International Microwave Symposium. He serves for the TPC of the IEEE Radio-Frequency Integrated Circuits Conference (RFIC). He also served as an Associate Editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and IEEE SOLID-STATE CIRCUITS LETTERS.



Patrick Reynaert (Senior Member of the IEEE) was born in Wilrijk, Belgium, in 1976. He received the Master of Industrial Sciences in Electronics (Ing.) from the Karel de Grote Hogeschool, Antwerpen, Belgium, in 1998, and the Master of Electrical Engineering (ir.) and the Ph.D. degree (dr.) in engineering science from the University of Leuven (KU Leuven), Leuven, Belgium, in 2001 and 2006, respectively.

During 2006 to 2007, he was a Post-Doctoral Researcher with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, USA, with the support of a BAEF Francqui Fellowship. During the summer of 2007, he was a Visiting Researcher at Infineon, Villach, Austria. Since October 2007, he is a Professor with the Department of Electrical Engineering (ESAT-MICAS), KU Leuven. His main research interests include mm-wave and THz CMOS circuit design, high-speed circuits, and RF power amplifiers.

Dr. Reynaert received the 2011 TSMC-Europractice Innovation Award, the ESSCIRC-2011 Best Paper Award, and the 2014 2nd Bell Labs Prize. He is the Chair of the IEEE SSCS Benelux Chapter. He serves or has served for the technical program committees of several international conferences including ISSCC, ESSCIRC, RFIC, PRIME, and IEDM. He has served as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS and a Guest Editor for the JOURNAL OF SOLID-STATE CIRCUITS.