A 22.9–38.2-GHz Dual-Path Noise-Canceling LNA With 2.65–4.62-dB NF in 28-nm CMOS

Zhixian Deng, *Graduate Student Member, IEEE*, Jie Zhou, *Student Member, IEEE*, Huizhen Jenny Qian, *Member, IEEE*, and Xun Luo, *Senior Member, IEEE*

***Abstract*— In this article, a 22.9–38.2-GHz dual-path noise-canceling low noise amplifier (LNA) is proposed, which can achieve a low noise figure (NF) by reducing the noise of both paths. Such LNA consists of one common gate (CG) amplifier with one three-stage transformer, one resistive feedback common-source (CS) amplifier, and two amplitude-adjusting amplifiers. The three-stage transformer is used in the CG amplifier to provide gain-boosting, noise-reducing, and wideband inter-stage matching operation, simultaneously. Meanwhile, amplitude-adjusting amplifiers with reconfigurable phase-tuning lines are utilized in both paths to optimize the noise-canceling performance. To verify the aforementioned principle, a dual-path noise-canceling LNA is implemented and fabricated using a conventional 28-nm CMOS technology. The proposed LNA consumed 18.9 mW under a 0.9-V supply. The measured NF is 2.65–4.62 dB within the operating frequency range of 22.9–38.2 GHz, while the peak gain is 14.5 dB. The in-band input 1-dB compression point ($IP_{1\ dB}$) and input third-order intercept point (IIP3) are −13.2 to −6.6 and −3.6 to 3.2 dBm, respectively.**

***Index Terms*— CMOS, low noise amplifier (LNA), noise canceling, mm-wave, wireless.**

I. Introduction

THE ever-increasing demands of high-data-rate and multi-standard wireless application already push the operation band of practical wideband sub-systems (such as receiver) to mm-wave frequency. As the key component in the mm-wave wideband receiver, low noise amplifier (LNA) with low noise figure (NF) and high linearity is necessary to achieve good performance. In general, the wideband operation can be easily achieved by using the common gate (CG) [1]–[3] or cascode [4]–[7] topology. However, the CG transistor increases the NF, while the relatively high supply voltage is required in the cascode topology. Common-source (CS) LNA can provide lower NF from a low supply voltage [8], [9], which is in sacrifice of relatively narrow operation bandwidth (BW). To extend the BW of CS amplifiers, several technologies are developed, such as the feedback technique [10]–[12] and distributed topology [13]–[15]. Nonetheless, the aforementioned amplifiers still suffer from the fundamental tradeoff between wideband matching and NF, which causes a relatively large in-band NF variation.

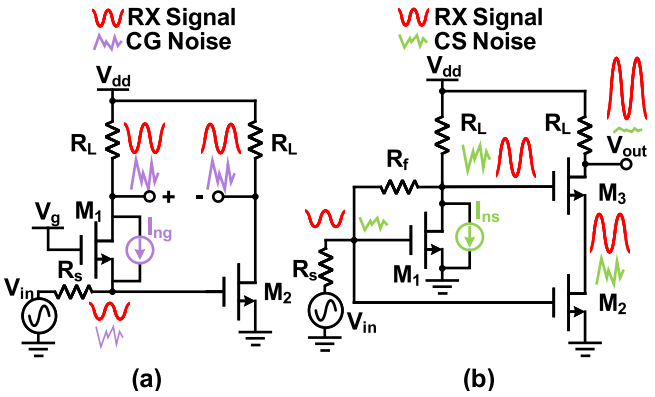


Fig. 1. (a) Configuration and operation principle of the conventional CG noise-canceling topology. (b) Configuration and operation principle of conventional resistive feedback CS noise-canceling topology.

Recent research studies show that the noise introduced by the core transistor of amplifier can be canceled, while the tradeoff between the BW and NF can be released by introducing the noise-canceling scheme to the LNA implementation [16]. Two well-known noise-canceling LNA topologies are CG noise canceling and resistive feedback CS noise canceling [17]. Fig. 1(a) shows the typical configuration and operation principle of the CG noise-canceling LNA. The noise of CG stage is replicated by an auxiliary CS stage for noise canceling at the differential output ports [18], [19]. For mm-wave application, Li *et al.* [20] presented an antenna-LNA co-design principle to implement a CG noise-canceling LNA, where the antenna can be used as a transformer to adjust the noise-canceling performance. Meanwhile, as shown in Fig. 1(b), a resistive feedback scheme can be introduced into CS amplifier for noise canceling [21]–[23]. However, it is limited to further decrease the NF since only the noise of core transistor (i.e., M_1) is reduced in either CG or CS noise-canceling topologies. By combining the noise-canceling principles in Fig. 1(a) and (b), narrow [24] and wideband [25] dual-path noise-canceling LNAs with reduced noise of both main and auxiliary paths are reported with enhanced NF performance. Nonetheless, due to the relatively large effects

Manuscript received December 1, 2020; revised April 4, 2021, May 16, 2021, and July 20, 2021; accepted July 31, 2021. Date of publication August 13, 2021; date of current version October 22, 2021. This article was approved by Associate Editor Alyosha Molnar. This work was supported in part by the National Natural Science Foundation of China under Grant 61934001 and Grant 61904025. *(Corresponding author: Xun Luo.)*

The authors are with the Center for Advanced Semiconductor and Integrated Micro-System, University of Electronic Science and Technology of China, Chengdu 611731, China (e-mail: xun-luo@ieee.org).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2021.3102602.

Digital Object Identifier 10.1109/JSSC.2021.3102602

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

of the parasitic and the interconnection, the wideband dual-path noise-canceling topology is not easy to implement in mm-wave. Therefore, the design of wideband mm-wave noise-canceling LNA with low NF remains a great challenge.

This article presents a 22.9–38.2-GHz dual-path noise-canceling LNA. The dual-path noise-canceling topology is proposed with the ability to reduce the noise in both paths. Such LNA consists of a CG amplifier, a resistive feedback CS amplifier, and two amplitude-adjusting amplifiers. A three-stage transformer is introduced in the CG stage, which can provide noise adjusting, gain boosting, and wideband matching operations. Reconfigurable phase-tuning lines are used in the amplitude-adjusting amplifiers of the proposed LNA to optimize the noise-canceling performance. Then, a dual-path noise-canceling LNA is implemented and fabricated in a conventional 28-nm CMOS technology for verification. The measured results show state-of-the-art performances in the noise figure (NF), linearity, and figure of merit (FoM). This article is organized as follows. The prototype with principle and theoretical analysis of the dual-path noise-canceling LNA is provided in Section II, while Section III presents the LNA circuit implementation. In Section IV, an LNA is fabricated, measured, and compared with the state of the arts. The conclusion is summarized in Section V.

II. Principle and Operation

Fig. 2 shows the principle and operation of the proposed dual-path noise-canceling LNA. The input signal is divided into two paths (i.e., paths I and II) at the input node of the proposed LNA. Path I consists of a CG stage, a feedback transformer (i.e., L_1 and L_2), and an amplifier A_1. Path II is formed by a resistive feedback CS stage and an amplifier A_2. After amplified by paths I and II, the input signal is recombined at the differential output. In the proposed noise-canceling LNA, the noise of both M_1 and M_2 can be reduced simultaneously. As shown in Fig. 2(a), the noise introduced by M_1 of CG stage (i.e., modeled as noise current I_{n1}) generates two out-of-phase noise voltages at its drain and source. The noise at the drain of M_1 is amplified by A_1 and then canceled at the differential output ports by its in-phase replica in path II. Meanwhile, Fig. 2(b) shows that in the CS stage, the noise introduced by M_2 (i.e., modeled as noise current I_{n2}) generates two in-phase noise voltages at its drain and gate through the feedback resistor. Those in-phase noise voltages are amplified by A_2 and path I and then canceled at the differential output as common-mode voltages. Good NF can be obtained in the proposed LNA since the noise of first-stage amplifiers (i.e., the CG amplifier and the resistive feedback CS amplifier) is reduced. Here, the feedback transformer (i.e., L_1 and L_2) provides the g_m boosting and noise-reducing functions to the CG stage, which can further reduce the noise of the proposed LNA. To clarify the aforementioned principles and guide the implementation of the proposed dual-path noise-canceling LNA, the rest of this section provides the detailed theoretical analysis of the dual-path noise-canceling scheme. Then, the effects of components values to achieve improved noise-canceling performance are discussed, while the functions of the feedback transformer and the amplitude-adjusting amplifiers are investigated.

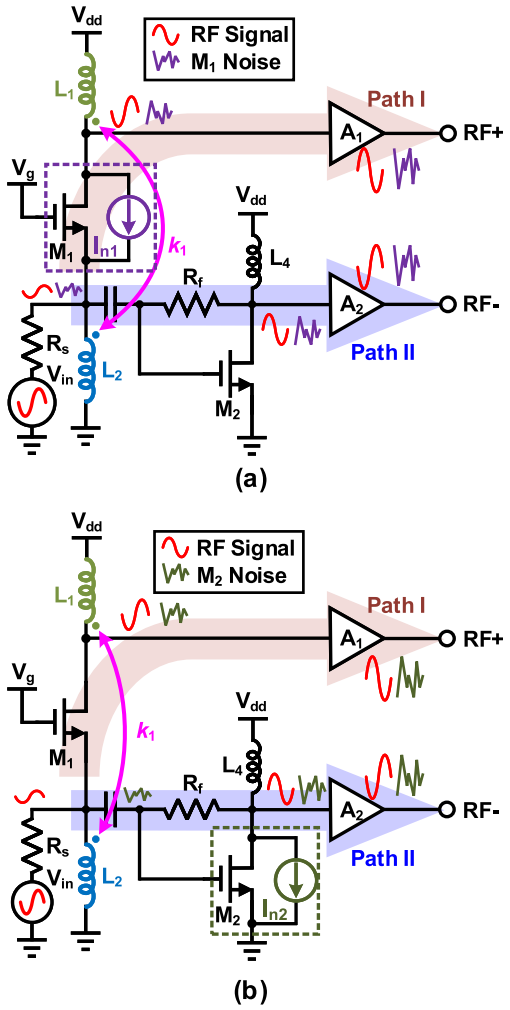


Fig. 2. Principle and operation of the proposed dual-path noise-canceling LNA. (a) M_1 noise-canceling scheme. (b) M_2 noise-canceling scheme.

A. Dual-Path Noise-Canceling Scheme

To further explain the basic operation principle of the proposed dual-path noise-canceling LNA, Fig. 3(a) exhibits the simplified schematic of the first-stage amplifier. Meanwhile, the related equivalent circuits to analyze the CG and CS noise-canceling schemes are shown in Fig. 3(b) and (c), respectively. The noise voltages (i.e., V_{X1} and V_{Y1}) generated by M_1 versus frequency can be calculated as

$$V_{X1} = \frac{Z_f Z_s I_{n1}}{Z_f + Z_s + g_{m1} Z_s Z_f + s L_4 g_{m2} Z_s} \tag{1}$$

$$V_{Y1} = \frac{-sL_1\left(Z_f + Z_s + sL_4 g_{m2} Z_s\right) I_{n1}}{Z_f + Z_s + g_{m1} Z_s Z_f + s L_4 g_{m2} Z_s} \tag{2}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively, while I_{n1}, Z_f, and Z_s can be expressed as

$$I_{n1}^2 = \frac{4kT\gamma\, g_{m1}}{\alpha} \tag{3}$$

$$Z_s = \frac{sL_2 R_s}{sL_2 + R_s} \tag{4}$$

$$Z_f = R_f + sL_4. \tag{5}$$

Here, (γ/α) is a process-bias-depended parameter [26], [27]. The noise voltage V_{X1} is inverted and amplified by the

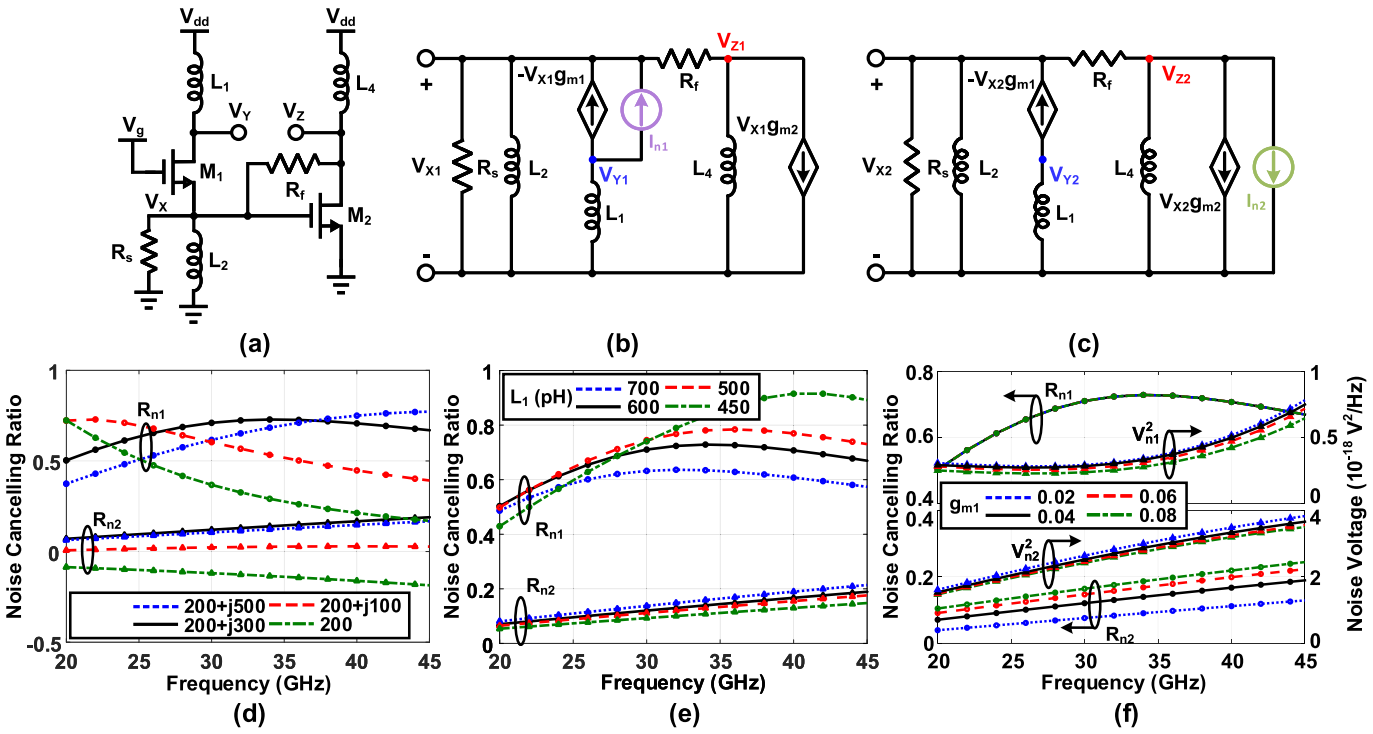


Fig. 3. (a) Simplified schematic of first-stage amplifier. (b) Simplified equivalent circuit for M_1 noise-canceling analysis. (c) Simplified equivalent circuit for M_2 noise-canceling analysis. (d) Calculated noise-canceling ratios R_{n1} and R_{n2} in different values of R_f. (e) Calculated noise-canceling ratios in different impedances of R_f. (f) Calculated noise-canceling ratios and noise voltages in different values of g_{m1}. (Source impedance $R_s = 50\ \Omega$, $L_1 = 600$ pH, $L_2 = 400$ pH, $L_4 = 600$ pH, $g_{m1} = g_{m2} = 0.04$ S, $(\gamma/\alpha) = 1$, and $R_f = 200 + j300\ \Omega$ are used in calculation, except specified in the figures.)

CS stage, which generates a noise voltage V_{Z1} and can be derived as

$$V_{Z1} = \frac{-sL_4Z_s\left(g_{m2}R_f - 1\right)I_{n1}}{Z_f + Z_s + g_{m1}Z_sZ_f + sL_4g_{m2}Z_s}. \tag{6}$$

Meanwhile, the noise current I_{n2} introduces two noise voltages V_{X2} and V_{Z2}, which are calculated as

$$V_{X2} = \frac{-sL_4Z_sI_{n2}}{Z_f + Z_s + g_{m1}Z_sZ_f + sL_4g_{m2}Z_s} \tag{7}$$

$$V_{Z2} = \frac{-sL_4\left(R_f + Z_s + g_{m1}R_fZ_s\right)I_{n2}}{Z_f + Z_s + g_{m1}Z_sZ_f + sL_4g_{m2}Z_s} \tag{8}$$

where I_{n2} is expressed as

$$I_{n2}^2 = \frac{4kT\gamma\, g_{m2}}{\alpha}. \tag{9}$$

Then, the noise voltage V_{Y2} is derived as

$$V_{Y2} = \frac{-s^2L_1L_4g_{m1}Z_sI_{n2}}{Z_f + Z_s + g_{m1}Z_sZ_f + sL_4g_{m2}Z_s}. \tag{10}$$

Here, the noise voltages of M_1 and M_2 at the differential output are obtained as (11) and (12) shown at the bottom of this page. Finally, the noise-canceling ratios R_{n1} and R_{n2} of M_1 and M_2 can be expressed as

$$R_{n1} = 1 - \frac{V_{n1}}{V_{Y1}} = \frac{L_4\left(-1 + g_{m2}R_f\right)Z_s}{L_1\left(Z_f + Z_s + sL_4g_{m2}Z_s\right)} \tag{13}$$

$$R_{n2} = 1 - \frac{V_{n2}}{V_{Z2}} = \frac{2R_f + 2Z_s + g_{m1}Z_s\left(2R_f - sL_1\right)}{R_f + Z_s + g_{m1}R_fZ_s}. \tag{14}$$

Equations (13) and (14) show that the noise-canceling performance is mainly depended on the loaded inductors (i.e., L_1 and L_4) and the transconductances of M_1 and M_2 (i.e., g_{m1} and g_{m2}). Meanwhile, the noise-canceling condition to achieve full noise canceling of M_1 and M_2 (i.e., $R_{n1} = R_{n2} = 1$) can be expressed as

$$g_{m2} = \frac{L_4Z_s + L_1\left(Z_f + Z_s\right)}{L_4Z_s\left(R_f - sL_1\right)} \tag{15}$$

$$g_{m1} = \frac{Z_s + R_f}{Z_s\left(sL_1 - R_f\right)}. \tag{16}$$

Equations (15) and (16) reveal that the noise-canceling condition of M_1 and M_2 cannot be satisfied at the same frequency. As shown in Fig. 3(d), the noise of

$$V_{n1} = V_{Y1} - V_{Z1} = \frac{s\left(L_4\left(-1 + g_{m2}R_f\right)Z_s - L_1\left(Z_f + Z_s + sL_4g_{m2}Z_s\right)\right)I_{n1}}{Z_f + Z_s + g_{m1}Z_fZ_s + sL_4g_{m2}Z_s} \tag{11}$$

$$V_{n2} = V_{Y2} - V_{Z2} = \frac{sL_4\left(R_f + Z_s + g_{m1}Z_s\left(R_f - sL_1\right)\right)I_{n2}}{Z_f + Z_s + g_{m1}Z_fZ_s + sL_4g_{m2}Z_s} \tag{12}$$

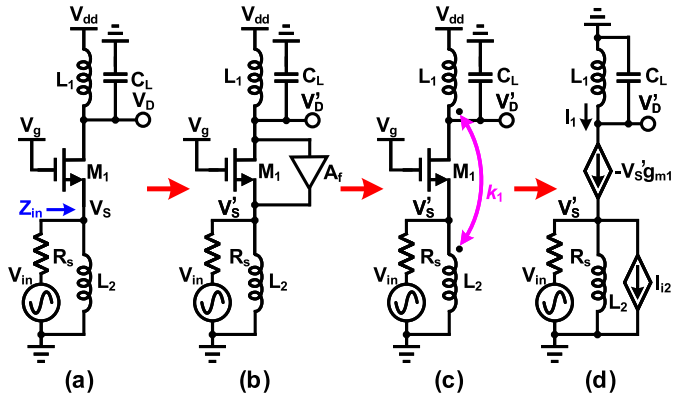


Fig. 4. (a) Conventional CG amplifier. (b) Principle of the proposed CG amplifier g_m boosting scheme. (c) Proposed transformer feedback g_m boosting scheme. (d) Equivalent circuit of the proposed g_m boosting scheme.

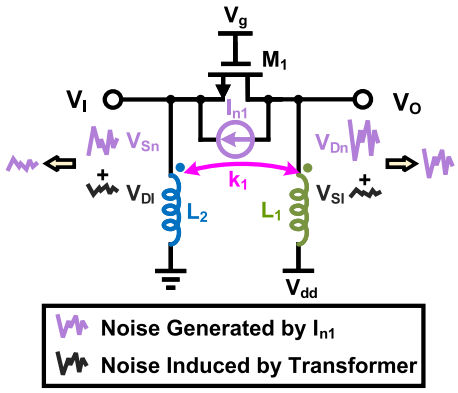


Fig. 5. Noise-reducing principle of the proposed CG stage with transformer-based positive feedback.

M_1 and M_2 can be partly canceled simultaneously. Here, the improvement of R_{n2} is limited by the implementation since the inductances (i.e., L_1–L_3) and the transconductance (i.e., g_{m1} and g_{m2}) should be allocated in a reasonable range that can be implemented at mm-wave. Meanwhile, the feedback resistor with positive image part $R_f = 200 + j300\ \Omega$ is optimized to achieved improved noise-canceling ratios, which represents that an additional inductor is used in the noise feedback path of CS amplifier (i.e., from node Z to node X) during the circuit implementation.

B. Transformer-Based g_m Boosting and Amplitude-Adjusting Amplifiers

Notice from (13) to (16) that, there is a complex tradeoff between noise-canceling ratios of M_1 and M_2. For example, Fig. 3(e) shows the tradeoff between the noise-canceling ratios of M_1 and M_2 once L_1 is varied. The aforementioned tradeoff can be released and the noise of both M_1 and M_2 can be reduced by increasing g_{m1}, while the noise-canceling ratio R_{n2} is increased without sacrificing R_{n1}, as shown in Fig. 3(f). Therefore, a g_m boosting technique is utilized in the CG amplifier.

Fig. 4(a) shows a conventional CG amplifier with capacitive load C_L, and the voltage gain can be calculated as

$$A_{\rm CG} = \frac{V_D}{V_{\rm in}} = \frac{Z_{\rm in}}{Z_{\rm in}+R_s}\frac{V_D}{V_S} = \frac{Z_{\rm in}}{Z_{\rm in}+R_s} g_{m1} Z_L \tag{17}$$

where Z_L is the load impedance, which is expressed as

$$Z_L = \frac{s^3 L_1 {C_L}^2}{1+s^2 L_1 C_L}. \tag{18}$$

As shown in Fig. 4(b), positive feedback with feedback factor A_f is introduced to the CG amplifier, and the source and drain voltages (i.e., V_S' and V_D') are changed to

$$V_S' = V_S + V_D' A_f \tag{19}$$

$$V_D' = V_S' g_{m1} Z_L. \tag{20}$$

Then, the gain of the CG amplifier and the effective transconductance of M_1 (i.e., g_{m1}') can be boosted to

$$A_{\rm CG}' = \frac{V_D'}{V_{\rm in}} = \frac{Z_{\rm in}}{Z_{\rm in}+R_s}\frac{g_{m1}}{1-Z_L g_{m1} A_f} Z_L \tag{21}$$

$$g_{m1}' = \frac{g_{m1}}{1-Z_L g_{m1} A_f}. \tag{22}$$

Such positive feedback can be implemented by the transformer consisted of L_1 and L_2, as shown in Fig. 4(c). The simplified equivalent circuit is shown in Fig. 4(d), where the effects of the positive feedback transformer can be modeled as the induced current I_{i2} [28]. The I_{i2} is expressed as

$$I_{i2} = I_1 \frac{L_m}{L_2} \tag{23}$$

where I_1 and L_m are the current flow through the inductor L_1 and the mutual inductance of the transformer, respectively, which can be calculated as

$$I_1 = \frac{-V_D'}{sL_1} \tag{24}$$

$$L_m = k_1\sqrt{L_1 L_2}. \tag{25}$$

Therefore, the source voltage of M_1 can be expressed as

$$V_S' = V_S - I_{i2}\frac{sL_2 R_s}{sL_2+R_s}. \tag{26}$$

Finally, A_f of the proposed positive feedback transformer can be derived from (19) and (23)–(26), which is expressed as

$$A_f = k_1\sqrt{\frac{L_2}{L_1}}\frac{R_s}{sL_2+R_s}. \tag{27}$$

Equation (27) shows that A_f can be adjusted by the coupling coefficient k_1. Meanwhile, the proposed transformer-based positive feedback scheme introduces a noise-reducing operation to the CG amplifier. Fig. 5 shows that the noise current I_{n1} generates a noise voltage V_{Dn} in the drain of M_1, and such noise voltage can induce a voltage V_{DI} in the secondary inductor L_2 by the electromagnetic induction of transformer. On the other hand, the noise voltage V_{Sn} generated in the source of M_1 induces a voltage V_{SI} in the primary inductor L_1. Here, the noise voltages V_{Dn} and V_{Sn} can be

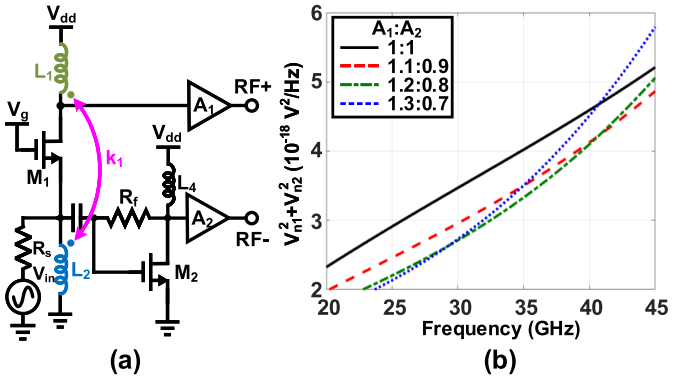


Fig. 6. (a) Configuration of the proposed dual-path noise-canceling LNA with amplitude-adjusting amplifiers A_1 and A_2. (b) Calculated output noise of the proposed LNA under the different gain ratio between A_1 and A_2. ($L_1 = 600$ pH, $L_2 = 400$ pH, $L_4 = 600$ pH, $g_{m1} = g_{m2} = 0.04$ S, $(\gamma/\alpha) = 1$, and $R_f = 200 + j300\ \Omega$ are used in calculation.)

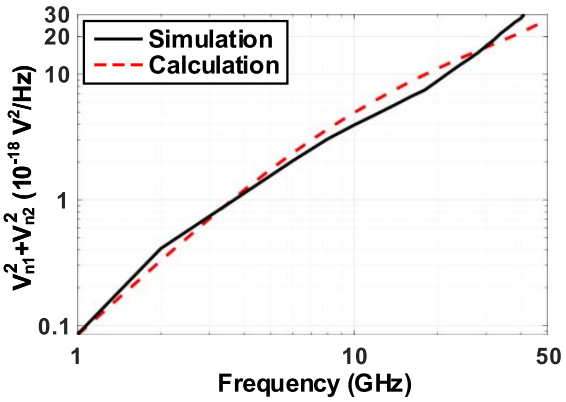


Fig. 7. Simulated and calculated noise voltage ($L_1 = 600$ pH, $L_2 = 400$ pH, $L_4 = 600$ pH, and $g_{m1} = g_{m2} = 0.04$ S are used). The process-bias-depended parameter of the utilized 28-nm CMOS technology $(\gamma/\alpha) = 4.6$ is extracted from the simulated result at 1 GHz).

partially suppressed by the out-of-phase noise voltages V_{SI} and V_{DI} [29], which can further reduce the noise of M_1.

Two amplitude-adjusting amplifiers A_1 and A_2 are introduced to optimize the noise voltages of both paths, as shown in Fig. 6(a). Assuming that such amplitude-adjusting amplifiers are ideally matched with the CG amplifier and resistive feedback CS amplifier, the gain of amplitude-adjusting amplifiers can be multiplied into the gain of both paths directly. Then, after noise canceling, the noise voltages of both paths at the differential output are expressed as

$$V'_{n1} = A_1 V_{Y1} - A_2 V_{Z1} \tag{28}$$

$$V'_{n2} = A_1 V_{Y2} - A_2 V_{Z2}. \tag{29}$$

Fig. 6(b) shows that the overall output noise can be reduced by adjusting the gain ratio of A_1 and A_2. Note that the design flexibility of the proposed LNA is improved by introducing the proposed amplitude-adjusting amplifiers since the gain of A_1 and A_2 can be easily tuned.

III. Implementation

Based on the aforementioned principles, a dual-path noise-canceling LNA is designed and implemented using a conventional 28-nm CMOS technology. As shown in Fig. 7, good agreement is achieved between simulation and calculation, which proves that (11)–(16) can be used to guide the design and components chosen. Meanwhile, due to the relatively large influence of parasitic at mm-wave, the proposed LNA should be optimized with the assistance of design tool ADS and Virtuoso. Thus, the schematic of the proposed LNA is shown in Fig. 8. The wideband input matching is mainly achieved by the CG stage with matching inductor $L_{gs} = 93$ pH, while a dc-block capacitor C_{dc} is used in the input of CS stage. The output interfaces of both paths are connected to a transformer with high common-mode rejection ratio, which can not only reduce the common-mode noise in both paths but also provide a wideband matching at the single-end output port.

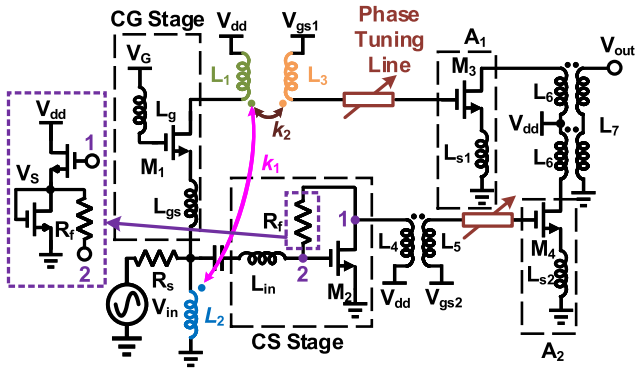


Fig. 8. Schematic of the proposed LNA.

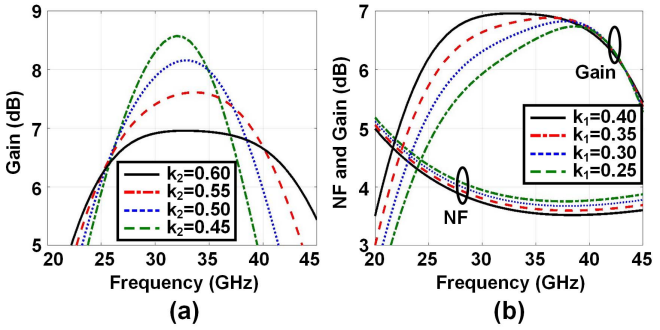


Fig. 9. (a) Simulated gain of the CG amplifier in different values of k_2. (b) Simulated NF and gain of the CG amplifier in different values of k_1 (loaded with 50 Ω).

The wideband impedance matching between CG amplifier and A_1 is achieved by the transformer consisted of L_1 and L_3. As shown in Fig. 9(a), the BW of CG amplifier is extended with the increasement of the coupling coefficient k_2 between L_1 and L_3. Meanwhile, as mentioned in Section II, a positive feedback transformer (i.e., consisted of L_1 and L_2) can provide a g_m boosting and noise-reducing operation. Fig. 9(b) shows that the gain is enhanced, while the NF is reduced with the increase of k_1. Note that the further increasement of k_1 would suffer from the instability issue since (27) shows that the positive feedback factor is dependent on the coupling coefficient k_1. Therefore, to meet the requirement of wideband

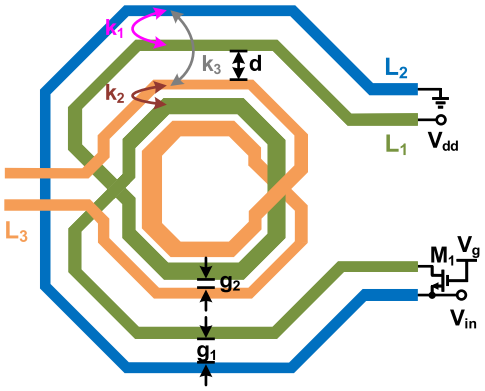


Fig. 10. Layout of the proposed three-stage transformer.

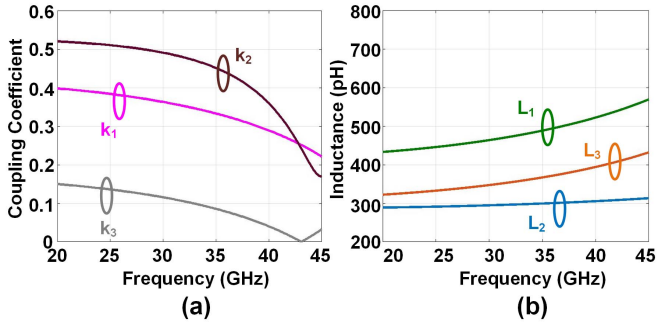


Fig. 11. Simulated results of the proposed three-stage transformer. (a) Coupling coefficients. (b) Inductances.

interstage matching of path I and the positive feedback of CG amplifier, a three-stage transformer is utilized where the inductor L_1 is reused in the positive feedback transformer (i.e., consisted of L_1 and L_2) and the inter-stage matching transformer (i.e., consisted of L_1 and L_3). The layout of the proposed three-stage transformer in CG amplifier is shown in Fig. 10, and the stepped-impedance inductors L_1 and L_3 are used to improve the quality factor [30]. The coupling k_1 is depended on the gap (i.e., g_1) between the L_2 and outer coil of L_1, while the gap g_2 between L_3 and inner coil of L_1 affects the coupling coefficient k_2. Here, the coupling between L_2 and L_3 (i.e., k_3) is undesired, which will decrease the stability of CG amplifier.

Thus, the distance between the inner and outer coils of L_1 (i.e., d) is broadened to reduce the coupling k_3. The simulated inductances and coupling coefficients of the proposed three-stage transformer are shown in Fig. 11, which reveals that the unwanted coupling k_3 is negligible. To further improve the gain of CG stage, a gain-peaking inductor L_g can be used in the bias circuit of M_1 [31]. Here, the gain is increased with L_g, which would lead to higher in-band ripple and lower stability [32]. In the proposed LNA, $L_g = 150$ pH is utilized to achieve the optimized performance.

As mentioned in Section II, an additional inductor is provided in the noise feedback path of CS amplifier for enhanced noise-canceling response. Therefore, an inductor L_{in} is used in the CS amplifier, as shown in Fig. 8. Meanwhile, such inductor is in series connected between the dc-block capacitor

TABLE I

L AND Q OF THE INDUCTORS AND TRANSFORMERS AT 28 GHZ

Device	L_{in}	L_g	L_{gs}	L_{s1}	L_{s2}	L_1	L_2	L_3
L (pH)	300	150	93	105	130	455	293	340
Q	18.5	18.8	17.4	17.9	18.4	14.6	19.2	15.3
Device	L_4	L_5	L_6	L_7				
L (pH)	396	320	243	163				
Q	16.4	15.8	10.6	15.2				

and the gate of M_2, which can further improve the voltage gain of CS amplifier by resonating with the parasitic capacitance of M_2. In the proposed LNA, $L_{\text{in}} = 300$ pH is utilized to achieve the optimized NF and gain performance. As shown in Fig. 8, a source follower buffer with a fixed current source is introduced in the feedback resistor chain. Such buffer releases the tradeoff between gain and NF performance [33], while an optimized bias voltage of M_2 can be generated by tuning the transistor size of the buffer. Then, the output of CS amplifier is a transformer-based wideband inter-stage matching network, which is connected to the amplitude-adjusting amplifier A_2. Here, the amplitude-adjusting amplifiers A_1 and A_2 at paths I and II are used to further improve the noise-canceling performance of the proposed LNA, as mentioned in Section II. In the proposed LNA, both A_1 and A_2 are implemented in the CS topology with a source degeneration inductor. Once the transistors sizes are determined, the gains of A_1 and A_2 are depended on their bias (i.e., V_{gs1} and V_{gs2}) and the source degeneration inductors (i.e., L_{s1} and L_{s2}). As shown in Fig. 12(a) and (b), the NF and gain of the proposed LNA is varied with the inductance of L_{s1} and L_{s2}. In the proposed LNA, the performance degeneration caused by the PVT variation can be calibrated by the phase-tuning lines [34] in the inter-stage matching networks of both paths, and the detailed discussion is given in Appendix A.

Compared to the previously reported wideband LNA with dual-path noise-canceling scheme operate at 1–20 GHz [25], inductors, transformers, and g_m boosting technique are used in the proposed LNA to achieve better gain and NF at higher frequency. Meanwhile, the amplitude-adjusting amplifiers provide additional design flexibility to achieve high performance at mm-wave. Thus, the dual-path noise-canceling LNA is designed and implemented based on the aforementioned principles and structures. The inductance and quality (Q) of the implemented inductors and transformers are given in Table I, while the bias voltage of M_2–M_4 (i.e., V_S, V_{gs1}, and V_{gs2}) is generated by the fixed on-chip circuits. Note that good robustness is achieved in the proposed LNA under bias variation, the related simulated results, please refer to Appendix B. The simulated result in Fig. 13(a) shows that the wideband operation of the proposed LNA is achieved by combining two paths with wideband response, while the noise of both paths can be reduced simultaneously. The relatively large in-band ripple is mainly because the inductance of source degeneration inductor L_{s1} and gain-peaking inductor L_g is chosen to achieve improved NF and BW, as shown in Fig. 12(a) and (c).

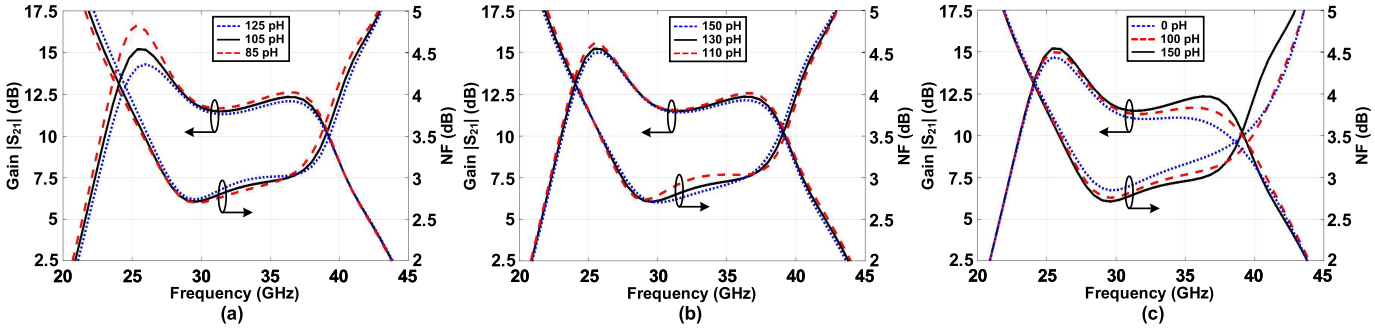


Fig. 12. Simulated gain and NF of the proposed dual-path noise-canceling LNA in different values of (a) L_{s1}, (b) L_{s2}, and (c) L_g.

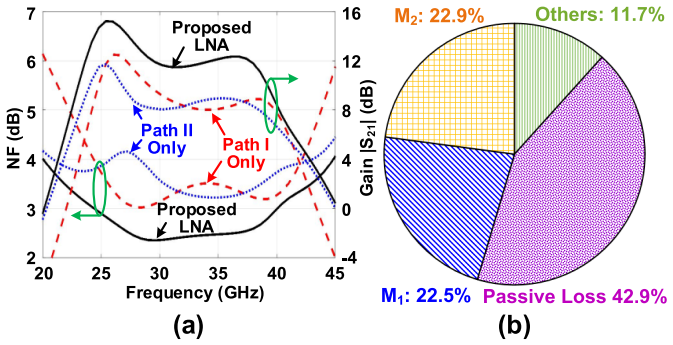


Fig. 13. (a) Simulated NF and gain of both paths and the proposed LNA. (b) Simulated noise contribution of the proposed LNA at 28 GHz.

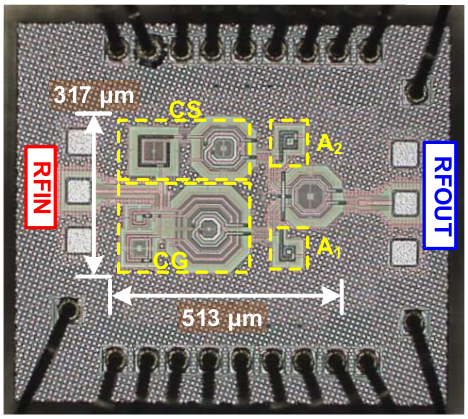


Fig. 14. Chip micrograph of the fabricated dual-path noise-canceling LNA.

Fig. 13(b) reveals that the noise contributed by M_2 is a bit larger than the noise contributed by M_1. Here, the noise contributed by M_1 and M_2 includes the current noise and the thermal noise of parasitic resistors. Meanwhile, the loss (i.e., Q) of passive components (i.e., transformers, inductors, capacitors, and interconnections) in the proposed LNA is the main reason for NF degeneration. The noise introduced by A_1, A_2, feedback resistor R_f, and bias circuits are summarized as other noise plotted in Fig. 13(b).

IV. Measurement and Comparison

Fig. 14 shows the chip micrograph of the fabricated dual-path noise-canceling LNA. The chip occupies a core area

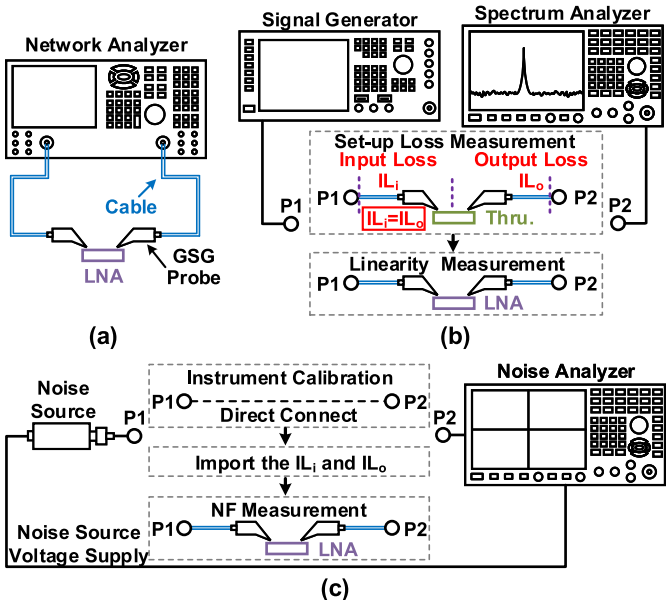


Fig. 15. (a) S-parameters measurement setup. (b) Linearity measurement and calibration setup. (c) NF measurement and calibration setup.

of 317 × 513 μm^2 while consuming 18.9 mW from a 0.9-V voltage supply. As shown in Fig. 15(a), the S-parameters measurement is performed by the network analyzer N5230A, while an SOLT de-embedding technology is used for the on-chip test calibration. Meanwhile, to measure the linearity of the proposed LNA, signal source SMW200A and spectrum analyzer FSW43 are used. A through (Thru.) line with negligible insertion loss is used to short the two probes, as shown in Fig. 15(b), and then, the total loss of the measurement setup (i.e., the combined loss of the probes, cables, and connectors) is obtained. Due to the symmetrical configuration, the input and output losses (i.e., IL$_i$ and IL$_o$) of the test setup can be calculated by half of the total loss. After de-embedding the loss of the setup, the linearity of the proposed LNA can be measured. To measure the NF of the proposed LNA, the spectrum analyzer FSW43 (with noise analyzer function) and noise source 346CK40 are used. The noise analyzer provides a calibration procedure that can calculate the NF of the proposed LNA after de-embedding the input and output losses of the test setup. The NF measurement is performed by the following three steps [35], as shown in Fig. 15(c): 1) the noise source is directly connected to the noise analyzer

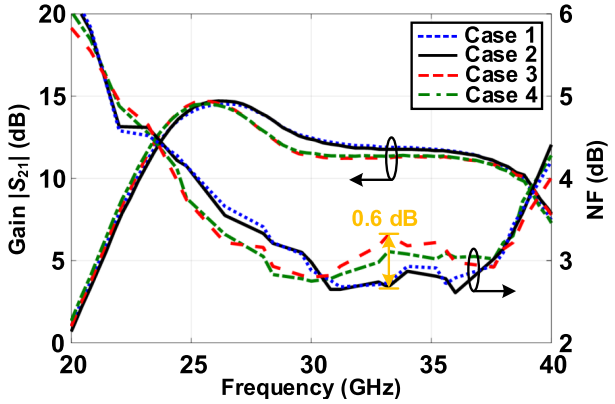


Fig. 16. Measured NF and gain of the proposed LNA under different setting cases of the phase-tuning lines. Case 1: all the switchable capacitors in both paths are switched OFF. Case 2: all the switchable capacitors in path II are switched ON. Case 3: all the switchable capacitors in path I are switched ON. Case 4: all the switchable capacitors in both paths are switched ON.

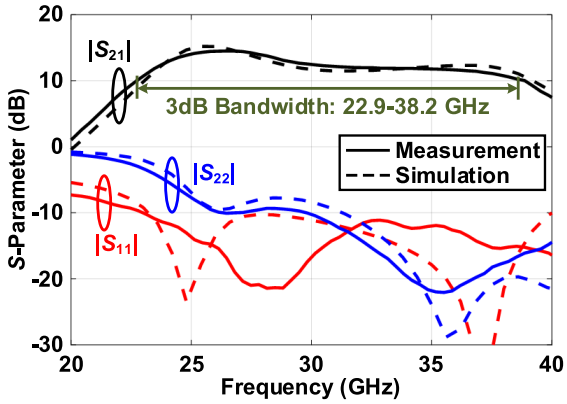


Fig. 17. Measured and simulated S-parameters of the proposed dual-path noise-canceling LNA (case 2).

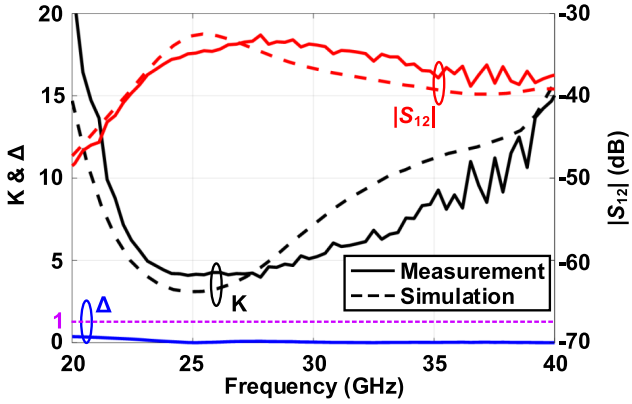


Fig. 18. Measured and simulated reversed isolation S_{12}, stability factor K, and Δ (case 2).

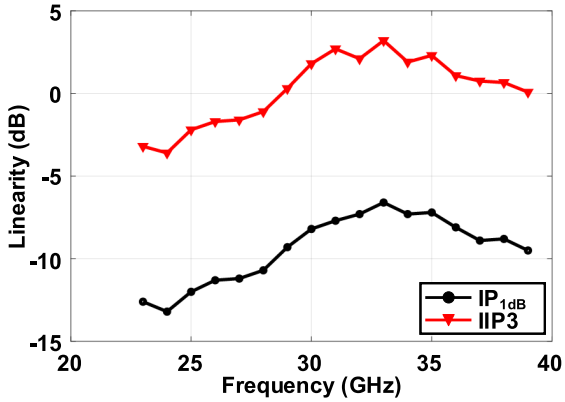


Fig. 19. Measured linearity of the proposed dual-path noise-canceling LNA (case 2).

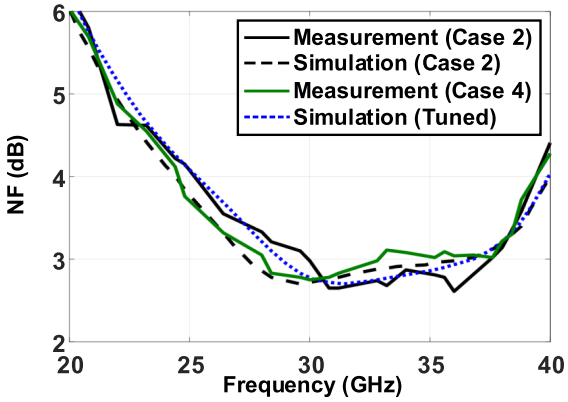


Fig. 20. Measured and simulated NF of the proposed LNA. Setting of simulation (tuned): reduce the input parasitic capacitance of M_3 (−6 fF).

for instrument calibration; 2) importing the input and output losses of the setup (i.e., IL_i and IL_o) to the noise analyzer, where the required IL_i and IL_o are obtained during the linearity measurement; and 3) measured the NF of the proposed LNA directly. During the measurement, the phase-tuning lines are adjusted by an off-chip digital control unit, while the bias voltage V_G is tuned to achieve optimized performance.

Fig. 16 shows the measured gain and NF of the proposed LNA under different settings of phase-tuning lines, which reveals that the maximum NF variation range is about 0.6 dB. The measured S-parameters in Fig. 17 show that the maximum gain of the proposed LNA is 14.5 dB at 26 GHz, while the 3-dB BW is 22.9–38.2 GHz. S_{11} is lower than −10 dB within the operating frequency range. Note that the bias and phase settings in simulation are the same with measurement. Meanwhile, Fig. 18 exhibits that the reversed isolation of the proposed LNA is lower than −30 dB in the operation band, and then, the stability factor K can be calculated from the measured data

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{30}$$

where the auxiliary condition Δ is expressed as

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}|. \tag{31}$$

The conditions $K > 1$ and $\Delta < 1$ are satisfied in full operation band, as shown in Fig. 18, which means that the proposed LNA is unconditionally stable in any source and load VSWR [36]. As shown in Fig. 19, the measured input 1-dB compression point ($IP_{1\ dB}$) and input third-order intercept point (IIP3) are −13.2 to −6.6 and −3.6 to 3.2 dBm, respectively. Similar to other multi-path-combined type amplifier,

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART LNAS

Ref.	RFIC 2016 [4]	MWCL 2018 [5]	RFIC 2019 [6]	RFIC 2019 [7]	IMS 2019 [9]	JSSC 2020 [12]	ISSCC 2020 [20]	TMTT 2020 [25]	**This Work**
Technology	40-nm CMOS	40-nm CMOS	65-nm CMOS	22-nm FDSOI	65-nm CMOS	22-nm FDSOI	45-nm CMOS SOI	65-nm CMOS	**28-nm CMOS**
Topology	Cascode	Cascode	Cascode	Cascode	CS	CS	NC*	D.-P. NC◇	**D.-P. NC◇**
Frequency (GHz)	48–61	26–33	24.9–32.5	24–43	24	22–32#	73–88	1–20	**22.9–38.2**
3-dB BW (GHz)	13	7.4	7.6	19	3	17	15	19	**15.3**
NF (dB)	3.6–4.4	3.3–4.3	3.25–4.20	3.1–3.7	3.4	1.7–2.2	4.8–6.1	3.3–5.3	**2.65–4.62**
Gain (dB)	15	27.1	18.3	23	23.5	21.5	12.8	16.8	**14.5**
IP_{1dB} (dBm)	N/A	−21.6	−24	−27–−20.4	−14+	N/A	−9.2–−7.4	−13–−8	**−13.2–−6.6**
IIP3 (dBm)	−15	−12.1	N/A	−19–−13.2	−7	−13.4	0.4–2.2	5.8	**−3.6–3.2**
Power (mW)	20.4	31.4	20.5	20.5	12	17.3	46	20.3	**18.9**
Core area (mm^2)	0.19	0.26	0.11	0.22	0.13	0.05	0.63**	0.096	**0.16**
FoM_1	N/A	0.74	0.09	1.62	1.88	N/A	1.41	2.48	**5.94**
FoM_2	−21.13	−10.78	N/A	−4.41	−4.03	0.94	5.36	22.70	**20.57**

* Noise-cancelling. ◇ Dual-path noise-cancelling. # Gain is within the 3-dB BW and $|S_{11}| < -10$ dB. + Estimated from the curves.
** With on-chip antenna.

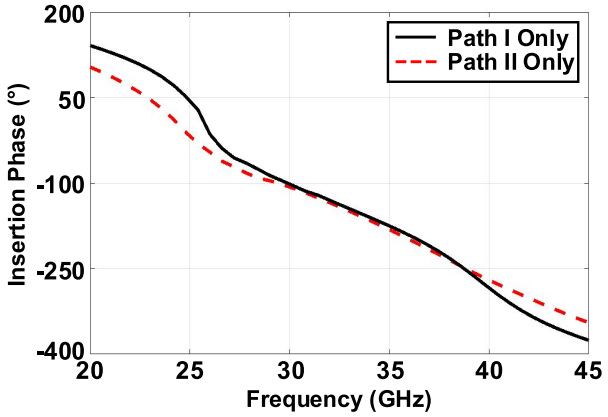


Fig. 21. Simulated insertion phase of the proposed LNA with only paths I and II.

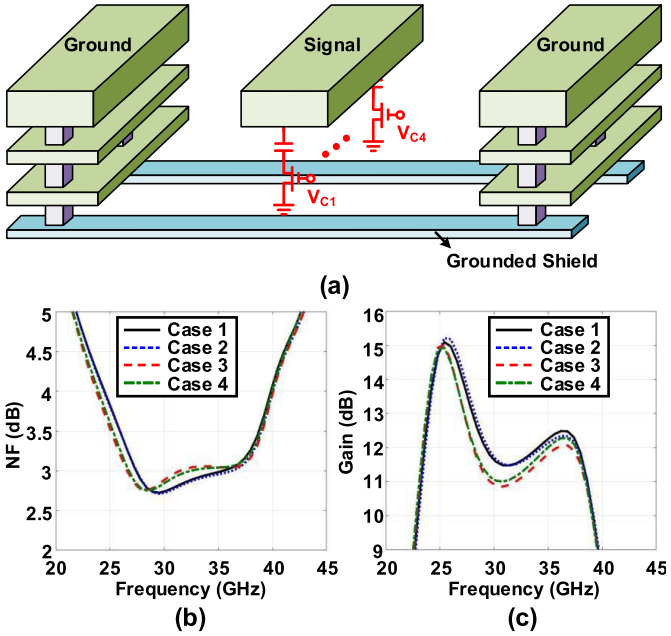


Fig. 22. (a) Configuration of the phase-tuning line with four switchable capacitors. (b) Simulated NF under different setting cases of phase-tuning lines. (c) Simulated gain of the proposed LNA under different setting cases of the phase-tuning lines. (Phase setting in different cases, please refer to the caption of Fig. 16.)

good linearity is achieved in the proposed LNA due to the dual-path topology.

Fig. 20 shows that the measured NF is 2.65–4.62 dB within the frequency range of 22.9–38.2 GHz. Compared to simulation, the measured NF response exhibits a slight frequency shifting to higher frequency. Such variation can be calibrated using the phase-tuning lines by the following procedures: 1) figure out the performance variation trends in different simulation settings and 2) compared the measured and simulated results and then change the phase setting of phase-tuning line following the trends obtained in step 1. For example, as shown in Fig. 20, similar frequency shifting can be obtained in simulation once the input capacitance of M_3 is reduced. Therefore, by tuning the phase setting to case 4 (increases about 7-fF input capacitance of M_3), the measured NF can be matched to the simulation.

Table II shows the performance summary and the comparison with state-of-the-art LNAs. Here, FoM FoM_1 and FoM_2

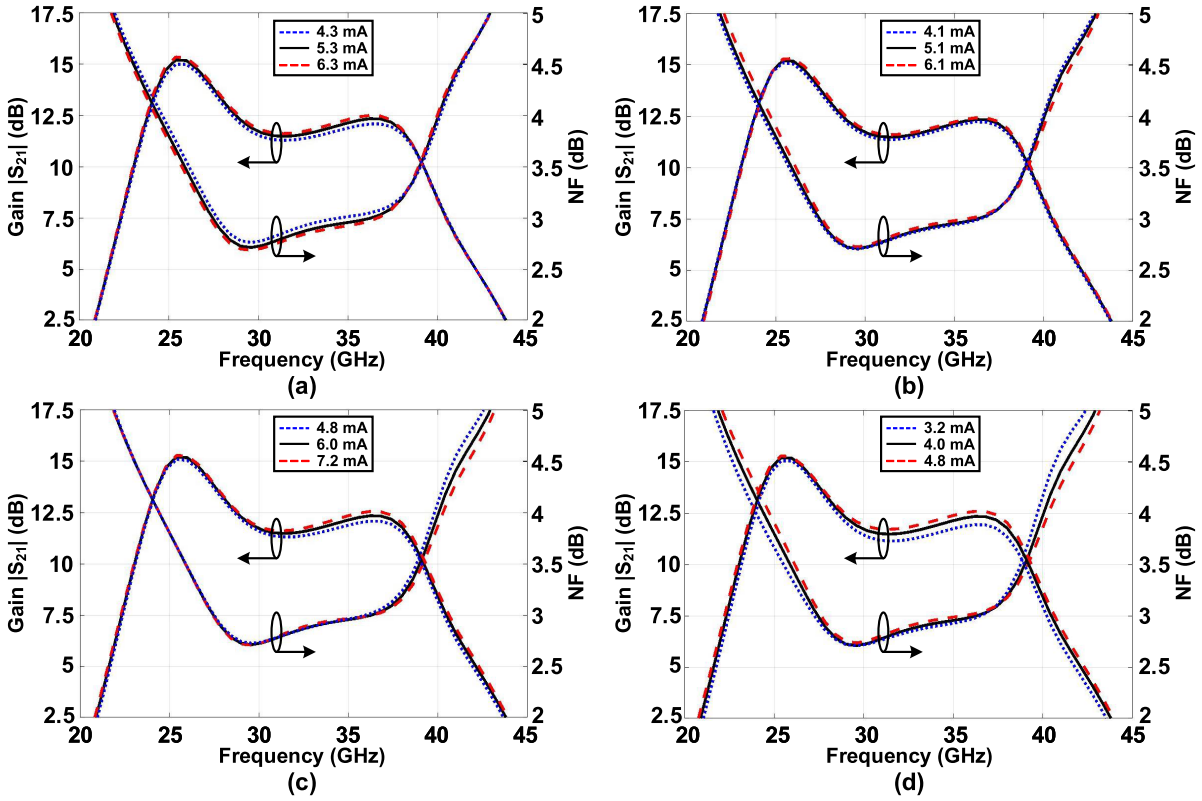


Fig. 23. Simulated NF and gain of the proposed LNA in different setting of (a) M_1 current, (b) M_2 current, (c) M_3 current, and (d) M_4 current.

are introduced for the fair comparison between the proposed LNA and previous works, which considers the performances of 3-dB BW, peak gain (power gain G_P and voltage gain G_V), linearity ($\text{IP}_{1\ \text{dB}}$ and IIP3), noise factor (F), and power consumption (P_{dc}). FoM_1 [5] and FoM_2 [19] are expressed as follows:

$$\text{FoM}_1 = \frac{G_P \times \text{BW[GHz]}}{F_{\text{min}} - 1} \times \frac{\text{IP}_{1\ \text{dB}}\text{[mW]}}{P_{\text{dc}}\text{[mW]}} \tag{32}$$

$$\text{FoM}_2 = 20\log_{10}\frac{G_V \times \text{BW[GHz]}}{F_{\text{min}} - 1} \times \frac{\text{IIP3[mW]}}{P_{\text{dc}}\text{[mW]}}. \tag{33}$$

Compared to the CG noise-canceling LNA at mm-wave [20], the proposed LNA achieves improved FoM in a compact size. Meanwhile, compared to the wideband dual-path noise-canceling LNA [25], the proposed LNA can obtain competitive performance at higher frequency. Compared to the state of the arts, Table II reveals that the proposed LNA shows enhanced performances in the low NF, high linearity, and low power consumption.

V. Conclusion

A dual-path noise-canceling LNA operated at 22.9–38.2 GHz is presented in this article. Compared to the conventional noise-canceling LNA with only one path noise-reducing ability, the proposed noise-canceling LNA is formed by a resistive feedback CS amplifier, two amplitude-adjusting amplifiers A_1 and A_2, and an output transformer, which can reduce the noise of both paths, simultaneously. The three-stage transformer can provide a g_m boosting, noise-reducing, and wideband interstage matching operation in CG amplifier, while the amplitude-adjusting amplifiers are utilized for the further improvement of noise-canceling performance. Then, the proposed LNA is fabricated in a conventional 28-nm CMOS technology and measured for verification. The proposed LNA consumes 18.9 mW from a 0.9-V power supply. The peak gain is 14.5 dB, while the 3-dB BW is 22.9–38.2 GHz. Within the operating frequency range, the minimum NF is 2.65 dB, while the peaks $\text{IP}_{1\ \text{dB}}$ and IIP3 are -6.6 and 3.2 dBm, respectively. With such good performances, the proposed dual-path noise-canceling LNA is attractive for wideband mm-wave wireless systems (e.g., 5G).

Appendix A

In the proposed dual-path noise-canceling LNA, the output transformer transfers the differential output of two paths to single end, and the input signals in paths I and II are recombined in-phase, while the out-of-phase noise is canceled at the single-end output. Fig. 21 shows that good in-band phase balance is achieved in the proposed dual-path noise-canceling LNA. However, the PVT variation and simulation inaccuracies will change the phase of both paths and hence result in performance degeneration. Such phase variation can be calibrated by introducing phase-tuning lines to both paths. As shown in Fig. 22(a), the proposed phase-tuning line consists of a coplanar waveguide (CPW) with grounded shield and four switchable capacitors. The switchable capacitors are controlled by the voltage $V_{c1,2,3,4}$, while the grounded shield [37] is utilized to reduce the substrate loss of the phase-tuning lines. The capacitance tuning range of each phase-tuning line is

about 7 fF, which results in about 4°–6° maximum available phase variation within the operation band. As shown in Fig. 22(b) and (c), the NF and gain of the proposed LNA vary with the phase settings. Note that, the proposed phase-tuning line is located in the inter-stage matching network of both paths, where the capacitance variation can not only change the phase shifting but also influence the gain and BW of the proposed LNA. Therefore, the further increase of phase-tuning range will cause significant performance degeneration on the gain and BW.

APPENDIX B

As shown in Fig. 23(a)–(d), the NF and gain changed slightly under the case of 20% current variation in one transistor, which shows that good robustness is achieved in the proposed LNA under partial bias variation.

REFERENCES

[1] H. Zhang, X. Fan, and E. S. Sinencio, "A low-power, linearized, ultra-wideband LNA design technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320–330, Feb. 2009.

[2] Y. Shim, C.-W. Kim, J. Lee, and S.-G. Lee, "Design of full band UWB common-gate LNA," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 10, pp. 721–723, Oct. 2007.

[3] Y.-T. Lo and J.-F. Kiang, "Design of wideband LNAs using parallel-to-series resonant matching network between common-gate and common-source stages," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 9, pp. 2285–2294, Sep. 2011.

[4] H. Gao *et al.*, "A 48–61 GHz LNA in 40-nm CMOS with 3.6 dB minimum NF employing a metal slotting method," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 154–157.

[5] M. Elkholy, S. Shakib, J. Dunworth, V. Aparin, and K. Entesari, "A wideband variable gain LNA with high OIP3 for 5G using 40-nm bulk CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 1, pp. 64–66, Jan. 2018.

[6] S. Kong, H.-D. Lee, S. Jang, J. Park, K.-S. Kim, and K.-C. Lee, "A 28-GHz CMOS LNA with stability-enhanced G_m-boosting technique using transformers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 7–10.

[7] L. Gao and G. M. Rebeiz, "A 24–43 GHz LNA with 3.1–3.7 dB noise figure and embedded 3-pole elliptic high-pass response for 5G applications in 22 nm FDSOI," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 239–242.

[8] S.-C. Shin, M.-D. Tsai, R.-C. Liu, K.-Y. Lin, and H. Wang, "A 24-GHz 3.9-dB NF low-noise amplifier using 0.18 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 7, pp. 448–450, Jul. 2005.

[9] Y. Ding, S. Vehring, and G. Boeck, "Design of 24 GHz high-linear high-gain low-noise amplifiers using neutralization techniques," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 944–947.

[10] R. Hu, "Wide-band matched LNA design using transistor's intrinsic gate-drain capacitor," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 3, pp. 1277–1286, Mar. 2006.

[11] M. T. Reiha and J. R. Long, "A 1.2 V reactive-feedback 3.1–10.6 GHz low-noise amplifier in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1023–1033, May 2007.

[12] B. Cui and J. R. Long, "A 1.7-dB minimum NF, 22–32-GHz low-noise feedback amplifier with multistage noise matching in 22-nm FD-SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1239–1248, May 2020.

[13] F. Zhang and P. R. Kinget, "Low-power programmable gain CMOS distributed LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1333–1343, Jun. 2006.

[14] J.-C. Kao, P. Chen, P.-C. Huang, and H. Wang, "A novel distributed amplifier with high gain, low noise, and high output power in 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1533–1542, Apr. 2013.

[15] V. Bhagavatula, M. Taghivand, and J. C. Rudell, "A compact 77% fractional bandwidth CMOS band-pass distributed amplifier with mirror-symmetric Norton transforms," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1085–1093, May 2015.

[16] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[17] I. Das and N. Nallam, "Noise cancelation? Explained!: The role of feedback in noise-canceling LNAs and receivers," *IEEE Microw. Mag.*, vol. 18, no. 6, pp. 100–109, Sep./Oct. 2017.

[18] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.

[19] J. Zhu, H. Krishnaswamy, and P. R. Kinget, "A DC-9.5 GHz noise-cancelling distributed LNA in 65 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2013, pp. 177–180.

[20] S. Li, T. Chi, D. Jung, T.-Y. Huang, M.-Y. Huang, and H. Wang, "An E-band high-linearity antenna-LNA front-end with 4.8 dB NF and 2.2 dBm IIP3 exploiting multi-feed on-antenna noise-canceling and G_m-boosting," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 78–79.

[21] M. El-Nozahi, A. A. Helmy, E. Sánchez-Sinencio, and K. Entesari, "An inductor-less noise-cancelling broadband low noise amplifier with composite transistor pair in 90 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1111–1122, May 2011.

[22] Z. Pan, C. Qin, Z. Ye, Y. Wang, and Z. Yu, "Wideband inductorless low-power LNAs with G_m enhancement and noise-cancellation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 1, pp. 26–38, Jan. 2018.

[23] B. Guo, J. Chen, L. Li, H. Jin, and G. Yang, "A wideband noise-canceling CMOS LNA with enhanced linearity by using complementary nMOS and pMOS configurations," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1331–1344, May 2017.

[24] M. Rahman and R. Harjani, "A 2.4-GHz, sub-1-V, 2.8-dB NF, 475-μm dual-path noise and nonlinearity cancelling LNA for ultra-low-power radios," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1423–1430, May 2018.

[25] H. Yu, Y. Chen, C. C. Boon, P.-I. Mak, and R. P. Martins, "A 0.096-mm^2 1–20-GHz triple-path noise canceling common-gate common-source LNA with dual complementary pMOS–nMOS configuration," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 1, pp. 144–159, Jan. 2020.

[26] A. J. Scholten, L. F. Tiemeijer, R. V. Langevelde, R. J. Havens, A. T. A. Z.-V. Duijnhoven, and V. C. Venezia, "Noise modeling for RF CMOS circuit simulation," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 618–632, Mar. 2003.

[27] X. Li, S. Shekhar, and D. J. Allstot, "G_m-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.

[28] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[29] T. Kihara, T. Matsuoka, and K. Taniguchi, "A 1.0 V, 2.5 mW, transformer noise-canceling UWB CMOS LNA," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2008, pp. 493–496.

[30] H. J. Qian, J. O. Liang, and X. Luo, "Wideband digital power amplifiers with efficiency improvement using 40-nm LP CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 3, pp. 675–687, Mar. 2016.

[31] Y.-H. Yu, Y.-S. Yang, and Y.-J.-E. Chen, "A compact wideband CMOS low noise amplifier with gain flatness enhancement," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 502–509, Mar. 2010.

[32] L. Gao, E. Wagner, and G. M. Rebeiz, "Design of E- and W-band low-noise amplifiers in 22-nm CMOS FD-SOI," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 1, pp. 132–143, Jan. 2020.

[33] P.-Y. Chang and S. S. H. Hsu, "A compact 0.1–14-GHz ultra-wideband low-noise amplifier in 0.13-μm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 10, pp. 2575–2581, Oct. 2010.

[34] Z. Deng, J. Zhou, H. J. Qian, and X. Luo, "High resolution reconfigurable phase-tuning line using self-shielded 3-D interdigital capacitor," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 6, pp. 605–608, Jun. 2020.

[35] L. Wu, H. F. Leung, and H. C. Luong, "Design and analysis of CMOS LNAs with transformer feedback for wideband input matching and noise cancellation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 1626–1635, Jun. 2017.

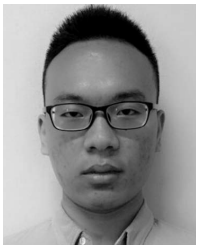
[36] D. M. Pozar, *Microwave Engineering*, 4th ed. New York, NY, USA: Wiley, 2011.

[37] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

Zhixian Deng (Graduate Student Member, IEEE) received the B.E. degree in microelectronics science and engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2019, where he is currently pursuing the Ph.D. degree in electronic science and technology.

His research interests include the reconfigurable microwave/millimeter-wave transceiver and passive components, especially integrated circuits.

Mr. Deng was a recipient of the IEEE IMS Student Design Competition Award from 2017 to 2019.



Jie Zhou (Student Member, IEEE) received the B.E. degree in microelectronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2016, where he is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics.

His research interests include reconfigurable transmitters and receivers.

Mr. Zhou was a recipient of the 2017 IEEE Microwave Theory and Techniques (MTT)-Society Undergraduate/Pre-Graduate Scholarship Award.

Huizhen Jenny Qian (Member, IEEE) received the B.E., master's, and Ph.D. degrees in electronic engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2008, 2011, and 2018, respectively.

Since 2019, she has been a Faculty Member with the Center for Integrated Circuits, UESTC, where she is currently an Associate Professor. Her research interests include wideband microwave/millimeter-wave transceivers, reconfigurable passive circuits, and on-chip array systems.

Dr. Qian was a recipient/co-recipient of the 2018 IEEE Microwave Theory and Techniques (MTT)-Society Graduate Fellowship Award, the IEEE International Wireless Symposium (IWS) Best Student Paper Award in 2015 and 2018, the IEEE International Microwave Symposium (IMS) Student Design Competition Award in 2017 and 2018, and the IEEE International Symposium on Radio-Frequency Integration Technology (RFIT) Best Student Paper Award in 2016 and 2019.

Xun Luo (Senior Member, IEEE) received the B.E. and Ph.D. degrees in electronic engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2005 and 2011, respectively.

From 2010 to 2013, he was with Huawei Technologies Company Ltd., Shenzhen, China, as the Project Manager to guide research and development projects of multi-band microwave/millimeter-wave (mm-wave) integrated systems for backhaul and wireless communication. Before joining UESTC, he was an Assistant Professor with the Department of Microelectronics, Delft University of Technology, Delft, The Netherlands. Since 2015, he has been with UESTC as a Full Professor, where he has been appointed as the Executive Director of the Center for Integrated Circuits. Since 2020, he has been the Head of the Center for Advanced Semiconductor and Integrated Micro-System, UESTC. He has authored or coauthored more than 100 journal and conference papers. He holds 39 patents. His research interests include RF/microwave/mm-wave integrated circuits, multiple-resonance terahertz (THz) modules, multi-bands backhaul/wireless systems, reconfigurable passive circuits, smart antennas, and system in package.

Dr. Luo is a Technical Program Committee Member of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. He is the Vice-Chair of the IEEE MTT-Society Chengdu Chapter. He was bestowed by China as the China Overseas Chinese Contribution Award in 2016. His Research Group BEAM X-Laboratory received multiple best paper awards and best design competition awards, including the IEEE RFIC Best Student Paper Award in 2021, the IEEE RFIT Best Student Paper Award in 2016 and 2019, the IEEE IWS Best Student Paper Award in 2015 and 2018, the IEEE IMS Best Student Design Competition Award from 2017 to 2019, the IEEE IMS Sixty-Second Presentation Competition Award in 2019, and multiple best paper award finalists from the IEEE conferences. He is also the TPC Co-Chair of the IEEE IWS in 2018 and the IEEE International Symposium on Radio-Frequency Integration Technology (RFIT) in 2019. He serves as a Track Editor for the IEEE MICROWAVE WIRELESS AND COMPONENTS LETTERS and is also an Associate Editor of the *IET Microwaves, Antennas & Propagation*.