Guest Editorial Introduction to the Special Issue on the 2021 IEEE International Solid-State Circuits Conference (ISSCC)

I. Introduction

THIS Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is dedicated to a collection of the best papers selected from the 2021 IEEE International Solid-State Circuits Conference (ISSCC) that took place on February 13–22, 2021, virtually. This issue covers papers from the Analog, Power Management, Data Converters, RF, and Wireless committees.

II. Analog Papers

Five analog papers from two sessions were selected, covering various design challenges in this field. The first paper presents a self-calibrated hybrid thermal-diffusivity and resistor-based temperature sensor, which demonstrates an inaccuracy of 0.25 °C (3σ) from −55 °C to 125 °C after 2-point trimming without relying on any external voltage/temperature references. The second paper introduces a capacitive humidity sensor readout using power-aware floating inverter amplifiers and adaptive range-shift zooming techniques, featuring a state-of-the-art resolution-FoM of 0.135 pJ·%RH^2. The third paper proposes a digital-input, variable-frequency $\Delta\Sigma$ Class-D amplifier for wireless headphone applications, achieving 82-mW non-clipping output power with 93% efficiency at 16 Ω and 33 μH load. The fourth paper presents a chopper-stabilized amplifier, which features a fill-in technique for mitigating the amplifier delay, achieving a measured IMD of −125.9 dB at an input frequency of 80 kHz. The final paper showcases a dynamic amplifier with paralleled Class-C and single-stage linear amplifiers, demonstrating a ≥100 dB dc gain and a 127-to-10 kHz GBW over 0.8-to-10 nF load with ≥59° phase margin.

III. Power Management Papers

Four papers were chosen from among two sessions covering power management topics, including dc–dc converters, high-voltage and gallium nitride GaN converters, and wireless power transfer. Ashourloo *et al.* present a hybrid Dickson switched-capacitor (SC) converter for automotive applications with up to 60-V input, 3.3-V output, and over 95% peak efficiency; the design leverages an integrated masterless multiphase controller for synchronizing across chip boundaries. Chen *et al.* present a monolithic GaN gate driver that uses circuit techniques to achieve fast turn-on while compensating for temperature effects of GaN switching devices and circuitry. Cao *et al.* present a high-conversion-ratio step-down dc–dc converter that uses an on-chip low-voltage hybrid SC converter combined with a single off-chip GaN FET to achieve over 90% efficiency at 1–2 A with 48 to 1 V step down. Novello *et al.* present a fully integrated dc–dc converter running at 1.25 GHz that uses on-chip coupled magnetics; the design achieves over 60% efficiency across a wide range and up to 1-W/mm^2 power density even while using a modest 180-nm process technology.

IV. Data Converter Papers

Three data converter papers were chosen for this special issue. The first paper demonstrates a 12-b, 16-GS/s RF-sampling capacitive DAC for multi-band software radio applications in a 16-nm FinFET process. Due to the co-integration with a wideband on-chip transmission-line matching network, the DAC is capable of signal synthesis between 500 MHz up to 8 GHz, with a measured peak RF output power of +5.6 dBm and a two-tone intermodulation distortion of better than −70 dBc up to the first Nyquist frequency with linearization. The second paper presents a synergistic effort of achieving a third-order noise shaping using only a single amplifier with an EF-CIFF structure while simultaneously attaining sampling kT/C noise cancellation in a noise-shaping SAR ADC. Prototyped in a 65-nm CMOS process, the work achieves an 84.8-dB SNDR in a 625-kHz bandwidth with a 182-dB Schreier FoM and a 0.8-pF input capacitance. The last paper in this section showcases a band-pass time-interleaved noise-shaping SAR ADC employed in a continuous-time, hybrid-loop delta-sigma modulator. The prototype, implemented in a 28-nm CMOS process, measured a peak SNDR of 67.5 dB with a 100-MHz bandwidth while consuming 13.4 mW at 1.6 GS/s.

V. Radio Frequency Papers

Six papers were chosen from four sessions covering various radio frequency topics, including power amplifiers, PLLS,

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RF front-ends, and VCOs from RF to THz. Qunaj *et al.* present a load-modulated balanced PA in the Ka-band for emerging cellular applications. The PA achieved a linear output power of 16 dBm operating at 36 GHz with a PAE of 22% and 20%, respectively, for data rates of 12 and 18 Gb/s. Yang *et al.* present a reflection coefficient sensor in the Ka-band that can be used for PA load tuning among other applications. The sensor is compact, power-efficient and achieved a magnitude error of <0.14 rms and a phase error of <40° rms. Yang *et al.* present a digital switch/floated capacitor power amplifier that achieved watt-level peak output power. The digital PA was able to output a 1k-QAM signal with a 40 MHZ bandwidth, while output $P_{\text{out}} > 23$ dBm and $\eta > 22\%$, achieving an EVM of -35.9 dB. Shu *et al.* present a low-phase noise VCO that utilized a four-port transformer at its core, with active devices integrated into the center of the winding. The VCO achieved a phase noise of < -132.2 dB/Hz at 1 MHz offset while consuming 20.9 mW across the 3–4 GHz frequency range. Qiu *et al.* present an oversampling PLL that uses a 32 kHz crystal oscillator reference, allowing power savings in IoT applications. The PLL, fabricated in 65 nm, achieves an rms jitter = 5.8 ps while consuming only 5 mW. Wu *et al.* present an analog-sampling Fractional-N PLL using a digital-to-time converter range-reduction technique. The PLL is fabricated in 14-nm FinFETs and achieves an rms jitter = 80 fs while consuming on 14.2 mW.

VI. Wireless Papers

Six papers were selected from four sessions focused on sub-6 GHz, millimeter-wave, ultra-wideband, terahertz, and low-power communication systems. The first paper presents a 5.4-GHz digital RF transmitter using a four-way Doherty combiner and a 50%-LO-based upconverter for high efficiency and spectral purity. The second describes a high efficiency 27 GHz transmitter that has a balanced power amplifier realized by combining two identical Doherty amplifiers through a quadrature hybrid coupler. The third paper demonstrates a 3–10 GHz impulse-radio ultra-wideband polar transmitter that employs analog-FIR pulse shaping and duty cycling to reduce power consumption. The fourth paper presents a packaged 16-element by 16-beam fully connected 71–86-GHz receiver sub-array for massive MIMO. The last two papers present THz transceiver ICs on CMOS for high accuracy phase imaging and localization of wireless nodes. They respectively achieve sub-5-μm range resolution and sub-2° 2-D localization accuracy. The work described in this set of papers defines the cutting edge of integrated circuits for wireless systems by advancing the power efficiency and integration level over the entire radio frequency range from GHz to THz.

Acknowledgment

The Guest Editors wish to thank all of the people involved in the paper selection process. The paper selection process involved tireless effort from the ITPC members who reviewed all of the ISSCC paper submissions, the ISSCC audience who rated papers during the conference, and the ISSCC session chairs who provided paper recommendations. The Guest Editors also thank the anonymous reviewers for their contributions during the paper review.

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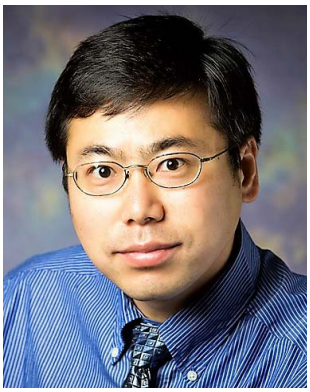

Yun Chiu (Senior Member, IEEE) received the B.S. degree in physics from the University of Science and Technology of China, Hefei, China, the M.S. degree in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, and the Ph.D. degree in electrical engineering and computer sciences from the University of California at Berkeley, Berkeley, CA, USA.

He was a Senior Staff Member of CondorVision Technology Inc., Fremont, CA, USA, from 1997 to 1999, in charge of developing analog and mixed-mode circuits for CMOS digital imaging products. From 1999 to 2004, he was with the Berkeley Wireless Research Center, University of California at Berkeley, where he worked on low-power and low-voltage CMOS data converters. In 2004, he joined the Department of Electrical and Computer Engineering, University of Illinois at Urbana–Champaign, Champaign, IL, USA, as an Assistant Professor, where he received the tenure offer in 2010. He is currently a Full Professor and the Erik Jonsson Distinguished Professor with the Department of Electrical and Computer Engineering, The University of Texas at Dallas, Richardson, TX, USA, where he also directs the Analog and Mixed-Signal Laboratory of the Texas Analog Center of Excellence. He has over 100 conference, journal, and book publications. His research interests are in the design of energy-efficient, highly integrated analog-digital interface ICs and subsystems, encompassing data converters (ADCs and DACs), amplifiers and filters, RF transmitter and receiver front-ends, power electronics, bio-electronic interfaces, detector front-end electronics for particle experiments, and adaptive signal-processing algorithms for chip-level analog performance enhancement.

Dr. Chiu was a co-recipient of the Jack Kilby Outstanding Student Paper Award from the 2004 International Solid-State Circuits Conference (ISSCC), the Outstanding Evening Session Award from the 2017 ISSCC, the 46th ISSCC/DAC Student Design Contest Award in 2009, and the Best Regular Paper Award from the 2012 Custom Integrated Circuits Conference (CICC). He was a Guest Editor of the Special Issue for 2021 ISSCC of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: Express Briefs from 2007 to 2009; he also served on the technical program committees of several IEEE solid-state circuits conferences, including the Symposium on VLSI Circuits, the CICC, and the Asian Solid-State Circuits Conference (A-SSCC). He currently serves on the data converter committee of the ISSCC.

Man-Kay Law (Senior Member, IEEE) received the B.Sc. degree in computer engineering and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2006 and 2011, respectively.

In 2011, he joined HKUST as a Visiting Assistant Professor. He is currently an Associate Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, Institute of Microelectronics, University of Macau, Macau, China. He has authored or coauthored more than 100 technical publications and holds six U.S./Chinese patents. His research interests are in the development of ultra-low-power CMOS sensing/readout circuits and energy harvesting techniques for wireless and biomedical applications.

Dr. Law was a co-recipient of the ASQED Best Paper Award in 2013, the A-SSCC Distinguished Design Award in 2015, the ASPDAC Best Design Award in 2016, and the Macao Science and Technology Invention Award by Macau Government–FDCT in 2020 (First Class), and in 2014 and 2018 (Second Class). He is also a Distinguished Lecturer of IEEE CASS and IEEE SSCS. He serves as a Technical Committee Member of IEEE CAS Committee on Sensory Systems as well as Biomedical and Life Science Circuits and Systems. He is a TPC Member of IEEE ISSCC, and also the ISSCC Far-East Secretary in 2022.

Nagendra Krishnapura (Senior Member, IEEE) received the B.Tech. degree from the Indian Institute of Technology Madras, Chennai, India, and the Ph.D. degree from Columbia University, New York, NY, USA.

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Jason T. Stauth (Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley, Berkeley, CA, USA, in 2006 and 2008, respectively.

Since 2011, he has been with the Thayer School of Engineering, Dartmouth College, Hanover, NH, USA, where he is currently an Associate Professor of Engineering. He was an IC Design Engineer at Allegro Microsystems from 2000 to 2003, a co-founder of QVSense, and the Director of Hardware Engineering at Solar Semiconductor from 2008 to 2011. He co-founded and advised Hive Battery from 2017 to 2020. His research interests include high-density and integrated dc–dc converters for renewable energy, automotive, computing, and soft-robotics applications.

Dr. Stauth is a member of the technical program committees for the IEEE International Solid-State Circuits Conference (ISSCC) and the IEEE Custom Integrated Circuits Conference (CICC). He received the NSF CAREER Award in 2016, best paper awards from IEEE COMPEL in 2015 and 2016, and the Excellence in Teaching Award from the Thayer School of Engineering in 2018. He is an Associate Editor of the IEEE SOLID-STATE CIRCUITS LETTERS (SSCL). From 2016 to 2021, he was an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS (TPEL) and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

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Prior to starting his graduate education, he was employed with Motorola Solutions, Plantation, FL, USA, working in cellular handset development. He was an Intern at Intel, Hillsboro, OR, USA, from 2006 to 2007, and a Post-Doctoral Research Associate with the University of Washington from 2008 to 2010. He was an Assistant Professor with the Department of Electrical and Computer Engineering, Rutgers University, New Brunswick, NJ, USA, from 2011 to 2012, and then an Assistant Professor and later an Associate Professor with the Department of Electrical and Computer Engineering, The University of Utah, Salt Lake City, UT, USA, from 2012 to 2018. He was the Head of the Group (RF Transceivers) at the Microelectronic Circuits Centre Ireland, Tyndall National Institute, in 2019. He is currently an Associate Professor at Virginia Tech, Blacksburg, VA, USA. He has authored more than 70 articles in peer-reviewed journals and refereed conferences. His research interests include high-efficiency digital transmitter architectures and power amplifier design.

Dr. Walling is a member of the ITPC for ISSCC. He received the Award for Outstanding Teaching at The University of Utah in 2015, the Excellence in Teaching Award from HKN at Rutgers University in 2012, the Best Paper Award from MobiCom in 2012, the Yang Award for Outstanding Graduate Research from the Department of Electrical Engineering, University of Washington, in 2008, an Intel Predoctoral Fellowship from 2007 to 2008, and the Analog Devices Outstanding Student Designer Award in 2006. He is an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS.