A Fractional-N Digitally Intensive PLL Achieving 428-fs Jitter and <-54-dBc Spurs Under 50-mV_{pp} Supply Ripple

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***Abstract*— In this article, we present a 4.5–5.1-GHz fractional-N digitally intensive phase-locked loop (DPLL) capable of maintaining its performance in face of a large supply ripple, thus enabling a direct connection to a switched-mode dc–dc converter. Supply pushing of its inductor–capacitor (LC) oscillator is suppressed by properly replicating the supply ripple onto the gate of its tail current transistor, while the optimum replication gain is determined by a new on-chip calibration loop tolerant of supply variations. A proposed configuration of cascading a supply-insensitive slope generator with an output of a current digital-to-analog converter (DAC) linearly converts the phase error timing into a corresponding voltage, which is then quantized by a successive approximation register (SAR) analog-to-digital converter (ADC) to generate a digital phase error. We also introduce a low-power ripple pattern estimation and cancellation algorithm to remove the phase error component due to the supply-induced delay variations of loop components. Implemented in 40-nm CMOS, the DPLL prototype achieves the performance of 428-fs rms jitter, <-55-dBc fractional spur, and <-54-dBc maximum spur while consuming 3.25 mW and being subjugated to a sinusoidal or sawtooth supply ripple of 50 mV_{pp} at 50-MHz reference divided by 3, 6, or 12.**

***Index Terms*— Current digital-to-analog converter (DAC), dc–dc converter, digitally intensive phase-locked loop (DPLL), inductor–capacitor (LC) oscillator, multimodulus divider (MMDIV), resample, ripple pattern estimation and cancellation, ripple replication and cancellation, slope generator (SG), successive approximation register (SAR) analog-to-digital converter (ADC), supply pushing, supply ripple.**

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I. Introduction

INTEGRATED circuits and systems are generally powered by switch-mode dc–dc converters, which transforms the voltage level of an energy source into the system's nominal supply voltage with sufficiently high efficiency [1]. However, if the dc–dc converter directly supplies sensitive analog or RF circuits, such as oscillators and phase-locked loops (PLLs), its output ripples could severely degrade their performance. Consequently, a low dropout (LDO) linear regulator is typically inserted after the switching converter to suppress the ripples. When the dominant pole of the LDO is located at its output, the load capacitor could be as large as several microfarads to guarantee the loop stability, thus necessitating the use of external capacitors. Hence, following the trend of full-system integration, the "capacitor-less" LDO topology with the dominant pole located at the output of the error amplifier (EA) is preferred. However, to isolate the sensitive oscillator from the clocked phase detection circuitry, PLLs usually require two separate LDOs [2], thereby worsening the system complexity and cost. The power efficiency of the LDO is related to both its dropout voltage (V_{DO}) and the quiescent current flowing through the EA (I_{EA}) and through the feedback resistor (I_F). The ~100-mV V_{DO}, established by the required power supply rejection (PSR) performance, consumes extra voltage headroom and degrades system efficiency by a factor of $\sim 0.9\times$ at a 1-V supply [3]. The levels of I_{EA} and I_F are mainly determined by the figure of merit (FoM) of the oscillator (FoM_{osc}) and loop (FoM_{loop}) components [4] for the corresponding LDOs, respectively. The analysis in [3] shows that the efficiency of the LDO powering the oscillator could further drop by a factor of ~ 0.7–$0.8\times$ due to the quiescent current. Consequently, it deems beneficial if the PLL could be powered directly from the dc–dc converter, thus entirely avoiding the LDOs.

The implementation of such a PLL faces several challenges. First, since the switched-capacitor-based dc–dc converters are generally clocked at several or tens of MHz, the induced variation on oscillator frequency could hardly be suppressed by PLLs with a typical bandwidth of <1 MHz.[1] Hence, several

[1] Note that the transfer function from the oscillator output to the PLL output is high pass.

techniques have been proposed in the literature to reduce the supply pushing of the oscillator [5]–[15]. However, most of these techniques are only effective for tiny (e.g., 1 mV) [5] or low frequency (<1 MHz) [6], [7], [10], [13] supply ripples or would require high power and area overhead [11], [12]. In [9], the PLL loop needs to be periodically opened for calibration. In [14], a test signal that is slow enough compared to the PLL bandwidth is applied on the supply of a ring oscillator, but this could lead to a long calibration time of more than hundreds of microseconds. Moreover, unlike in the ring oscillator [9], [14], it is difficult to modulate the supply of an inductor–capacitor (LC) oscillator. In [16], we have proposed a feedforward ripple replication and cancellation technique for an LC oscillator. However, similar to [12], its calibration loop still requires a "clean" supply.

Besides the oscillator, the delay and transfer function of the PLL's other building blocks are also modulated by the supply ripple, thus contributing to the phase error perturbation at the output of a phase detector (PD). This increases the PLL output spurs, mainly at the ripple frequency, f_{rip}, and its harmonics. Moreover, in a fractional-N operation, the fractional frequency (f_{frac}) inter-modulates with f_{rip} due to the PD nonideality, generating output spurs at the intermodulation frequencies ($f_{\text{rip}} \pm f_{\text{frac}}$). Nevertheless, in the scarcely available literature on PLLs with reduced supply sensitivity, mainly the integer-N operation is considered [2], [17], while the intermodulation problem between f_{rip} and f_{frac} of fractional-N operation is seldom discussed.[2]

In contrast to its analog counterpart, a highly digitally intensive PLL (DPLL) features the natural ability to exploit various digital calibration techniques to tackle the aforementioned issues with relative ease. Consequently, a DPLL is favored when architecting for the direct powering by the switched-mode dc–dc converter. In this article, we propose a digital-to-analog converter (DAC)-assisted fractional-N DPLL architecture to enable direct operation under a large 50-mV_{pp} supply ripple. The reduced supply sensitivity of the proposed voltage-domain PD suppresses the intermodulated terms, while the effect of the supply-induced delay variation is canceled through digital calibration. The supply pushing of the LC oscillator is also reduced through the feedforward cancellation technique with an improved calibration loop.

This article is organized as follows. Section II provides a detailed analysis of the issues encountered by directly powering the PLL from the converter. The proposed loop structure is derived in Section III. The detailed circuit implementations of different DPLL blocks are discussed in Section IV, while measurement results are provided in Section V.

II. Design Challenges When Supplying PLL With Large Ripple

This section investigates the effects of supply ripple on the PLL's spectral purity. Note that although the DPLL structure is chosen as an example in a portion of the following analysis, the result is also valid for analog PLLs.

[2]Note that the intermodulation effect analyzed in [18] and [19] is between the reference frequency and the oscillation frequency, generating fractional spurs, which is not similar to the effect mentioned here.

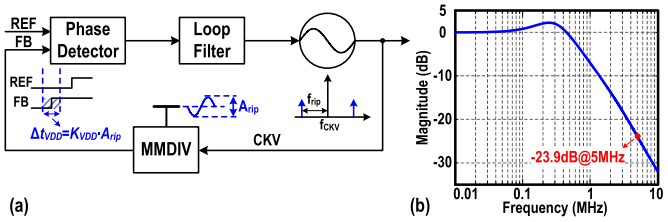

Fig. 1. (a) Spurs produced by the supply ripple modulating the divider output delay. (b) Magnitude response of a type-II PLL with a typical 300-kHz bandwidth and a damping factor of 0.707.

A. Spurs Due to Oscillator Supply Pushing

It is well known that the level of spurious tones around the carrier, induced by a sinusoidal supply ripple with a peak-to-peak amplitude of A_{rip} and a frequency of f_{rip}, can be estimated by

$$S_{\text{osc}} = 20 \cdot \log_{10}\left(\frac{K_{\text{push}} \cdot A_{\text{rip}}}{4 f_{\text{rip}}}\right) \tag{1}$$

where K_{push} is the supply pushing of the oscillator. From (1), to guarantee <-50 dBc spur level under a 50-mV_{pp} ripple, K_{push} should be less than 1.26 MHz/V, which is much lower than that of state-of-the-art RF oscillators [20]. To tackle this issue, the feedforward cancellation technique with an improved calibration loop is introduced in Section IV-D to improve the oscillator's supply sensitivity.

B. Spurs Due to Delay Perturbations of PLL's Components

Supply ripples also degrade the PLL's spectral purity by modulating the delay of the edge-critical loop components. Fig. 1(a) shows an example in which the propagation delay of the multimodulus divider (MMDIV) is affected by its supply voltage. This delay variation is then sensed by the PD and transferred to the PLL's output, leading to spurs at f_{rip} from the carrier. Assuming that the delay deviation is proportional to its supply perturbation A_{rip}, the spur level can be calculated as

$$S_{\text{dly}} = 20 \cdot \log_{10}\left(\frac{\pi \cdot K_{\text{VDD}} \cdot A_{\text{rip}}}{2 T_{\text{CKV}}}\right) + \text{TF}_{\text{loop}} \tag{2}$$

where K_{VDD} is the supply sensitivity of the MMDIV delay, T_{CKV} is the oscillator period, and TF_{loop} expresses the amount of dB attenuation provided by the loop. A detailed derivation of (2) is provided in Appendix A. The magnitude response of a type-II DPLL with a typical 300-kHz bandwidth is shown in Fig. 1(b). Note that a wider bandwidth would result in a lower attenuation by the loop (TF_{loop}), worsening the spur performance due to the delay variation, while a narrower bandwidth would provide less filtering of the oscillator phase noise (PN), consequently affecting the in-band PN and jitter performance of the loop [4]. For a 5-MHz f_{rip}, the suppression offered by the loop is only -23.9 dB. Hence, with a simulated $K_{\text{VDD}} \approx 400$ ps/mV, a 50-mV_{pp} ripple causes an approximately -40-dBc spur at a 5-GHz carrier. Therefore, extra techniques will be introduced in Section IV-C3 in order to suppress the effect of this delay variation and to reduce the corresponding spurs.

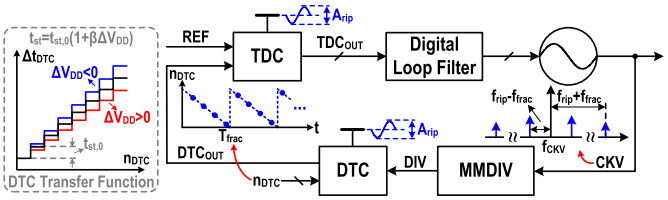

Fig. 2. Conventional time-domain DPLL employing DTC and TDC.

C. Spurs Due to Intermodulation Between f_{rip} and f_{frac}

Conventionally, the fractional-N DPLL has been realized in the time domain and quantizes its phase error by means of a time-to-digital converter (TDC) [21]. In order to limit the TDC input range, a digital-to-time converter (DTC) is typically inserted before it [22], [23], as shown in Fig. 2. The delay generated by the DTC compensates for the sawtooth phase error corresponding to the synthesized fractional channel (ω_{frac}). Hence, the DTC input codeword may be estimated by

$$n_{\text{DTC}} = \frac{T_{\text{CKV}} \cdot \text{sawtooth}\{\omega_{\text{frac}} t\}}{t_{\text{st},0}} \tag{3}$$

where $t_{\text{st},0}$ is the nominal DTC time step. By virtue of the fine-resolution DTC, the TDC should ideally see a constant input. Thus, the power consumption, linearity, and supply sensitivity of the TDC can be significantly relaxed. However, the DTC performance becomes crucial as it needs to cover a large dynamic range with sufficiently fine resolution. Since the DTC delay is typically set by changing the load of an inverter [22], [24], its time step is sensitive to supply and can be modeled by

$$t_{\text{st}} = t_{\text{st},0} \cdot \left(1 + 0.5\beta A_{\text{rip}} \sin(\omega_{\text{rip}} t)\right) \tag{4}$$

where β is the supply sensitivity of DTC delay in V^{-1}. Consequently, the DTC output delay is modulated by the supply ripple as

$$\begin{aligned}\Delta t_{\text{DTC}} &= n_{\text{DTC}} \cdot t_{\text{st}} \\ &= T_{\text{CKV}} \cdot \text{sawtooth}\{\omega_{\text{frac}} t\}\left(1 + 0.5\beta \text{A}_{\text{rip}} \sin(\omega_{\text{rip}} \text{t})\right).\end{aligned} \tag{5}$$

By replacing the sawtooth waveform in (5) with the fundamental component of its Fourier transform and after lengthy algebra, we obtain

$$\begin{aligned}\Delta t_{\text{DTC}} = \frac{T_{\text{CKV}}}{\pi} \sin(\omega_{\text{frac}} t) + \frac{\beta A_{\text{rip}} T_{\text{CKV}}}{4\pi} \\ \cdot \left(\cos[(\omega_{\text{rip}} - \omega_{\text{frac}})t] - \cos[(\omega_{\text{rip}} + \omega_{\text{frac}})t]\right).\end{aligned} \tag{6}$$

As a result, Δt_{DTC} will contain frequency components at $f_{\text{rip}} \pm f_{\text{frac}}$, potentially generating in-band spurs at the DPLL output at the level of $20\log_{10}(\beta \cdot A_{\text{rip}}/4)$. A detailed analysis is provided in Appendix B.

Based on circuit-level simulations in the employed 40-nm CMOS node, β is around 1.2–2.05 V^{-1}, corresponding to a spur level of −31.8 to −36.5 dBc. Considering that f_{frac} is likely subject to frequent changes, a calibration of the intermodulation terms could be unfeasible. The analysis above assumes that a first-order $\Delta\Sigma$ modulation is used in the loop. For a higher order modulation, the sawtooth pattern at the PD input would be randomized, reducing the spur level due to the intermodulation. However, its quantization noise around f_{rip} will be down-converted by the DTC/TDC supply sensitivity, thus degrading the in-band PN. Therefore, it is still necessary to improve the supply sensitivity of PD. Hence, in Section III, we propose a digital PD structure with improved supply immunity to suppress the performance degradation due to such intermodulation.

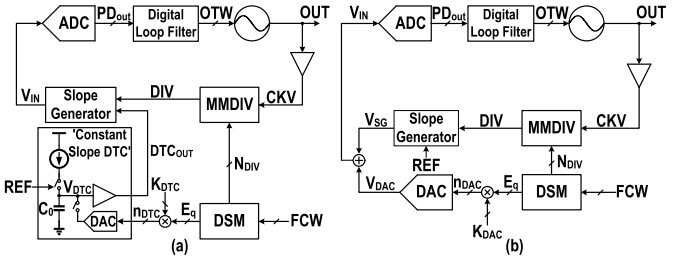

Fig. 3. ADC-based fractional-N DPLL structure using (a) constant-slope DTC or (b) DAC.

As mentioned above, the analysis in this section is valid for both analog and digital PLL implementations. Compared to the case of DTC/TDC, a charge pump in the conventional analog PLL may offer a lower sensitivity to supply. However, the charge pump could become overly sensitive by a mismatch between its "up" and "down" current branches [25]. Meanwhile, the divider, phase/frequency detector (PFD), and buffers used as an interface between different blocks are still affected by the supply ripple, thus necessitating calibrations to remove their effects. Since the phase error information in the analog [26]–[29] or hybrid [30], [31] PLLs is processed in the voltage domain, the implementation of the calibration loops would be more complex than in their digital counterparts and further deteriorated by the non-idealities of analog circuits in sub-micrometer technologies. Therefore, a highly digitally intensive PLL architecture is selected here to realize the direct connection to the dc–dc converter output.

III. Proposed DPLL Architecture

In contrast to the aforementioned time-domain realization, implementation of the phase detection in the voltage domain (see Fig. 3(a) as an example) has been gaining popularity in recent years [24], [32]–[36]. Assisted by a steep slope of the sampled waveform, the analog-to-digital converter (ADC)-based PD could achieve a fine resolution at low power consumption [24], [32]–[34]. Due to its power efficiency and simple structure, a successive approximation register (SAR)-ADC is beneficially employed in the DPLL design. By operating in the voltage domain with only one comparator and a capacitive DAC (CDAC), it also provides better immunity to supply variations. However, for fractional-N applications, a DTC is still used to accommodate the limited linear range of the slope generator (SG) and to reduce the dynamic range of the ADC [24], [33]. In order to further exploit the operation in the voltage domain with improved supply immunity, a constant-slope DTC should be considered here [37]–[39]. As shown in Fig. 3(a), the constant-slope DTC charges a load capacitor, C_0, with a constant current at the corresponding edge of the input signal and flips the following

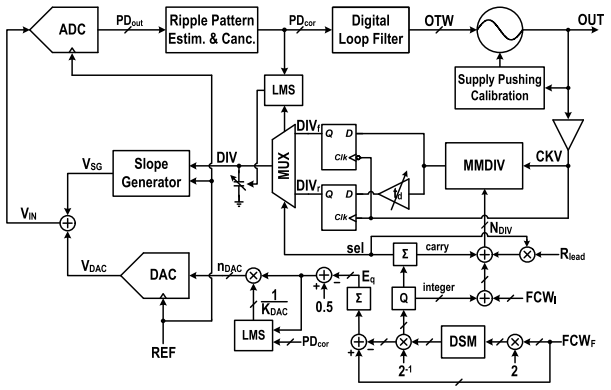

Fig. 4. Block diagram of the proposed fractional-N DPLL.

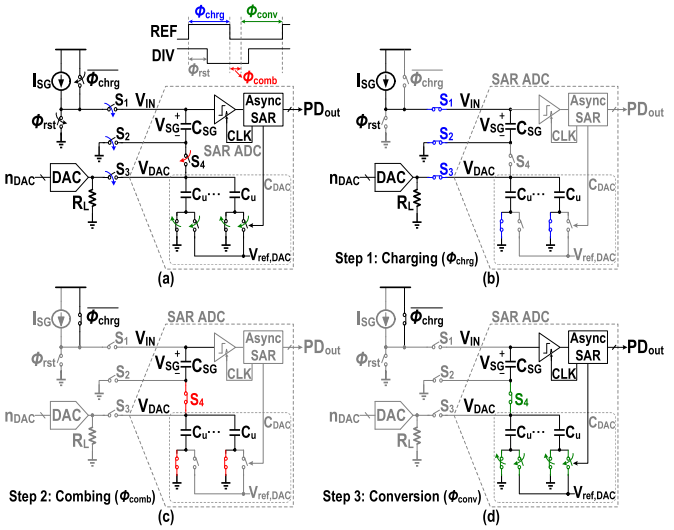

Fig. 5. (a) Simplified block diagram, and (b)–(d) operational principle of PD.

buffer when the charged voltage level reaches its threshold. The variable output delay is achieved by presetting the starting voltage on C_0 to different values using a DAC. Given that this DAC can be implemented with good supply immunity, the DPLL structure of Fig. 3(a) would be able to better tolerate supply ripples.

To detect the phase error, the DPLL structure in Fig. 3(a) traverses between the time and voltage domains several times. First, the constant-slope DTC converts the desired delay into the starting voltage on C_0. Second, the following buffers convert it back to the time domain. Third, the slope generator converts the time difference between the DTC output, DTC_{out}, and the feedback signal, DIV, into the ADC input voltage, V_{IN}. In fact, this process could be simplified, as shown in Fig. 3(b). In this structure, the time difference between the reference signal, REF, and the feedback signal, DIV, is directly converted into a corresponding voltage, V_{SG}, through the slope generator, while a DAC is used to generate a compensation voltage, V_{DAC}, based on the MMDIV quantization error. By summing V_{SG} and V_{DAC}, the resulting V_{IN} will be only proportional to the PN component and vary little when the PLL is locked. The structure in Fig. 3(b) now operates entirely in the voltage domain, reducing its supply sensitivity. Essentially, it converts the time to voltage only once, simplifying the system structure and circuit implementation. A similar voltage-domain PD is also used in [40] to achieve an improved power–jitter tradeoff. However, to operate under the supply ripple, the loop in [40] and Fig. 3(b) still needs to be further modified.

The complete loop structure is shown in Fig. 4. The ripple pattern estimation and cancellation block is inserted after the ADC to remove the phase error pattern at f_{rip} induced by the delay variations of loop components due to the supply ripple. To further suppress the spur due to the intermodulation effect, a second-order $\Delta\Sigma$ modulator is employed, while the MMDIV output is resampled by both edges of the oscillation signal, CKV, to limit the input range of the slope generator for better linearity and noise performance. The mismatch between the two resampling paths is compensated by varying the capacitive load of the multiplexer (MUX) through a least mean square (LMS) algorithm. Finally, to suppress the supply pushing of the LC oscillator, the feed-forward cancellation technique proposed in [16] is adopted, while its calibration loop has been modified to be able to tolerate the supply ripples.

IV. Circuit Implementation

In this section, the detailed circuit implementation of key blocks in the proposed fractional-N DPLL is discussed.

A. Phase Detector

1) Operating Principle: A simplified block diagram of the phase detection circuitry is shown in Fig. 5(a). It chiefly consists of a slope generator, a current-steering DAC, a combiner switch (S_4), and an SAR ADC converting the phase error to a digital bitstream. The desired phase error is digitized through three steps: charging (ϕ_{chrg}), combining (ϕ_{comb}), and conversion (ϕ_{conv}), as shown in Fig. 5(b)–(d). During the first step ϕ_{chrg}, the current source in the slope generator, I_{SG}, charges the load capacitor, C_{SG}, between the falling edges of REF and DIV [41], [42], converting its input time difference into a corresponding voltage

$$V_{\text{SG}} = (t_{\text{os}} + E_q \times T_{\text{CKV}} + t_n) \times (I_{\text{SG}}/C_{\text{SG}}) \tag{7}$$

where $E_q \times T_{\text{CKV}}$ is the deterministic time error due to the fractional operation, t_n is the time difference due to the random noise and supply-induced delay variations in the loop, and t_{os} is the time offset between the falling edges of REF and DIV in the absence of any deterministic and random noise. During the same phase, to compensate for the deterministic part in V_{SG}, the DAC output voltage, V_{DAC}, is also impressed on C_{DAC}, while the bottom plate of its unit capacitors (C_{u}) is connected to the ground. Note that the same unit capacitors will be used as the charge-scaling DAC by the ADC in the conversion phase. The DAC control code, n_{DAC}, is determined by the accumulated quantization error of the $\Delta\Sigma$ modulator driving the divider (E_q in Fig. 4)

$$n_{\text{DAC}} = (E_{q,\max} - E_q)/\widehat{K}_{\text{DAC}} \tag{8}$$

where $E_{q,\max}$ is the maximum value of E_q (with a second-order $\Delta\Sigma$ modulator and the resampling technique in Section IV-B, $E_{q,\max} = 0.5$). $\widehat{K}_{\text{DAC}}$ is the estimation of DAC gain, $K_{\text{DAC}} = (V_{\text{res}} \cdot C_{\text{SG}})/(T_{\text{CKV}} \cdot I_{\text{SG}})$, where V_{res} is the

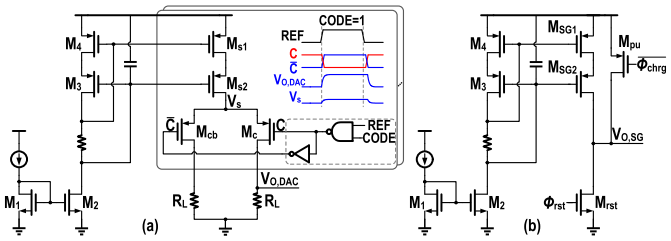

Fig. 6. Schematic of (a) current DAC and (b) slope generator.

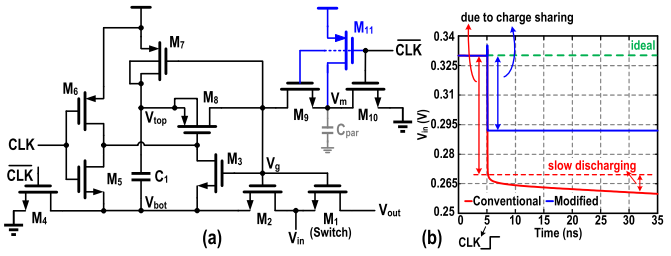

Fig. 7. (a) Schematic of the bootstrap switch. (b) Simulated performance of S_4 during the tracking phase.

DAC voltage resolution. When it is accurately estimated, the sampled V_{DAC} can be calculated by

$$V_{\mathrm{DAC}} = V_{\mathrm{DAC,os}} + n_{\mathrm{DAC}} \times V_{\mathrm{res}} = V_{\mathrm{DAC,os}} + (E_{q,\max} - E_q) \times T_{\mathrm{CKV}} \times (I_{\mathrm{SG}}/C_{\mathrm{SG}}) \quad (9)$$

where $V_{\mathrm{DAC,os}}$ is an offset voltage independent of n_{DAC}. In the next step, ϕ_{comb}, V_{SG}, and V_{DAC} are combined by connecting the top plate of C_{DAC} to the bottom plate of C_{SG} through S_4. By summing (7) and (9), the generated ADC input voltage becomes

$$V_{\mathrm{IN}} = t_n \times (I_{\mathrm{SG}}/C_{\mathrm{SG}}) + [V_{\mathrm{DAC,os}} + (I_{\mathrm{SG}}/C_{\mathrm{SG}}) \times (t_{\mathrm{os}} + E_{q,\max} \times T_{\mathrm{CKV}})]. \quad (10)$$

The second term in (10) is time-invariant related to t_{os}. Due to the feedback operation of the loop, t_{os} will be adjusted automatically such that the corresponding term settles to the ADC's reference level, V_{ref}. Therefore, the ADC only needs to convert the input variations related to t_n. Note that the system is designed so that $V_{\mathrm{DAC,os}}$ and the C_{SG} charge due to t_{os} equally provide the required input dc offset. Hence, the maximum voltage on the C_{SG} and C_{DAC} capacitors is limited to $\sim V_{\mathrm{ref}}/2$, providing enough voltage headroom for the PMOS current sources to operate linearly. In contrast, the DAC and slope generator in [40] sequentially charge the same capacitor to $\sim V_{\mathrm{ref}}$. This reduces the voltage headroom of the slope generator's current source, substantially degrading its linearity in a deep sub-micrometer technology with reduced supply.

2) Circuit Design: Fig. 6(a) shows the DAC schematic, consisting of 290 unary cascode current sources to satisfy the range and linearity requirements. As the DAC is biased through the current mirror, the DAC output variation due to the supply ripple can be estimated by

$$V_{\mathrm{O,DAC}} \approx \frac{R_L}{R_L + r_{o,s1} + r_{o,s2} + g_{m,s2} r_{o,s1} r_{o,s2}} \cdot A_{\mathrm{rip}} \quad (11)$$

where $g_{\mathrm{m,s1(2)}}$ and $r_{\mathrm{o,s1(2)}}$ are the small-signal transconductance and output resistance of $M_{\mathrm{s1(2)}}$, respectively. Equation (11) shows that the high output impedance of the cascode structure is also beneficial in suppressing the supply-induced variation at the DAC output, and consequently, $M_{\mathrm{s1,2}}$ are implemented as long-channel devices. During the output current transition from one branch to the other, the voltage across the current source, as observed at V_{s}, is affected. This dynamic disturbance couples to the bias voltage of the current mirror through the parasitic capacitance of $M_{\mathrm{s1,2}}$, degrading the DAC settling speed and linearity. To alleviate this issue, dynamic element matching is employed to relax the matching requirements [43] and to reduce the M_{s1} size and parasitic capacitance. Moreover, to remove the dependence of the output transition on the previous DAC samples, a return-to-zero encoding is adopted here by resetting the DAC output before each conversion. The implementation of the slope generator is shown in Fig. 6(b). Similar to the current DAC, a cascode current source is employed for better linearity and reduced supply sensitivity. After the output voltage, $V_{\mathrm{O,SG}}$, has been sampled on C_{SG}, the pull-up transistor, M_{pu}, will pull the output node to the supply in order to suppress any leakage current through switch S_1 during the following steps (see Fig. 5).

A bootstrap technique, as shown in Fig. 7, is employed to implement the sampler ($S_{1,3}$) and voltage combiner (S_4) switches of Fig. 5 for the purpose of minimizing their ON-resistance. In the conventional bootstrap switch [44], [45], due to the reliability considerations of M_{10}, NMOS M_9 with its gate directly connected to supply is added to charge V_{m} to around $V_{\mathrm{DD}} - V_{\mathrm{th}}$ during the tracking phase. However, since M_9 is on the verge of turning on, its equivalent resistance is not large enough to suppress the leakage. Unlike in ADC designs, where the input is normally considered a "voltage source," the input of S_4 is stored as charge on C_{DAC} [see Fig. 5(c) and (d)]. Therefore, the leakage through M_9 causes the input level to decrease slowly during the tracking phase, ultimately leading to the nonlinearity during the ADC conversion. To overcome this, the M_9 gate is also connected to $\overline{\mathrm{CLK}}$, and M_{11} is added to pull-up V_{m} to fully turn off M_9 during the tracking phase, providing a large enough OFF-resistance. With the new design, simulations prove that V_{in} remains constant, and the initial drop due to the charge sharing with parasitic capacitance is compensated by the K_{DAC} estimation. Since V_{in} is less than 360 mV in this design, $M_{9,10}$ should not suffer from any reliability issues.

The comparator used in the SAR ADC is shown in Fig. 8(a). During the comparison (i.e., CLK = 1), the voltage perturbation at the internal nodes is coupled to the input, disturbing the input voltage and comparator's decision. To alleviate this kickback effect, dummy capacitors [see the red dotted region in Fig. 8(a)] and a sampling switch (M_{ref}) are placed at the other input of the comparator to sample the reference voltage, $V_{\mathrm{ref,samp}}$, in every reference cycle. Both V_{IN} and $V_{\mathrm{ref,samp}}$ are affected similarly by the kickback, and consequently, the comparator can decide correctly, as shown in Fig. 8(b). Moreover, the supply ripple can also couple to the comparator's inputs through the drain–source/gate–drain parasitic capacitance of $M_{\mathrm{SG}}/M_{\mathrm{ref}}$, potentially affecting the comparator's decision.

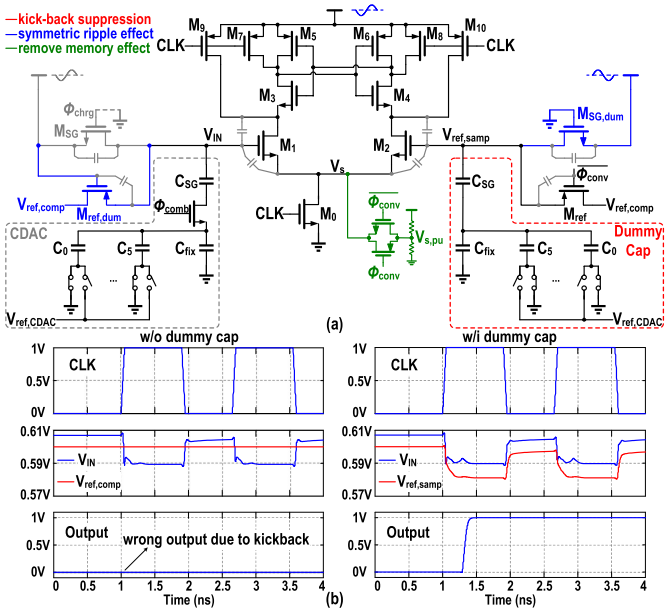

Fig. 8. (a) Schematic of the comparator in SAR ADC. (b) Simulation results of its kickback effect.

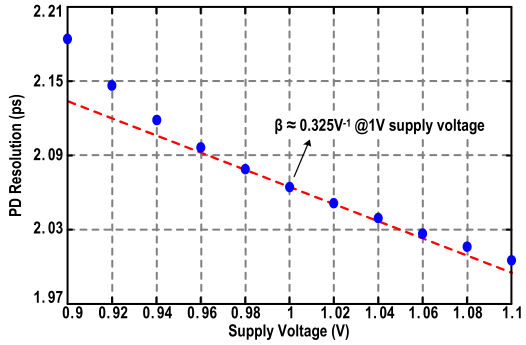

Fig. 9. Simulated supply sensitivity of the PD.

Hence, two dummy switches, $M_{SG,dum}$ and $M_{ref,dum}$, are also inserted [see the components in blue in Fig. 8(a)] such that the supply ripple appears as a common-mode (CM) voltage at the comparator's inputs, thus securing its seamless operation. Finally, the common-source node of $M_{1,2}$, V_s, is also pulled up to a fixed voltage during the charging and combining phases to remove the memory of the last conversion at the comparator's internal nodes [see the components in green in Fig. 8(a)].

Fig. 9 reports the simulated supply sensitivity of the implemented PD, reading $\beta \approx 0.325\ V^{-1}$ around the 1-V supply, which is about 3.7–6.3 times lower than that of the conventional TDC/DTC. To further improve the spur performance, a second-order $\Delta\Sigma$ modulator is employed, as discussed in Section IV-B.

B. Divider and Resampler

The oscillator's frequency is divided down by a 6-bit MMDIV, implemented by cascading six stages of divide-by-2/3 cells [46]. A second-order $\Delta\Sigma$ modulator drives the MMDIV to randomize the pattern of division ratio, thereby further suppressing the possible spurs at the intermodulation frequencies and ensuring proper convergence of the K_{DAC} calibration at near-integer channels. However, the maximum time duration in which the slope generator is active increases to $2T_{CKV}$ in this case. Hence, the dynamic range of V_{SG} is double in comparison with the first-order modulator case, thus compromising the linearity of the cascode current mirror in the slope generator. To reduce the maximum time error related to the high-order $\Delta\Sigma$ modulator, Tasca *et al.* [47] proposed to sequentially resample the divider output by the rising and falling edges of CKV with two flip-flops. Although a fixed timing relationship could be guaranteed in this way, the delay of the flip-flop could easily reach $0.5T_{CKV}$ at higher oscillation frequencies, leading to a metastability problem. In this design, the divider output is directly resampled in parallel by both the rising and falling edges of CKV (see Fig. 10). The following 2-to-1 MUX then selects between the two resampled outputs (DIV_r and DIV_f), realizing a quantization step of $0.5T_{CKV}$ and reducing the dynamic range of the slope generator to only one T_{CKV} ($\pm 0.5T_{CKV}$). The correct timing relationship is sensed by the sequence detect block and the result (R_{lead}) is provided to correctly control the divider. Besides, a tunable delay (t_d) is inserted before the rising-edge triggered resampling flip-flop and calibrated on-chip to avoid metastability. More details will be further elaborated in Section IV-C1.

The input to the $\Delta\Sigma$ modulator represents the fractional frequency ratio between the PLL output and the reference in the unit of the quantization step. Therefore, to correctly control the divider with its quantization step being halved through resampling, the input to the $\Delta\Sigma$ modulator, FCW_F, is doubled first, while the modulator output is divided by two to cancel this effect (see Fig. 4) since the divider itself is still an integer one. The integer part of the division result adds with the integer part of the frequency control word, FCW_I, to form the division ratio of MMDIV (N_{div}), while its fractional part is accumulated. By default, DIV_f leads DIV_r ($R_{lead} = 0$). Hence, the 1-bit sum of the accumulation (sel) controls the MUX to pass through DIV_r when the $0.5T_{CKV}$ time step is required, and when a carry-out signal is generated, N_{div} is further increased by 1. When DIV_r leads DIV_f ($R_{lead} = 1$), an extra 1 is added to N_{div} when DIV_r is selected to compensate for the reversed timing relation between $DIV_{f,r}$.

C. Digital Calibration

1) Calibration of t_d: Since the MMDIV is triggered by the falling edge of CKV, its output (DIV_{int}) may fall intolerably close to the CKV rising edge. Thus, a tunable delay (t_d) is inserted before the rising-edge triggered resampling flip-flop to avoid metastability. As shown in Fig. 10, the tunable delay block aligns its output (DIV_d) with the following falling edge of CKV so that the maximum setup and hold margin could be guaranteed when sampled by the CKV rising edge. To find the proper value of t_d, its control code is swept, and for each delay setting, the delayed output (DIV_d) is sampled by the falling edge of CKV to obtain the calibration input, CAL_{in}. The optimum control code is reached when CAL_{in} jumps from high to low. A similar principle is used in [48] to delay the

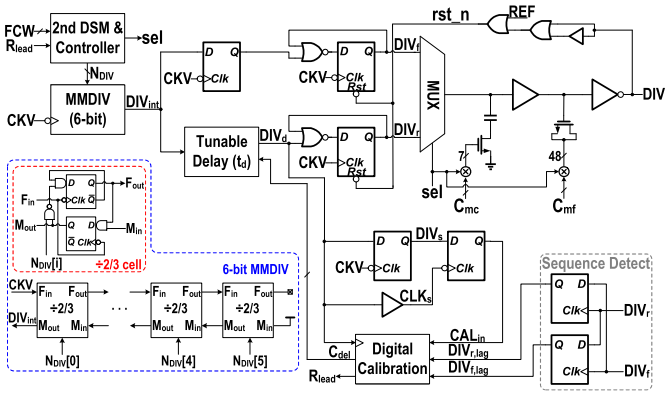

Fig. 10. Block diagram of the MMDIV and the resample system.

rising-edge triggered divider output close to the CKV falling edge so that it would not experience metastability when getting retimed by the CKV rising edge again. However, it faces a dilemma that the proper t_d value needed during the PLL locking should be obtained with the oscillator operating at the desired frequency, which is guaranteed after the loop is locked. The problem is more severe under the supply ripple since both the divider output delay and t_d are affected by the supply perturbations. Thus, due to the incorrect phase relationship between the reference and the supply ripple and the inaccurate T_{CKV}, the t_d values calibrated before the loop settles may also lead to metastability during the normal operation. In this design, $\mathrm{DIV_f}$ is guaranteed to be free of metastability through obtaining $\mathrm{DIV_{int}}$ from the $\mathrm{M_{out}}$ terminal of the first divide-by-2/3 cell (see Fig. 10) while placing the corresponding resampling flip-flop in close proximity. Hence, the locking of the loop is guaranteed by operating the $\Delta\Sigma$ modulator in the first-order mode and fixing sel to 0 initially. Then, the proper t_d values are calibrated under the correct phase relationship between the reference and the ripple. After the t_d calibration, the loop switches seamlessly to the second-order $\Delta\Sigma$ operation mode with the resampling process enabled.

The dynamic range of t_d is designed to cover at least one T_{CKV} in the fast process corner. Considering the delay variations under different process, voltage and temperature (PVT) conditions, the calibration may align DIV_d to the first or second falling edge after $\mathrm{DIV_{int}}$. Therefore, instead of only sampling $\mathrm{DIV_{int}}$ by the CKV falling edge once [47], [49], two flip-flops in cascade (see Fig. 10) perform this sampling twice so that $\mathrm{DIV_f}$ always leads or lags $\mathrm{DIV_r}$ by only $0.5T_{\mathrm{CKV}}$. The uncertainty in the timing relationship is then resolved by the sequence detect block through mutual sampling $\mathrm{DIV_{f,r}}$ by each other, and its output R_{lead} is used to correctly generate N_{div}.

If the dc supply voltage shifts after the t_d calibration, DIV_d would deviate from its optimum position, and the rising-edge triggered resampling flip-flop may re-enter its metastable state in case DIV_d becomes too close to the CKV rising edge again. However, only an intermittent re-calibration of the t_d value is sufficient considering more than 40 mV of tolerable variation of the dc supply as obtained from simulations. Meanwhile, by varying the t_d control code around the calibrated one when sel is 0, the corresponding calibration algorithm could be easily modified to operate in the background and update the t_d value when the non-optimum condition is detected.

2) Calibration of Resampler's Mismatch: In the resampling system, any mismatch between the two resampling paths, including the delay mismatch and the deviation from the 50% CKV duty cycle, would lead to spurs at f_{frac}. In [47] and [49], this mismatch is compensated by a DTC through an LMS algorithm [50]. However, in the proposed design, compensating the mismatch through the DAC would increase the dynamic range of slope generator and DAC, thus affecting their linearity performance. Meanwhile, the finer DAC resolution (∼0.5 mV for ∼0.5-ps equivalent time resolution) required for the accurate compensation also leads to a larger DAC area and power consumption due to more stringent matching requirements and more complex decoding logic. To avoid these issues, the mismatch is compensated directly at the MUX output with a bank of variable capacitors consisting of seven thermometer-coded switched capacitors for coarse-tuning and 48 thermometer-coded MOS capacitors for fine-tuning. The MOS capacitors are sized to achieve ∼0.5 ps resolution, thus guaranteeing the <−50-dBc spur level. Since, in practice, the variable capacitors only need to cover a delay range of several picoseconds, its delay step is not expected to largely deviate from the nominal value. Meanwhile, the integral non-linearity requirement of the capacitor bank is largely relaxed as long as its monotonicity is preserved.

The control codes of the variable capacitors, C_{mc} and C_{mf}, in Fig. 10, are generated through the LMS algorithm (see Fig. 4). Under a dc–dc converter supply ripple, the mismatch between the two resampling paths periodically changes, and consequently, the compensated C_{mc} and C_{mf} values must be adjusted accordingly. Note that the mismatch variation will be further sampled by the pattern of the MUX selection signal. Thus, in general, the resulting pattern is no longer located at f_{rip} and could not be tackled by the ripple pattern estimation and cancellation block introduced in the following subsection.

Since, in a practical system, the PLL reference frequency (f_{ref}) is typically provided by a highly stable crystal oscillator, it is reasonable to generate the switching frequency ($f_{\mathrm{sw}} = f_{\mathrm{rip}}$) of the dc–dc converter powering the PLL directly through dividing down f_{ref}. Hence, $f_{\mathrm{rip}} = f_{\mathrm{ref}}/n$ ($n = 1, 2, 3, \ldots$), where the integer n represents the division ratio of the corresponding frequency divider. Though the highest f_{sw} is limited to f_{ref} under this arrangement, an even higher f_{sw} would not be preferred due to the complexity of an extra block required to generate f_{sw}. Meanwhile, f_{sw} should also be chosen carefully, balancing the tradeoff between the increase in losses of converter switching and clock distribution at the upper f_{sw} end and the sheer complexity of the frequency divider with a large division ratio at the lower end. Bearing these in mind, for $f_{\mathrm{ref}} = 50$ MHz in this design, we selected f_{sw} to be equal to f_{ref} divided by 3, 6, or 12. Therefore, the mismatch pattern repeats itself every n ($n = 3$, 6, or 12 in this design) reference cycles. As a result, n separate LMS loops are used to calibrate C_{mf}, with the ith ($i = 1, \ldots, n$) loop calibrating C_{mf} of the $k \times n + i$ ($k = 1, 2, 3, \ldots$) reference cycles. Such an arrangement would guarantee proper compensation even under the pessimistic assumption that the mismatch could vary by

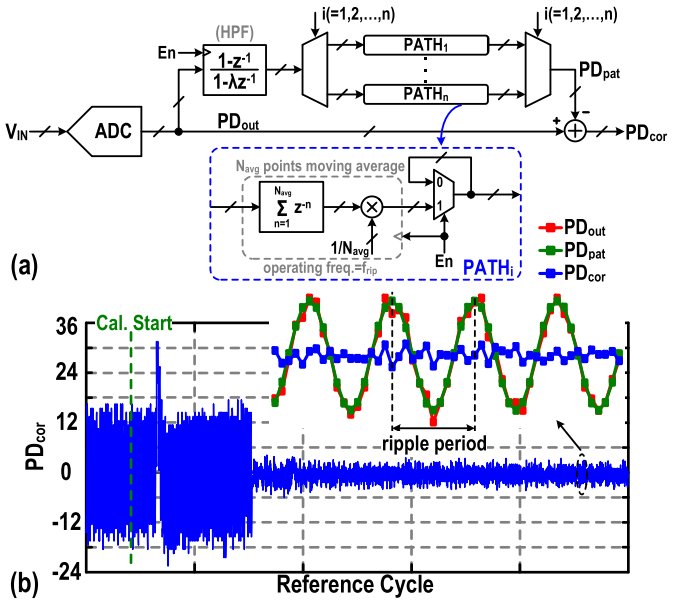

Fig. 11. (a) Block diagram of the ripple pattern estimation and cancellation. (b) Example of calibration waveform with $f_{\text{rip}} = f_{\text{ref}}/12$.

a large amount under the 50-mV_{pp} supply ripple considered here. Another LMS loop is also implemented to calibrate an average C_{mc} code for all reference cycles to simplify the calibration process. The detailed operation of the calibration process will be further discussed in Section IV-C4.

3) Ripple Pattern Estimation and Cancellation: As discussed in Section II-B, the output delay perturbations of MMDIV and resample flip-flops caused by the supply ripple are sensed by the PD, and thus, they appear as spurs at the DPLL output. The subsequent pattern estimation and cancellation block, shown in Fig. 11, is used to suppress this effect. Since the SAR ADC output, PD_{out}, shows a periodic digital pattern at f_{rip} due to supply-induced delay variations, the task of this digital block is to extract this pattern and subtract it from PD_{out} before modulating the oscillator. To do so, n $(= f_{\text{ref}}/f_{\text{rip}})$ branches (PATH_{i} in Fig. 11), each storing one different point of PD_{out}, are rotationally enabled. The N_{avg}-point moving-average filter in PATH_{i} is employed to suppress the random noise component in PD_{out} to guarantee accurate estimation of the f_{rip} pattern. A high-pass filter (HPF) is also inserted at the front. The HPF avoids the detected phase error at low-frequency offsets from entering the calibration loop and affecting the generated pattern PD_{pat}. Hence, the PN performance of the DPLL at low-frequency offsets would not be affected by this calibration. A similar algorithm is employed in [51] to suppress the fractional or external DPLL spurs, consuming ~2 mW for each calibration loop. In contrast, $f_{\text{ref}}/f_{\text{rip}}$ in this design is a known integer determined during system planning, allowing us to avoid the need for the complex fractional delay filter and the extra calibration loop to optimize the filter coefficient, as in [51], resulting in a much lower power consumption. Meanwhile, after the accurate PD_{pat} is obtained, the extraction process is also turned off by disabling the enable signal (En). After that, only the output of each branch is preserved with all other calculations in the calibration loop disabled, which further reduces the

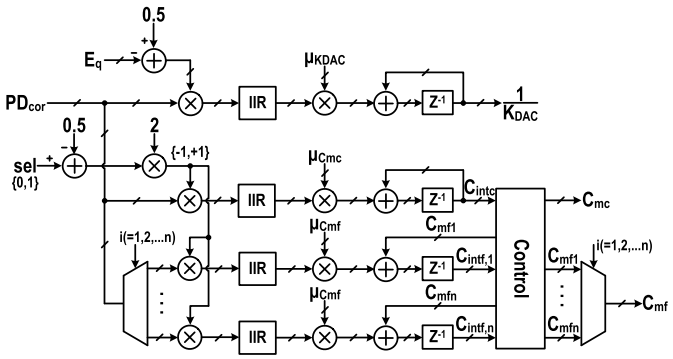

Fig. 12. Block diagram of the LMS calibration loops for the DAC gain and resampler's mismatch.

current consumption to ~80 μA. Compared to the ~2 mW consumed by the loop components, the power efficiency is thus only degraded by ~4%. The extraction process may also keep operating in the background to track environmental changes if needed, raising the power consumption to ~190 μA. Otherwise, a simple digital threshold detector could be implemented to monitor PD_{cor} and only trigger the extraction process when PD_{cor} exceeds the predefined threshold value, lowering the extra power penalty.

Note that the algorithm cannot suppress the effect of supply noise. Hence, the PN induced by the supply noise is determined by the intrinsic supply sensitivity of the circuit, which is similar to conventional designs. Meanwhile, in the practical setting, the dc–dc converter typically shows a much lower output noise compared to LDOs [52]–[55], thus posing no significant degradation to the loop performance.

4) Co-Operation of Calibration Loops: The detailed block diagram of the LMS loops calibrating K_{DAC} and $C_{\text{mc/f}}$ is shown in Fig. 12. The error signal, PD_{cor}, is cross-correlated with $(0.5 - E_q)$ and also with the selection signal (sel) of the resampler's MUX. A simple first-order IIR filter follows to attenuate non-dc components after the correlation. Note that it is the inverse of K_{DAC}, $1/K_{\text{DAC}}$, that is actually being estimated so that the calculation of n_{DAC} is realized with a multiplier instead of a divider, thus saving power consumption and hardware. The estimation of the coarse C_{mc} and fine C_{mf} control codes is completed in two steps. First, the controller enables the LMS loop to calibrate for an average C_{mc} value over a predefined number of reference cycles. C_{mc} is then fixed and the corresponding LMS loop disabled while starting the calibration of the fine-tuning code C_{mf}. As discussed in Section IV-C2, C_{mf} is estimated cyclically through $n = f_{\text{ref}}/f_{\text{rip}}$ LMS loops (see Fig. 12), with the ith $(i = 1, \ldots, n)$ loop correlating the PD_{cor} and the sel signal of the $k \times n + i$ $(k = 1, 2, 3, \ldots)$ reference cycles. The individual results, $C_{\text{intf,i}}$, are monitored by the controller and directly passed onto C_{mfi} to form the C_{mf} sequence if they remain within the [0, 48] range. When the limits are exceeded, the controller adds/subtracts 32 to/from $C_{\text{intf,i}}$ to generate the corresponding C_{mfi} while decreasing/increasing C_{mc} by two for the $k \times n + i$ reference cycles. Therefore, the fine-tuning range is extended with a minimal disturbance introduced during the LMS calibration process.

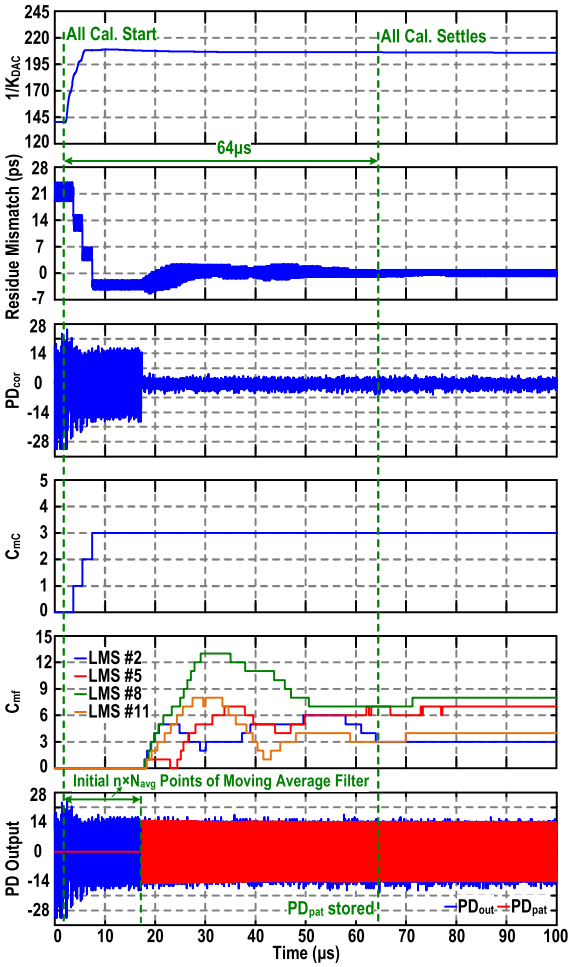

Fig. 13. Convergence trajectory of the calibration process with $f_{\text{rip}} = f_{\text{ref}}/12$.

Fig. 13 shows the simulated convergence trajectory of the calibration process with $f_{\text{rip}} = f_{\text{ref}}/12$. The induced mismatch is large to clearly demonstrate the settling behavior. In general, the implemented calibration loops could operate in parallel without a dedicated calibration sequence due to the difference in signal patterns they operate on: The signals that PD_{cor} is correlated with are related to f_{frac}, with $(0.5-E_q)$ showing the high-pass shaped noise spectrum of the $\Delta\Sigma$ modulator and the sel signal being rich in discrete tones at f_{frac} and its harmonics, while the ripple pattern cancellation algorithm extracts the pattern at f_{rip}. To increase the settling speed, a larger integration step ($\mu_{\text{KDAC},0}$ and $\mu_{\text{Cmf},0}$) is employed initially and then gear-shifted to their final values of $\mu_{\text{KDAC},0}/32$ and $\mu_{\text{Cmf},0}/32$ in two steps under the control of a reference cycle counter in order not to affect the loop performance during the normal operation. As shown in Fig. 13, the settling time of the whole calibration process is ∼64 μs and is dominated by the C_{mf} calibration. For special cases of f_{frac} being close to f_{rip} or its harmonics, the frequency of the sel pattern becomes related to f_{rip}, and the interaction between the $C_{\text{mc/f}}$ calibration and the ripple pattern cancellation could impede the proper loop convergence. However, the problem could be avoided by disabling the $C_{\text{mc/f}}$ calibration in this scenario, while the ripple pattern estimation and cancellation block could cancel the effects of both the supply-induced delay perturbation and the resampler's mismatch that is small enough as not to saturate the PD output.

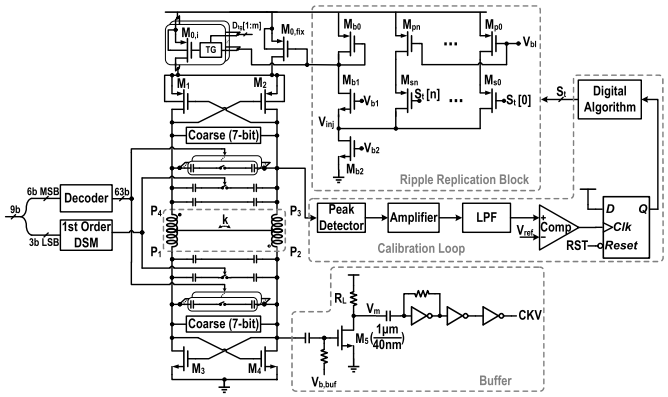

Fig. 14. Schematic of the *LC* oscillator with its calibration loop.

D. LC Oscillator and Supply Pushing Calibration

The structure of the complementary *LC* oscillator is shown in Fig. 14. It consists of 7-bit 5.2-MHz/LSB binary and 63-bit 125-kHz/LSB unary switched capacitors for coarse and fine frequency tuning, respectively. An extra switched capacitor controlled by a first-order $\Delta\Sigma$ modulator is also added to further improve the frequency resolution to ∼15 kHz. The first stage of the oscillator's buffer is implemented by an NMOS common-source amplifier with a load resistor. A tiny NMOS is intentionally used in this stage so that the variation of its input parasitic capacitance due to the supply ripples would not affect the oscillator's performance. Three stages of self-biased inverters then generate a rail-to-rail square wave that drives the MMDIV and the resampling flip-flops.

Similar to [16], a ripple replication block (RRB), controlled by the 6-bit $S_{\text{t}}[5:0]$ from the calibration loop, is designed to replicate the supply ripple to the gate of M_0 with a proper gain to stabilize the oscillator tail current and reduce its supply pushing. M_0 is implemented as a parallel combination of a fixed part, $M_{0,\text{fix}}$, with a bank of switchable unit transistors, $M_{0,i}$, to tune the tail current and, correspondingly, the oscillation swing. Compared to the conventional integration of an LDO with a current-biased oscillator in which the pass transistor of the LDO, M_{pass}, should be placed above the tail current source, the proposed technique performs both supply regulation and current tuning with only one transistor, thus saving the extra voltage headroom consumed by M_{pass}. Merging the tail transistor with M_{pass} might also reclaim the extra headroom, but the oscillator would then become voltage-biased whose current would be poorly controlled over PVT variations. Meanwhile, higher supply sensitivity of a voltage-biased oscillator could place higher demands on the PSR performance of the LDO, further degrading its power efficiency.

The calibration loop first detects and amplifies the variation of the oscillation amplitude. A digital algorithm then determines the optimum code to minimize that amplitude variation, thereby reducing spurious tones. The reduced supply pushing

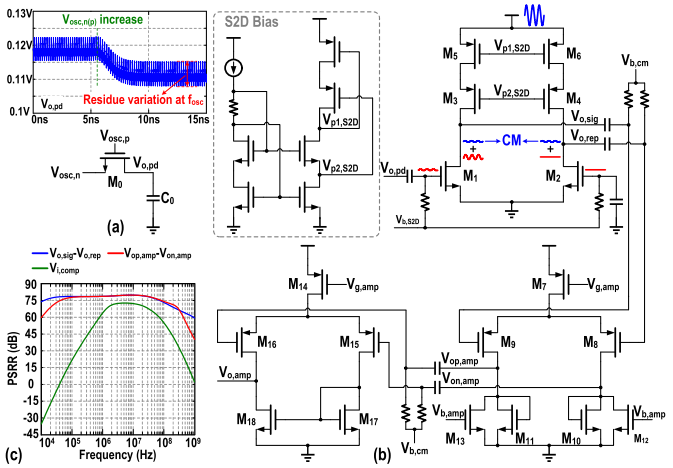

Fig. 15. Schematic of (a) peak detector and (b) amplifier chain in the oscillator calibration loop. (c) Simulated PSRR of the loop.

is also beneficial in significantly suppressing the conversion of thermal noise of supply to PN. Foreground calibration is selected due to the relatively relaxed spur requirement of the targeted applications (i.e., <-50 dBc) and the slow supply and temperature drifts of a low-power system whose effect could be compensated with intermittent recalibrations. In [16], the calibration loop needs to be powered with a clean supply to operate correctly. In this work, we tackle this issue by modifying the structure of the peak detector and amplification chain.

Fig. 15(a) shows the peak detector, consisting of an NMOS transistor, M_0, and a load capacitor, C_0. The gate and source terminals of M_0 are driven by the oscillator's differential output, $V_{\text{osc},n(p)}$. Hence, M_0 acts as a switch and approximately turns ON for half of the oscillator cycle when $V_{\text{osc},p} \geq V_{\text{osc},n} + V_{\text{th}}$. During this phase, the low-pass filter formed by M_0 ON-resistance and C_0 filters out the high-frequency components and extracts the average value of this half-cycle, leading to a peak detection gain of $\sim 1/\pi$. Since the peak detector is not connected to the supply, its performance is not affected by the supply ripple.

Fig. 15(b) shows the amplifier chain located between the peak detector and comparator. Similar to the DAC current source, the first amplifier stage is implemented with a cascode PMOS current mirror for a higher PSR ratio (PSRR). We now inspect the outputs of the first-stage amplifier. The supply ripple and the peak detector voltage appear as CM and differential-mode (DM) signals, respectively. Therefore, when these signals are sent to the following differential amplifier stages, the desired signal is further amplified, while the supply-induced variations are suppressed by their CM rejection ratio (CMRR). As can be gathered from simulation results in Fig. 15(c), PSRR is higher than 60 dB at the comparator's input over the desired frequency range (i.e., 2–20 MHz), enough for the calibration loop to function correctly under the 50-mV_{pp} ripple.

V. Measurement Results

The proposed fractional-N DPLL is implemented in TSMC 40-nm 1P8M CMOS without the customary ultra-thick metal layers. Fig. 16 shows the chip micrograph. The DPLL has an active area of 0.39 mm^2, in which the oscillator, the current DAC, and the digital part occupy 0.157, 0.14, and 0.056 mm^2, respectively. Powered by a 1.0-V supply, the whole loop consumes 3.25 mW (1.02 mW for digitally controlled oscillator (DCO), 0.92 mW for PD, and 0.63 mW for the digital part).

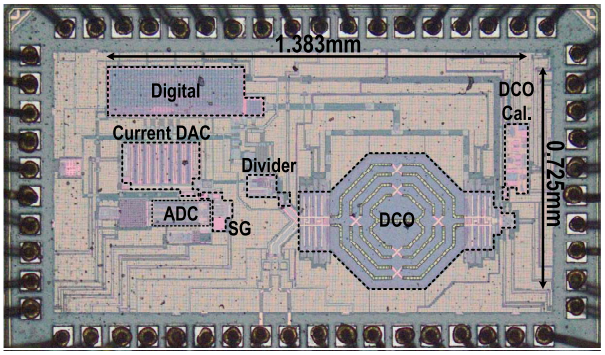

Fig. 16. Chip micrograph of the DPLL.

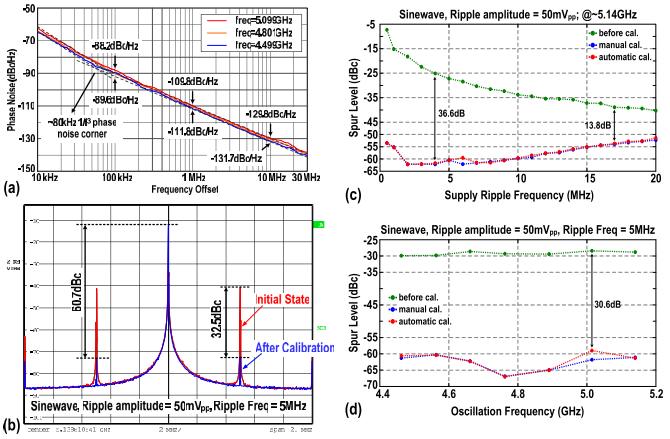

Fig. 17. Measurements of the free-running DCO: (a) PN across the TR; (b) spectrum before and after the automatic calibration in face of a 50-mV_{pp} 5-MHz sinusoidal ripple. Spur levels across (c) ripple frequency and (d) oscillation frequency for both the manual and automatic calibrations.

The DPLL is first set to an open-loop mode to measure the performance of the free-running DCO. The measured tuning range (TR) is 4.47–5.14 GHz. Fig. 17(a) shows the measured PN performance across the TR. PN varies from -109.8 to -111.8 dBc/Hz at the 1-MHz offset, with a flicker noise corner around 80 kHz. The effectiveness of the modified calibration loop is verified in Fig. 17(b)–(d). In these measurements, a 50-mV_{pp} sinewave ripple is applied to the supply of the oscillator core and its calibration loop. Fig. 17(b) compares the oscillator spectrum before and after the calibration. Under the 50-mV_{pp} 5-MHz supply ripple, the measured spur level is reduced by 32.5 dB and reaches -60.7 dBc after the calibration. Fig. 17(c) shows the measured spur level over the frequency of the supply ripple. The oscillator exhibits lower than -51-dBc spur level with the 0.5–20-MHz 50-mV_{pp} supply ripples, while the calibration loop is able to successfully find the optimum operating point in most cases. The improvement after the automatic calibration is between 13.8 and 36.6 dB for 4–17-MHz ripples. The rise of the spur level after the calibration at higher f_{rip} is due to the limited bandwidth of

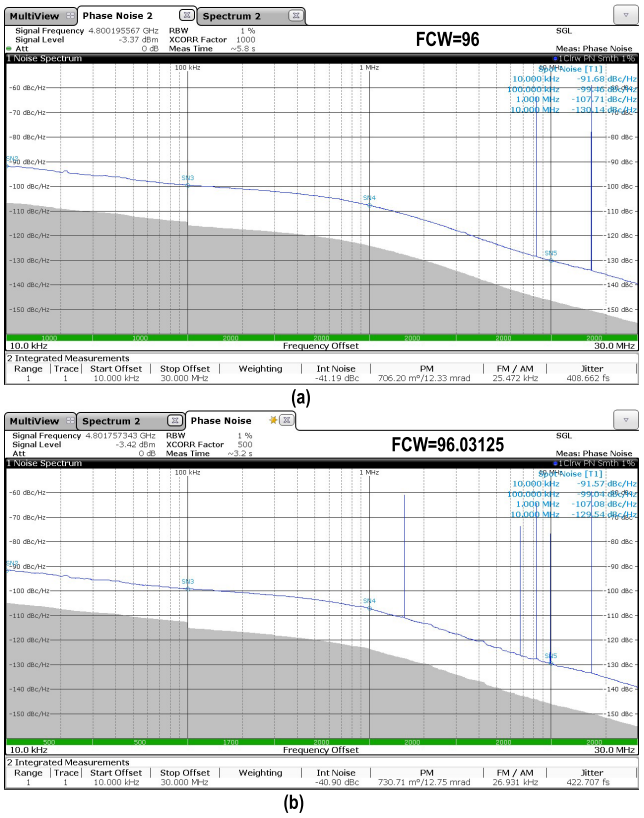

Fig. 18. Measured DPLL PN at (a) integer-*N* and (b) fractional-*N* channels around 4.8 GHz.

RRB since a phase shift between the supply ripple and its replica would result in a partial cancellation of the oscillator's tail current variation [16]. In Fig. 17(d), the spur level is measured across the oscillator TR. The worst case spur level under the 50-mV$_{pp}$ 5-MHz ripple is ≤ -59 dBc, while the calibrated value also follows the optimum one successfully on most occasions. The improvement after the calibration is higher than 30 dB across the TR.

The DPLL is measured with a 50-MHz external crystal reference clock and under the 50-mV$_{pp}$ supply ripple. Fig. 18 shows the measured PN plot for both the integer-*N* and fractional-*N* channels around 4.8 GHz when $f_{rip} = f_{ref}/6$. The rms jitter integrated from 10 kHz to 30 MHz is 423 fs for the fractional-*N* operation and 409 fs for the integer-*N* operation.

The DPLL output spectrum is measured in three different scenarios. In Fig. 19(a), a 50-mV$_{pp}$ 4.167 MHz (i.e., $f_{ref}/12$) ripple is applied to the oscillator and its calibration loop. The spur at f_{rip} due to the oscillator supply pushing is suppressed by 37 dB and reaches −62.7 dBc after the corresponding calibration is performed. The same ripple is then applied to the DPLL components except for the oscillator. As shown in Fig. 19(b), the spur at f_{rip} due to the delay variations of the loop components is −61.5 dBc, improving 31.6 dB due to the ripple pattern estimation and cancellation technique. Finally, the same ripple is applied to the entire DPLL. As shown in Fig. 19(c), when all calibration loops are enabled, the f_{rip} spur is reduced by 34.4 dB and reaches −60.5 dBc. In all three cases, the spur at f_{frac} due to the residue mismatch of the resampling block is <-60 dBc after the mismatch calibration, while the spur at $2 \times f_{frac}$ originating from the nonlinearity of PD remains <-71.6 dBc. Extra spurs at $f_{rip} \pm f_{frac}$ and $2f_{rip} \pm f_{frac}$ with levels <-66 dBc could also be observed in Fig. 19(b) and (c). These spurs come from the undesired coupling between the supply of PD and the DCO output, both routed on the top metal layers with only $\sim 10\ \mu$m spacing, and could also be observed when the oscillator is left free-running. In contrast, these spurs disappear when no ripple is applied to the PD supply. To suppress these spurs, the distance between the PD and the oscillator should be increased in future designs.

Similar measurements are performed when the frequency of the 50-mV$_{pp}$ ripple is increased to $f_{ref}/3$ (i.e., 16.67 MHz). As can be gathered from Fig. 19(d)–(f), the f_{rip} spur is dominated by the oscillator supply pushing since the spur level due to the delay variations of the DPLL components is further suppressed by the low-pass transfer function of the loop. Fig. 20 shows the measured spur level at f_{frac} and $2f_{frac}$ across the fractional frequency, indicating that the mismatch calibration improves the in-band (out-of-band) f_{frac} spur level by about 9–14 dB (3–7 dB). Furthermore, considering both f_{frac} and $2f_{frac}$ spurs, a worst case spur level of −55 dBc is achieved after the calibration.

The oscillator and the DPLL are also measured under sawtooth ripples to better mimic the actual scenario of being directly powered by a switched-mode dc–dc converter. Fig. 21 shows the measured performance of the free-running DCO when a 50-mV$_{pp}$ sawtooth ripple is applied to both the oscillator core and the calibration loop. Fig. 21(a) compares the oscillator spectrum before and after the calibration. At a 5-MHz ripple, the spur at the fundamental offset is reduced by 26.8 dB and reaches −57.3 dBc after the calibration. Fig. 21(b) plots the measured spur levels over the ripple frequency. In the entire span of 0.5–20 MHz, the highest spur is ≤ -46.8 dBc. The observed improvement after the automatic calibration is 13.3–24.6 dB for 4–17 MHz ripples. The entire oscillator TR was also scanned and the worst case spur level is ≤ -57.3 dBc under a 50-mV$_{pp}$ 5 MHz sawtooth ripple; the calibrated value follows the optimum one in most cases. The improvement after the calibration is >26 dB across the TR.

Fig. 22 shows the measured PN and spurious performance for the fractional-*N* operation around 4.8 GHz under the 50-mV$_{pp}$ sawtooth ripple when $f_{rip} = f_{ref}/6$. The integrated jitter is 428 fs for the fractional-*N* operation, while it is 411 fs for the integer-*N* operation. As expected, the PN performance of the DPLL under sawtooth ripples remains similar to that measured with sinusoidal ripples.

The measured output spectrum of the DPLL under a 50-mV$_{pp}$ 4.167-MHz (i.e., $f_{ref}/12$) sawtooth ripple is shown in Fig. 23. Compared to the initial state where no calibration is performed, the spurs at f_{rip} and its harmonics induced by the ripple on the oscillator supply are suppressed after the supply pushing calibration, and the levels of these spurs are now mainly dominated by the variation of the output delay of loop components [see Fig. 23(a)]. When the ripple pattern estimation and cancellation algorithm is enabled, the spectrum in Fig. 23(a) shows that the spur at f_{rip} is suppressed significantly, while the spurs at its harmonics are also lowered.

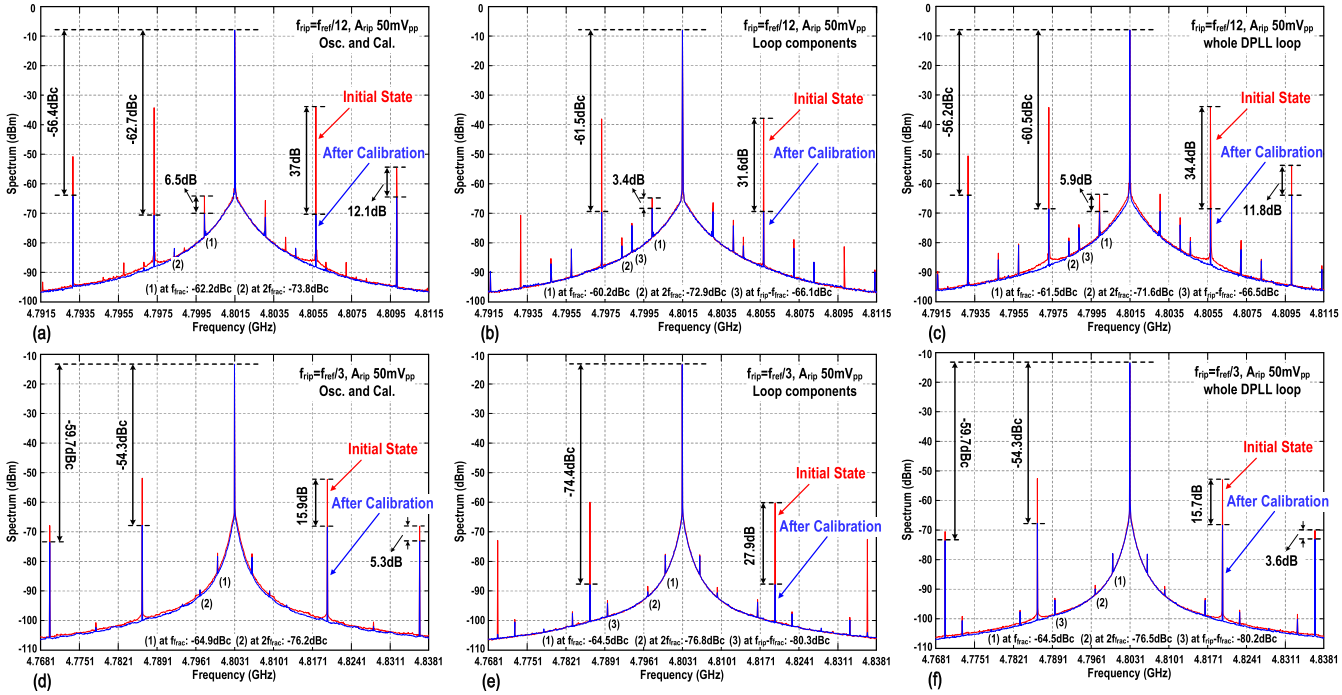

Fig. 19. Measured DPLL spectra when the 50-mV$_{pp}$ $f_{ref}/12$ ($f_{ref}/3$) supply ripple is applied to (a) (d) oscillator and its calibration loop, (b) (e) loop components, and (c) (f) whole DPLL.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

		This Work			TCAS-II'12 [17]	TCAS-I'14 [2]	ESSCIRC'16 [11]	VLSI'17 [12]			ISSCC'16 [7]	JSSC'18 [38]	JSSC'21 [42]	TCAS-I'19 [41]	JSSC'21 [29]
Tech. (nm)		40 (w/o UTM)			90	65	65	65			40	65	45 (PDSOI)	130	130
PLL Type		Digital Frac-N			Digital Int-N	Digital Int-N	Digital Int-N	Digital Int-N			Digital Int-N	Digital Frac-N	Analog Frac-N	Analog Frac-N	Analog Frac-N
Osc. Type		LC			Ring	LC	LC	Ring			Ring	LC	LC	LC	LC
Ripple applied to		whole loop			whole loop	GRO PD	Osc.	Osc.			Osc.	-	-	-	-
Cancellation Tech.		SAR ADC based PD Ripple pattern cal. Feedforward K_{push} cal.			Cancel osc. supply noise through opposite sensitivities	GRO based supply noise monitor	FCW compensation	Noise suppression loop			Two constant-Gm biasing	-	-	-	-
V_{DD} (V)		1.0			0.6	1.0	1.0	1.0			1.1	1.0/0.8	1.0	1.2	1.2
f_{ref} (MHz)		50			50	26	30	50			200	26×2	100	50	50
f_{out} (GHz)		4.47-5.14			0.8	1.4-1.8	3-5	3.2			3.2	2.0-2.8	7.7-9.1	1.9-2.3	1.8-2.3
PN (dBc/Hz)	In-band	-99.1 (@100kHz)			NA	-74## (@50kHz)	-103† (@100kHz)	-86.3 (@10kHz)			-105† (@3MHz)	-103.8 (@100kHz)	-120### (@1MHz)	-110.3 (@200kHz)	-109.2 (@200kHz)
	Out-band	-117.5 (@3MHz)			NA	-98## (@1MHz)	-120† (@3MHz)	-108 (@10MHz)			-119† (@100MHz)	-128.0 (@10MHz)	-135### (@10MHz)	-127.9 (@2MHz)	-132† (@10MHz)
PN_{norm}* (dBc/Hz)	In-band	-99.1 (@100kHz)			NA	-58.8## (@50kHz)	-100.4† (@100kHz)	-82.8 (@10kHz)			-101.5† (@3MHz)	-97.9 (@100kHz)	-118.3### (@1MHz)	-103.6 (@200kHz)	-102.0 (@200kHz)
	Out-band	-117.5 (@3MHz)			NA	-82.8## (@1MHz)	-117.4† (@3MHz)	-104.5 (@10MHz)			-115.5† (@100MHz)	-122.2 (@10MHz)	-133.3### (@10MHz)	-121.2 (@2MHz)	-124.9† (@10MHz)
Integrated Jitter (ps)		0.428			34.1#	NA	0.52	7.8			3.85	0.53	0.135	0.291	0.414
Frac. Spur (dBc)		<-55			-	-	-	-			-	<-56	<-55####	<-48.6	-57
Frac. $Spur_{norm}$** (dBc)		<-55			-	-	-	-			-	<-50.1	<-47.9	<-41.9	-49.9
Ripple Amplitude		50mV_{pp}			50mV_{pp}	200mV_{pp}	NA	20mV_{pp}			50mV_{pp}	-	-	-	-
f_{rip} (MHz)		$f_{ref}/12$	$f_{ref}/6$	$f_{ref}/3$	1-100	1.0	0.5-10	0.5	2.5	20	0.1	-	-	-	-
Spur @ f_{rip} (dBc)	sinewave	-60.5	-61.6	-54.3	NA	-49##	NA	-63	-45.5	-59.2	-28†	-	-	-	-
	saw-tooth	-59.7	-64.4	-57.6	NA	NA	<-50	NA	NA	NA	NA	-	-	-	-
Power (mW)		3.25			0.66	11.3	21.3	2.73			2.915	0.98	4.5	3.2	2.8
FoM_R*** (dB)		-242.3			-211.1	NA	-234.6	-217.8			-217.6	-245.4	-247.8	-245.7	-243.2
Area (mm^2)		0.39			0.0221	0.65	0.63	0.047			0.0216	0.23	0.1‡	0.45	0.4

*Phase noise normalized to 4.8GHz, $PN_{norm}=PN+20\times\log_{10}(4.8GHz/f_{out})$ **Spur level normalized to 4.8GHz, $Spur_{norm}=Spur+20\times\log_{10}(4.8GHz/f_{out})$ ***$FoM_R=10\times\log_{10}((\sigma_{rms})^2\times Power/1mW\times(f_{ref}/50MHz))$ [56]
#Measured at 280MHz output (f_{ref}=17.5MHz) ##Measured after divide by 2 at 832MHz †Estimated from measurement result ‡Excluding the integrated loop filter
###Estimated from measurement after divide by 2 at ~3.95GHz ####Measured after divide by 4 at ~2.12558GHz

In contrast, the spur level at f_{frac} remains unaffected during these calibrations. To suppress this spur, the mismatch calibration is then enabled, and the spur level at f_{frac} is reduced from −54.5 to −60.4 dBc, as shown in Fig. 23(b). During the mismatch calibration, the levels of spurs at f_{rip} and its harmonics remain unchanged. The spur level at $2f_{frac}$ due to the PD nonlinearity also remains at ∼−72.6 dBc during these calibrations.

Table I summarizes the performance of the proposed DPLL and compares it with state-of-the-art designs. We first compare the performance of the prototype under supply ripple to state-of-the-art low-power (<5 mW) fractional-N PLLs

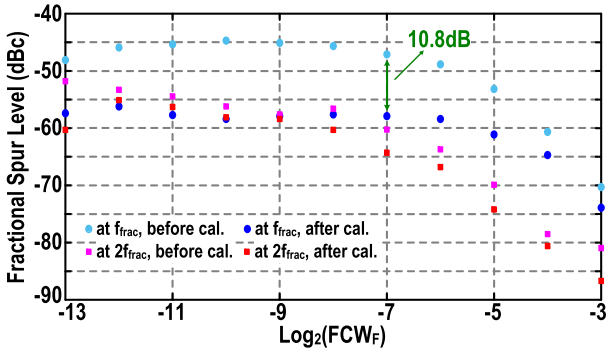

Fig. 20. Measured fractional spur levels versus fractional FCW (FCW_F).

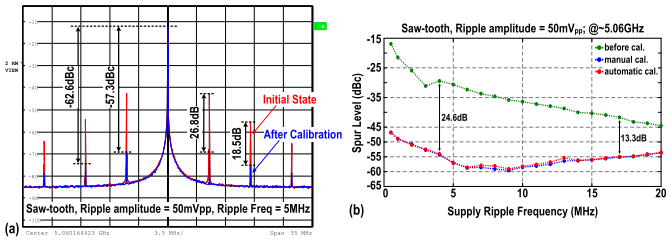

Fig. 21. Measurements of the free-running DCO under sawtooth ripples: (a) spectrum before and after the automatic calibration in face of a 50-mV_{pp} 5-MHz ripple; (b) worst case spur levels across the ripple frequency for both the manual and automatic calibrations.

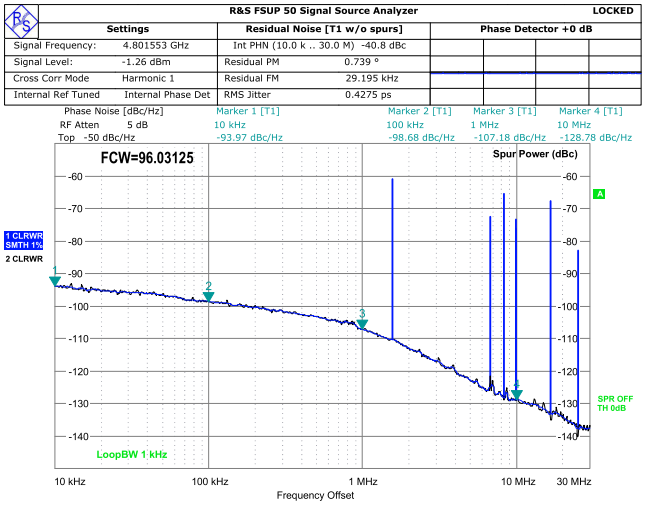

Fig. 22. Measured DPLL PN at the fractional-*N* channel around 4.8 GHz under sawtooth ripples.

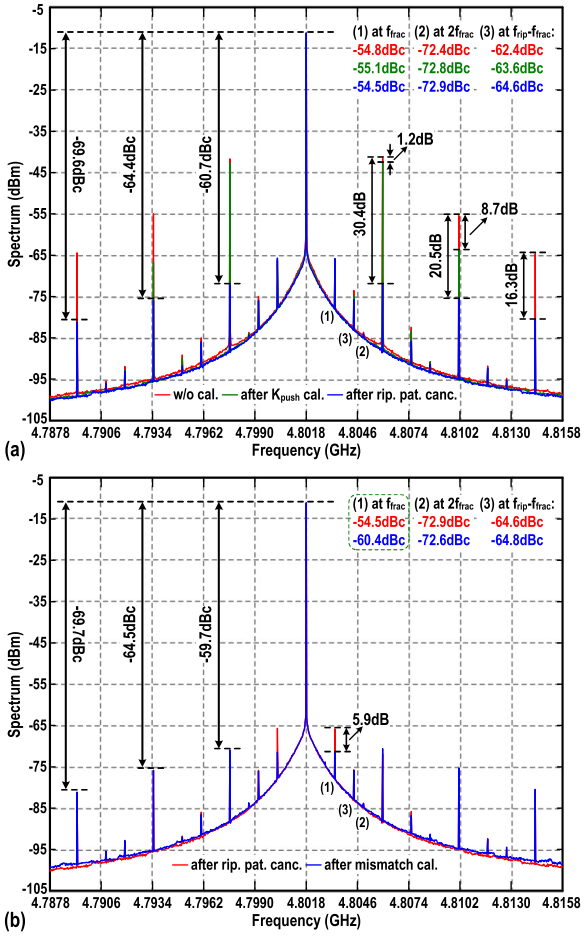

Fig. 23. Measured DPLL spectrum under a 50-mV_{pp} $f_{ref}/12$ sawtooth ripple at the initial state [red curve in (a)] and after enabling the oscillator supply pushing calibration [green curve in (a)], after enabling the ripple pattern estimation and cancellation [blue curve in (a) /red curve in (b)], and after enabling the divider resampler mismatch calibration [blue curve in (b)] sequentially.

under a clean supply [29], [38], [41], [42]. The normalized FoM (FoM_R, defined at the bottom of Table I) is ∼3 dB worse compared to [38] and [41], while it is ∼5 dB worse compared to [42] implemented in the silicon on insulator (SOI) technology. This is partly due to the fact that no ultra-thick top metal layer is available in the technology used, limiting the *Q*-factor of the DCO. Moreover, in order not to offset the advantages of removing the LDOs, no external capacitor is used to filter out the noise of the biasing current in the slope generator and current DAC; this, however, increases the contribution of PD's circuit noise to the in-band PN by about 40% as per simulations. In contrast, for example, the design in [42] uses several external tunable reference voltages to charge/discharge the capacitors in its sampling PD and the following CDAC, which is difficult to integrate on-chip. Next, our prototype is compared to designs with "dirty" supplies [2], [7], [11], [12], [17]. The f_{rip} spur of the prototype is the lowest under a large 50-mV_{pp} supply ripple. Meanwhile, to the best of our knowledge, the proposed design is the first fractional-*N* PLL that can successfully operate under the supply ripples with acceptable performance.

VI. Conclusion

This article demonstrates a fractional-*N* DPLL that is insensitive to supply ripples, thereby enabling a direct connection to a dc–dc converter. To tolerate the supply ripple, the feedforward ripple replication and cancellation technique with an improved calibration loop is adopted to reduce the supply pushing of the *LC* oscillator. The output of the MMDIV, which is driven by a second-order $\Delta\Sigma$ modulator, is resampled by both edges of the oscillator output to halve the input range of the following slope generator. This facilitates a linear and supply-insensitive conversion from time to voltage domain by the slope generator. Meanwhile, a current DAC compensates

for the excursion due to the fractional-N operation in order to limit the dynamic range of the SAR ADC that quantizes the phase error. A ripple pattern estimation and cancellation algorithm is integrated to cancel the phase error induced by the delay variations of the loop component under the supply ripple from the ADC output so that it would not modulate the oscillator. Prototyped in 40-nm CMOS, the DPLL exhibits 428-fs rms jitter and <-55-dBc fractional spur, while the ripple spur is also <-54 dBc.

APPENDIX A

Since the supply perturbation is relatively small, it is reasonable to assume that the delay variation, Δt_{VDD}, is proportional to the ripple amplitude A_{rip}, i.e.,

$$\Delta t_{\mathrm{VDD}} = K_{\mathrm{VDD}} A_{\mathrm{rip}}. \tag{12}$$

Hence, the peak-to-peak phase deviation presented at the PD input is

$$\Delta\phi_{\mathrm{VDD}} = 2\pi \cdot \frac{K_{\mathrm{VDD}} A_{\mathrm{rip}}}{T_{\mathrm{CKV}}} \tag{13}$$

inducing an extra phase variation at the PLL output with a peak-to-peak amplitude of

$$\Delta\phi_{\mathrm{VDD,out}} = 2\pi \cdot \frac{K_{\mathrm{VDD}} A_{\mathrm{rip}}}{T_{\mathrm{CKV}}} \cdot 10^{\mathrm{TF_{loop}}/20}. \tag{14}$$

Note that ϕ_{VDD} is normalized to f_{osc} directly, and thus, $\mathrm{TF_{loop}} \approx 1$ at low frequency offsets, as shown in Fig. 1(b). Instead, if ϕ_{VDD} is normalized to f_{ref}, $\mathrm{TF_{loop}}$ should be multiplied by the division ratio, resulting in the same expression shown in (14). Based on (14), the output signal of the PLL, x_{PLL}, is expressed as

$$x_{\mathrm{PLL}} = A_{\mathrm{osc}} \sin\left(\omega_{\mathrm{osc}} t + \frac{\Delta\phi_{\mathrm{VDD,out}}}{2} \sin\left(\omega_{\mathrm{rip}} t\right)\right) \tag{15}$$

where A_{osc} is the amplitude of CKV. Given that $|\phi_{\mathrm{VDD,out}}|$ is typically much less than $\pi/6$, (15) could then be approximated as

$$x_{\mathrm{PLL}} \approx A_{\mathrm{osc}} \sin(\omega_{\mathrm{osc}} t) + A_{\mathrm{osc}} \cdot \frac{\Delta\phi_{\mathrm{VDD,out}}}{4} \cdot \left(\sin[(\omega_{\mathrm{osc}} + \omega_{\mathrm{rip}})t] - \sin[(\omega_{\mathrm{osc}} - \omega_{\mathrm{rip}})t]\right). \tag{16}$$

Combining (16) and (14), the spur level induced by the delay variation of MMDIV under supply ripple is calculated as

$$\begin{aligned} S_{\mathrm{dly}} &= 20 \cdot \log_{10}\left(\frac{\phi_{\mathrm{VDD,out}}}{4}\right) \\ &= 20 \cdot \log_{10}\left(\frac{\pi \cdot K_{\mathrm{VDD}} \cdot A_{\mathrm{rip}}}{2T_{\mathrm{CKV}}}\right) + \mathrm{TF_{loop}} \end{aligned} \tag{17}$$

which is the very result presented in (2).

APPENDIX B

As shown in (5), the output delay of DTC is modulated by the supply ripple as

$$\Delta t_{\mathrm{DTC}} = T_{\mathrm{CKV}} \cdot \mathrm{sawtooth}\{\omega_{\mathrm{frac}} t\}\left(1 + 0.5\beta \mathrm{A_{rip}} \sin(\omega_{\mathrm{rip}} t)\right) \tag{18}$$

in which $\mathrm{sawtooth}\{\omega_{\mathrm{frac}} t\}$ represents the sawtooth waveform with a fundamental frequency of f_{frac} and a peak-to-peak magnitude of 1. Its Fourier series is

$$\mathrm{sawtooth}\{\omega_{\mathrm{frac}} t\} = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{1}{n\pi} \cdot \sin(n\omega_{\mathrm{frac}} \mathrm{t}). \tag{19}$$

The first term in (19) corresponds to a delay offset, which cancels with the dc value of the delay between REF and DIV in the locking state and can be ignored in the following analysis. The second term of (19) will generate intermodulation terms, and we will focus on its fundamental component ($n = 1$) since it has the largest magnitude. By replacing this fundamental component into (18), we have

$$\begin{aligned} \Delta t_{\mathrm{DTC}} &= T_{\mathrm{CKV}} \cdot \frac{1}{\pi} \sin(\omega_{\mathrm{frac}} t) \cdot \left(1 + 0.5\beta A_{\mathrm{rip}} \sin(\omega_{\mathrm{rip}} t)\right) \\ &= \frac{T_{\mathrm{CKV}}}{\pi} \sin(\omega_{\mathrm{frac}} t) + \frac{\beta A_{\mathrm{rip}} T_{\mathrm{CKV}}}{4\pi} \\ &\quad \cdot \left(\cos[(\omega_{\mathrm{rip}} - \omega_{\mathrm{frac}})t] - \cos[(\omega_{\mathrm{rip}} + \omega_{\mathrm{frac}})t]\right) \end{aligned} \tag{20}$$

which is exactly the result shown in (6). The first term in (20) compensates for the deterministic delay variation between REF and DIV due to the fractional-N operation, while its second terms contains intermodulation, potentially generating in-band spurs at the PLL output. From (20), the phase fluctuation corresponding to the intermodulation terms is

$$\Delta\phi_{\mathrm{DTC,int}} = \frac{\beta A_{\mathrm{rip}}}{2} \cdot \left(\cos[(\omega_{\mathrm{rip}} - \omega_{\mathrm{frac}})t] - \cos[(\omega_{\mathrm{rip}} + \omega_{\mathrm{frac}})t]\right). \tag{21}$$

Hence, the output signal of the PLL could be expressed as

$$\begin{aligned} x_{\mathrm{PLL}} &= A_{\mathrm{osc}} \sin(\omega_{\mathrm{osc}} t + \Delta\phi_{\mathrm{DTC,int}}) \\ &= A_{\mathrm{osc}} \sin\left(\omega_{\mathrm{osc}} t + \frac{\beta A_{\mathrm{rip}}}{2} \right. \\ &\quad \left. \cdot \left(\cos[(\omega_{\mathrm{rip}} - \omega_{\mathrm{frac}})t] - \cos[(\omega_{\mathrm{rip}} + \omega_{\mathrm{frac}})t]\right)\right). \end{aligned} \tag{22}$$

Since $\beta A_{\mathrm{rip}}/2$ is much less than $\pi/6$, (22) could then be approximated as

$$\begin{aligned} x_{\mathrm{PLL}} &\approx A_{\mathrm{osc}} \sin(\omega_{\mathrm{osc}} t) \\ &\quad + A_{\mathrm{osc}} \cdot \frac{\beta A_{\mathrm{rip}}}{4} \cdot \left(\cos[(\omega_{\mathrm{osc}} + \omega_{\mathrm{int},-})t] + \cos[(\omega_{\mathrm{osc}} - \omega_{\mathrm{int},-})t]\right) \\ &\quad - A_{\mathrm{osc}} \cdot \frac{\beta A_{\mathrm{rip}}}{4} \cdot \left(\cos[(\omega_{\mathrm{osc}} + \omega_{\mathrm{int},+})t] + \cos[(\omega_{\mathrm{osc}} - \omega_{\mathrm{int},+})t]\right) \end{aligned} \tag{23}$$

in which $\omega_{\mathrm{int},-} = \omega_{\mathrm{rip}} - \omega_{\mathrm{frac}}$ and $\omega_{\mathrm{int},+} = \omega_{\mathrm{rip}} + \omega_{\mathrm{frac}}$. From (23), it can be concluded that the intermodulation terms in (20) would generate spurs at $f_{\mathrm{rip}} \pm f_{\mathrm{frac}}$ at the PLL output, and when they fall in-band, the spur level should be $20\log_{10}(\beta \cdot A_{\mathrm{rip}}/4)$.

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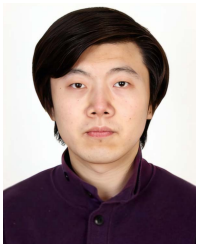

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