DPU: DAG Processing Unit for Irregular Graphs with Precision-Scalable Posit Arithmetic in 28nm

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Abstract—Computation in several real-world applications like probabilistic machine learning, sparse linear algebra, and robotic navigation, can be modeled as irregular directed acyclic graphs (DAGs). The irregular data dependencies in DAGs pose challenges to parallel execution on general-purpose CPUs and GPUs, resulting in severe under-utilization of the hardware. This paper proposes DPU, a specialized processor designed for the efficient execution of irregular DAGs. The DPU is equipped with parallel compute units that execute different subgraphs of a DAG independently. The compute units can synchronize within a cycle using a hardware-supported synchronization primitive, and communicate via an efficient interconnect to a global banked scratchpad. Furthermore, a precision-scalable positTM arithmetic unit is developed to enable application-dependent precision. The DPU is taped-out in 28nm CMOS, achieving a speedup of 5.1× and 20.6× over state-of-the-art CPU and GPU implementations on DAGs of sparse linear algebra and probabilistic machine learning workloads. This performance is achieved while operating at a power budget of 0.23W, as opposed to 55W and 98W of the CPU and GPU, resulting in a peak efficiency of 538 GOPS/W with DPU, which is $1350 \times$ and $9000 \times$ higher than the CPU and GPU, respectively. Thus, with specialized architecture, DPU enables low-power execution of irregular DAG workloads.

Index Terms—Graphs, irregular compute graphs, parallel processor, synchronization, precision, posit

I. INTRODUCTION

DIRECTED acyclic graph (DAG) is a directed graph with nodes and edges without cycles. DAGs are often used to model computation in programs, in which a node represents some compute operations, and the edges represent the dataflow and the dependencies among these operations. For example, the computation of a fully-connected neural network can be represented as a DAG with nodes corresponding to neural operations, and edges corresponding to the connectivity among them, directed according to the dataflow.

While the aforementioned neural network would result in a very regular DAG, several applications are characterized by

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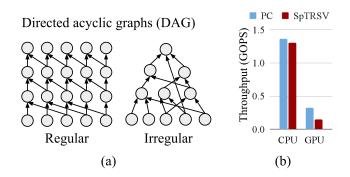


Fig. 1. (a) Regular (eg. dense linear algebra) vs irregular (eg. sparse linear algebra) DAGs. (b) Low GPU performance for irregular DAGs.

highly *irregular* DAGs, in which the edges point to seeminglyrandom nodes without repetitive patterns. For example, in a sparse neural network, around 60-70% of the edges can be dropped [1], leading to some irregularity in the DAG structure (fig. 1(a)). Different applications exhibit different degrees of irregularity. In this work, we focus on highly-irregular DAGs resulting from more than 99% sparsity in applications like sparse linear algebra, probabilistic machine learning, robotic localization, drone navigation, etc. [2], [3], [4], [5].

DAG irregularity poses several challenges for efficient hardware execution. For example, fig. 1(b) shows CPU and GPU irregular DAG throughput corresponding to two applications: (1) probabilistic circuits (PC, also called sum-product networks) used in machine learning [6], [7], and (2) sparse matrix triangular solve (SpTRSV), a widely-used linear algebra operation [8]. The GPU severely underperforms compared to the CPU despite having highly parallel hardware. Such a low performance is due to the irregularity. The seemingly-random edges are unsuitable for the commonly used single-instructionmultiple-data (SIMD) units and systolic arrays. Irregular edges also result in irregular memory accesses, leading to underutilization of caches and memory bandwidth. These irregular accesses also prevent memory coalescing, which is crucial for high GPU performance. Moreover, parallelizing different parts of DAGs across multiple units (like CPU cores, GPU streaming multiprocessors, etc.) demands high communication and synchronization overhead.

To overcome the aforementioned challenges, this paper proposes **DPU**, a specialized DAG Processing Unit designed to efficiently execute highly-irregular computational graphs and provide an optimized solution for these emerging workloads. The DPU is taped out in TSMC 28nm technology, and benchmarked on probabilistic machine learning and sparse linear algebra DAG workloads. Some of the key features are:

- Parallel asynchronous compute units equipped with software-managed local scratchpads for data reuse, connected to a global banked scratchpad via a low-overhead *asymmetric* crossbar for high memory bandwidth.
- Hardware support for fast synchronization across compute units, as frequently required for irregular DAGs.
- Execution based on decoupled data handling and compute streams to overlap memory and arithmetic instructions.
- Precision-scalable arithmetic units based on a customized positTM representation to enable application-dependent precision selection.

The paper is organized as follows. The basics of irregular DAG execution and the related challenges are discussed in §II. Section §III describes the DPU architecture and §IV explains the internal of a compute unit of the DPU, followed with §V that discusses the precision-scalable positTM unit. Subsequently, §VI presents the experimental results and measurements of the taped-out processor. Finally, §VII and §VIII discusses the related work and concludes the paper.

II. BACKGROUND AND CHALLENGES

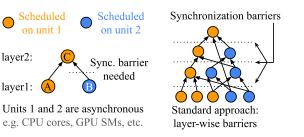
A. Background of DAG execution

In this paper, a DAG represents a graph of nodes and edges encoding the computation to be performed for an application. Depending on the application, the DAG nodes may represent one or a few arithmetic operations (e.g. addition, multiplications) on the node's inputs. The output result of a node serves as an input to the nodes connected to the outgoing edges of that node. Executing a computational DAG means evaluating the operations in all the nodes in a *valid* order.

1) **Execution order**: The directed edges of a DAG represent data dependencies, which impose an ordering of execution of the nodes. For all the edges, the source node of an edge should be executed before the destination node. Put differently, a node can be executed only after all the *predecessor* nodes connected to the incoming edges have finished execution.

2) What can be executed in parallel?: At a given moment, all the nodes whose predecessor nodes have finished execution can be scheduled. These are called the *active* nodes. The execution begins with the source nodes of the DAG being *active*, as they do not have any incoming edges. Subsequently, different nodes become active as the execution progresses. Note that the active nodes can be executed in parallel, as there are no dependencies among active nodes by definition (otherwise they would not have been active together).

As such, DAG execution happens in multiple layers. A set of nodes becomes active in each layer. The total number of layers is the same as the length of the longest path of nodes (critical path). Parallelism in a DAG can be quantified as the total number of nodes divided by the critical path length. This metric quantifies a bound on the possible speedup over a sequential execution. Eg., a DAG with a parallelism of 100 cannot be executed faster than $100 \times$ even with infinite parallel units.



(b)

Fig. 2. **Synchronizations.** (a) Need for a synchronization in a simple DAG. (b) Commonly-used *layer-wise* synchronization placement

(a)

3) Synchronizations: If the active nodes in a layer are mapped across multiple asynchronous compute units, then synchronization barriers might be needed to maintain the required ordering before beginning a new layer of active nodes. Examples of such asynchronous units are CPU cores and GPU streaming multiprocessors (also DPU's compute units, as explained later in the paper). Consider a DAG with 3 nodes as shown in fig. 2(a). Suppose nodes A and B of the first layer are scheduled on different units. To schedule node C from the next layer on unit 1, it must be ensured that node B has finished execution on unit 2 and its results are visible to unit 1. But, by definition, asynchronous units do not provide such guarantees. Hence, an explicit synchronization barrier is needed before scheduling node C.

4) Placement of nodes and synchronizations: For applications such as probabilistic machine learning and sparse linear algebra, the DAG structure is fully known at compile time, allowing strategic mapping of nodes to the compute units and the placement of the synchronizations by a compiler. The aim is to reduce the total number of synchronizations and the associated overhead. Fig. 2(b) shows the standard approach of *layer-wise* synchronizations (also called level scheduling), first introduced in [9], where a synchronization is used after every layer of active nodes. The active nodes in a layer are mapped across available parallel compute units that then have to be synchronized before executing the next layer.

DPU uses an advanced graph-partitioning technique to reduce the number of synchronization barriers, as explained in [10]. The DAGs are partitioned into *superlayers* (fig. 3), each containing 64 subgraphs (possibly spanning multiple DAG layers) for 64 compute units in DPU. A synchronization barrier is used after every superlayer. The subgraphs are made as large as possible to reduce the number of synchronizations, but also optimized to have similar sizes to balance the workload. This is achieved by translating the DAG partitioning task into a constrained-optimization problem and using the Google OR-Tools solver [11]. As such, given a DAG, the mapping of nodes to the compute units and the placement of synchronizations are fixed at compile time.

B. Challenges due to irregularity

The irregularity in DAG structure poses several challenges for efficient execution on general-purpose processors like

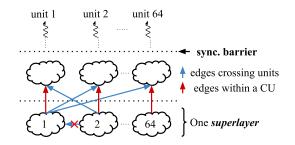


Fig. 3. Our approach of superlayer-based synchronization placement

TABLE I CHALLENGES AND OPPORTUNITIES IN IRREGULAR DAG EXECUTION AND RELATED DPU INNOVATIONS

Challenges/opportunities for irregular DAGs	DPU innovations		
SIMD unfriendly	Asynchronous compute units with independent instructions		
Frequent synchronizations	Hardware-supported synchronization with special instructions, and <i>superlayer</i> -based parallel execution		
Inefficient use of caches	Software-managed scratchpads		
Data prefetching	Decoupled-instruction streams for efficient hardware prefetching		
Diverse applications with varying precision requirement	Precision-scalable custom posit TM arithmetic		

CPUs and GPUs. These are summarized in table I along with the related DPU's innovations to address them.

1) SIMD unfriendly: The active nodes to be executed in parallel may perform the same arithmetic operation on the inputs, which would make them suitable for a SIMD execution. However, the inputs of these nodes typically reside in random memory locations owing to the irregularity of the DAG structure, making them unlikely to be co-located in a CPU or GPU cache-line. In fact, some of them may not be cached at all and need to be fetched from external memory. Experiments in [12] find that around 50% of the load requests in graph workloads result in cache misses. This leads to high variability in the load latency of these inputs, causing all the SIMD lanes to stall for the slowest input. Thus, despite the availability of parallel operations to execute, random memory loads make irregular DAGs SIMD-unfriendly.

Consequently, the x86 CPU SIMD vector instructions are not useful for irregular DAGs, and parallelizing threads across multiple CPU cores are preferred from a performance point of view. GPUs, on the other hand, can tolerate irregular memory latency by switching thread warps when a thread stalls (given there are enough thread warps available to schedule). However, GPUs suffer from other bottlenecks as discussed subsequently. The DPU uses asynchronous compute units that execute independent instruction streams instead of a SIMD unit.

2) *Frequent synchronizations:* The total amount of computation done per synchronization barrier is a key indicator of parallel performance — the higher the better, to amortize the synchronization cost. This amount depends on the DAG structure and the barrier-placement techniques (refer §II-A4). In our benchmarks, the *layer-wise* approach results in 210 compute operations per barrier, which increases to 633 with the superlayer-based approach for 64 parallel units. Yet, if the barrier takes comparable cycles as the computations, it can severely degrade the parallel performance, possibly making it even worse than a sequential execution.

The synchronization barriers in multi-core CPUs are implemented with atomic operations on a shared memory location. These atomic operations typically incur long latency from the CPU core to the outer-most shared caches or external memory. Furthermore, these operations also create a burst of cachecoherency traffic as every core modifies the same location, increasing the barrier cost further. Due to these reasons, the synchronization barriers in CPUs typically take 3000 cycles (measured with the EPCC microbenchmark [13]). Similarly, in the GPUs, the global synchronization for all the CUDA cores consumes around 2000 cycles [14]. To avoid this bottleneck, DPU is equipped with a hardware-supported barrier instruction that synchronizes all the units in a single cycle.

3) Inefficient use of caches: DAG execution results in randomly addressed single-word memory accesses (typically of 4B) with lower spatial locality, which implies that the 32/64 words cacheline granularity of CPU and GPU is too high, and most of the fetched words are unlikely to be used. Such random accesses also prevent the memory-request coalescing, which is critical for good GPU performance. Smaller cachelines are preferable for these workloads, but lead to higher area/energy overhead of tag storage and lookup. Furthermore, depending on the access patterns, some words are reused much more frequently than the others. Thus, selectively choosing which words to store locally results in an efficient use of the scarce on-chip local storage. Due to these reasons, DPU uses software-managed local scratchpads with single-word accesses, instead of hardware-managed caches.

4) Data prefetching: An out-of-order CPU core tries to find the data-prefetching opportunities at runtime, and can issue multiple out-standing load requests [15], [16]. However, [17] reports that an Intel CPU could only keep 2-3 load requests in flight while executing graph workloads, even when the architecture supported up to 10 load requests. The main reason for this underperformance is the limited instruction window in which the core looks for independent load requests, and widening this window is area and power-hungry. To prefetch data efficiently, DPU exploits the fact that the DAG structure is known at compile time. The compiler decouples the DPU's instructions into memory and processing *streams*, which are executed independently on different subunits. This enables low-overhead prefetching and memory-compute overlap, without using costly out-of-order hardware.

III. DPU ARCHITECTURE

A. Compute units (CU)

Fig. 4 shows the DPU architecture with 64 parallel **compute units** (CU) that execute 64 subgraphs in the superlayers shown in fig. 3. Each CU is equipped with its own instruction memory and executes these instructions *asynchronously*; a stalled CU does not stall the others. The CUs communicate via a global

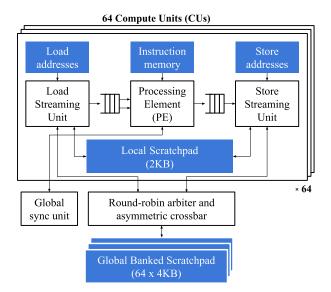


Fig. 4. The DPU architecture with 64 parallel CUs

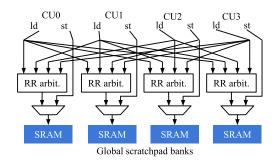


Fig. 5. Asymmetric crossbar to reduce area and power overhead

scratchpad connected by an asymmetric crossbar (§III-B). The single-cycle synchronization of CUs is made possible with a *global barrier* instruction and a global sync unit (§III-C). The detailed architecture of CU is explained later in §IV. A specialized compiler [10] is designed that takes an arbitrary DAG and generates the superlayers, schedules operations, performs memory allocation, etc. for DPU execution.

B. Global scratchpad and asymmetric crossbar

As observed in [12], irregular graphs typically lead to relatively high global traffic when executed on parallel units. In our benchmarks, we also observe a similar trend. The blue global edges in superlayers in fig. 3 accounts for 33% of the total edges in our benchmarks. In DPU, this global inter-CU communication happens via a high-bandwidth global scratch-pad. The 256KB scratchpad is constructed with 64 banks of 4KB each, providing an overall bandwidth of 2Kb/cycle.

Furthermore, for low hardware overhead, the CUs connect to the global scratchpad via an *asymmetric* crossbar (fig. 5), such that a CU can load data from any bank but can store to only one specific bank each. This asymmetry of global loads but restricted stores (instead of the other way around) is a deliberate design choice considering the fact that an output of a node is stored only once but usually loaded multiple times from different CUs.

The asymmetric design does reduce the flexibility of mapping intermediate node outputs to the global scratchpad banks. In fact, the bank mapping is fully determined based on the mapping of operations to the CUs (which happens during the superlayer generation), because the output of an operation on a CU can only be stored to that CU's respective bank. On the other hand, with a full crossbar, the compiler could possibly map an output to any bank to reduce bank conflicts. However, predicting and averting these bank conflicts during compilation is anyway not possible given that the CUs are asynchronous and can possibly stall for unpredictable cycles (for example, waiting for the next instruction). As a result, in practice, it is very difficult for a compiler to exploit the additional flexibility coming from a full crossbar, and hence the inflexibility of an asymmetric crossbar does not drastically impact the throughput.

For each bank, the load requests are selected based on a round-robin arbitration scheme, while the store request has the highest priority. The store request cannot participate in the round-robin arbitration with 64 load requests because that would reduce the store bandwidth by $64 \times$ compared to the loads. Overall, this asymmetric crossbar consumes 45% lower area and energy than the symmetric counterpart that allows store requests to reach every bank.

C. Global sync unit

To mitigate the overhead of frequent synchronizations, the CUs are equipped with a special instruction for global barrier, complemented with a central dedicated global sync hardware unit. When a CU reaches a global barrier instruction, it indicates this to the global sync unit and stalls until the other CUs hit their global barrier instruction. The global sync unit uses a tree of AND gates to determine if all the CUs have reached the barrier, and communicates this to all the CUs within that cycle, enabling a single-cycle synchronization. Even though the paths to/from the global sync units create a long combinational loop due to the unit's centralized role, they are not the critical paths in our design.

IV. COMPUTE UNIT (CU) ARCHITECTURE

A. Local scratchpad

Because the subgraphs in the superlayers are made as large as possible, they have a significant proportion of intra-CU edges shown in red in fig. 3 (67% of the total number of edges in our benchmarks). To exploit this locality, the CUs are equipped with an address-mapped local scratchpad. The compiler maps the output data of a node to the local scratchpad if all outgoing edges of the node are intra-CU (colored red in fig. 3), otherwise it is mapped to the global scratchpad. A scratchpad is used instead of a cache due to the following reasons:

- A software-managed scratchpad can selectively store only the data that has local reuse.
- The typical cacheline granularity of 32 or 64 words is too large for graphs due to frequent irregular memory fetches, and results in wasted interconnect traffic [12], [17].

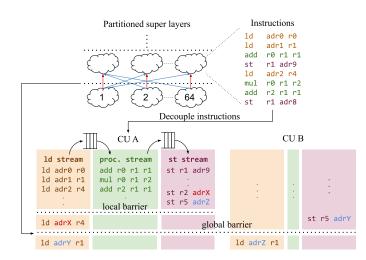


Fig. 6. Decoupled streams to overlap memory and processing instructions

• An address-mapped scratchpad avoids tag storage and lookup, reducing the area and energy footprint.

B. Data prefetching using decoupled instruction streams

For a given DAG, the memory load and store instructions to/from the scratchpads can be predicted at compile time. This is leveraged to perform aggressive data prefetching by overlapping memory requests with arithmetic operations without the need for expensive out-of-order hardware. As shown in fig. 6, the instructions for CUs are decoupled into three *streams*: load, processing and store streams, which are executed independently on different components of the CU.

Load streaming unit: The load addresses (for both global and local scratchpads) along with the corresponding destination registers are programmed in the load address memory. The load streaming unit prefetches the data by issuing these load requests to the local or global scratchpads. The loaded data may not yet be allowed to be written to the register file in the PE, because the PE might still be using the destination register for some other computation. Instead, the data is pushed on a FIFO going to the PE, from where the PE will eventually consume it at the right moment. The load streaming unit keeps streaming the load requests as long as there is space in the FIFO. The prefetching cannot cross barriers, hence the length of the stream is controlled by a special load stream length register, which is programmed by the PE after every barrier. The FIFO becomes empty at the barriers, hence frequent barriers reduce prefetching efficiency.

PE: The processing streams contain the actual arithmetic instructions to be executed on the PE (fig. 7). A custom instruction set is designed (table II), which dictates the computation of the arithmetic unit in the PE. The PE does not contain pipeline stages, and all the instructions have a latency of 1 cycle. The instructions have an 18b compute field, with a 3b opcode for ALU and special-function instructions (table II) and $3 \times 5b$ operand register file addresses. A 32-entry 32b register file is used with 3 write ports (2 for load ports and 1 for the arithmetic unit) and 2 read ports (for the arithmetic unit). The compiler makes sure that the 3 write ports write to

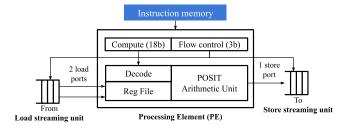


Fig. 7. Internal PE design and FIFO flow-control for precise ld/st timing

TABLE II Instructions of PE

add, mul	Add or multiply two numbers
max, min	Max or min of two numbers
global or	Barriers for synchronization
local barrier	Darriers for synchronization
set_ld_stream_len	Sets the load stream length until next barrier
set_precision	Sets the precision of the arithmetic unit

different registers in the same cycle, to avoid conflicts. This is done by precisely controlling the timing of the loads, using flow control bits (see further). The output of the arithmetic unit connects to one of the register write ports and the FIFO to the store streaming unit.

The 3 remaining instruction bits control the PE's IO dataflow. The PE cannot directly communicate with scratchpads; it only gets/puts data from/to the FIFOs of load/store units. The FIFO flow control bits are encoded in the processing instructions, to let the PE precisely control the timing of migrating data from the load FIFO to the register file, resp. from the ALU output to the store FIFO. These flow control bits indicate whether a FIFO load/store is needed in parallel with the compute operation of the current instruction. The PE stalls if a load flow control bit is set, but there is no data in the load FIFO, or if the store bit is set but the store FIFO is full. With such a flow control, PE avoids data hazards like the writeafter-read (WAR) hazard in which the data from load FIFOs overwrite an active register that is not yet fully consumed.

Store streaming unit: The store streaming unit waits for data to show up on the store FIFO from the PE, and stores them to local/global scratchpads according to the addresses in the store stream. It also informs the PE whether all the data is stored to the memory and there are no outstanding store requests left, which helps the PE to decide if the compute unit is ready to sync with other units at the barriers.

Local barrier. The load-to-PE and the PE-to-store communication happens via FIFOs, and the corresponding datadependencies are resolved by the FIFOs' flow control. There

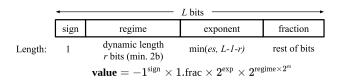


Fig. 8. The positTM representation

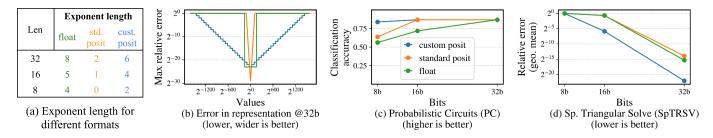


Fig. 9. Accuracy impact of different representations. Custom posit performs better due to lower error for wider range of values.

is also a dependency of load stream on the store stream. A load following a store to the same scratchpad address (adrX in fig. 6) should not be executed before the store finishes. Since the streaming units operate independently, this ordering is not guaranteed. To address this, an intra-CU *local barrier* is used. The *load stream length* is programmed such that the load streaming unit waits at the local barrier for the store unit to catch-up before proceeding.

Stream generation: Given a subgraph to be executed on a CU, the DPU compiler first generates the corresponding instructions, by (1) scheduling the operations of subgraph nodes in a topological order using a depth-first traversal, (2) performing register allocation using the linear-scan method [18], and (3) inserting the load-store instructions as needed depending on the register file size. Next, local barriers are inserted such that every load following a store to the same address has at least one barrier in between. Finally, from these instructions, the decoupled streams are generated by assigning the instructions to their respective type of stream, while preserving the order.

Performance impact. Due to the data prefetching enabled by the decoupled streams, the DPU achieves $1.8 \times$ speedup over an in-order version of DPU that uses the coupled instructions (over the benchmarks described in §VI).

V. PRECISION-SCALABLE POSITTM UNIT

Application dependent precision-scalability. DAGs from different applications can have widely varying precision requirements. For example, the probabilistic circuit (also called sum-product network) [6], [7], one of our irregular workloads, is used in machine learning for inference and reasoning under uncertainty. It can be used for safety-critical applications like autonomous navigation [4] demanding highly accurate computation, but can also be deployed for simpler applications like human activity classification (running, sitting, etc.) [19], [20], which can tolerate some mispredictions. To meet such diverse requirements, PEs are equipped with precision-scalable arithmetic units that can perform $1 \times 32b$, $2 \times 16b$ or $4 \times 8b$ operations in a single cycle, enabling batch execution based on the application requirements.

PositTM representation. The DPU uses the positTM [21] instead of the floating-point representation to enable lowerprecision operations wherever possible. The posit representation (fig. 8) allows trading accuracy for range at runtime. To do this, it uses a new *regime* field, whose length dynamically varies depending on the magnitude of the number, allowing

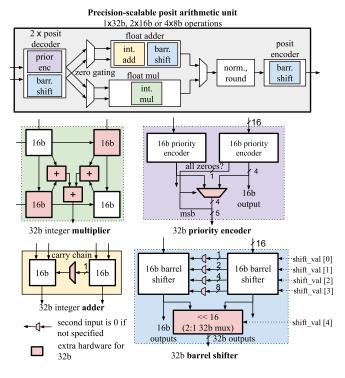


Fig. 10. Posit arithmetic unit with precision-scalable subunits

to simply reduce the length of the other fields instead of under/overflowing. The posit representation is specified as a tuple $\langle L, es \rangle$ where L is the total length and es is the maximum length of the exponent field.

Custom posit. The standard posit representation proposed by Gustafson [21] aims to have higher precision than floats around the value of 1.0, while sacrificing precision for small and large numbers (fig. 9(b)). While this design choice might be suitable for some applications, our target applications are characterized by a very large dynamic range and sensitivity to approximations across this range, requiring us to take a different approach. In DPU, higher *es* is used (fig. 9(a)) such that the custom posit has a similar precision to float around 1.0, but a more gradual precision degradation for small/large values, greatly increasing the representable range of values. Fig. 9(b) demonstrates this gradual, tapered degradation of precision.

Application accuracy with custom posit. To quantify the impact of lower-precision computation on an application's accuracy, the arithmetic operations $(+ \text{ and } \times)$ in posit and float

TABLE III Posit unit area and power breakdown

	Area	Power		
	$ imes 10^3~\mu{ m m2}$	%	μW	%
Decoders	1.2	17	166	19
Float add and mul	4.3	57	484	56
Normalize and round	1.4	18	142	17
Encoder	0.6	8	64	8
Precision-scalable posit unit	7.5		856	

 TABLE IV

 PERFORMANCE COMPARISON WITH AN STATE-OF-THE-ART POSIT UNIT

	This work			PACoGen [24]	
Operating mode	32b	16b	8b	32b	
Area ($\times 10^3 \ \mu m2$)		7.5		5.7	
Energy (pJ/op)	3.05	1.33	0.57	2.08	
Throughput (ops/cycle)	1	2	4	1	

representations are prototyped with software models in Python. Fig. 9(c) and (d) shows the impact of lower precision float, standard posit, and custom posit on different applications. Fig. 9(c) shows classification accuracy on machine learning tasks from UCI repository [22] with probabilistic circuit DAGs, while fig. 9(d) shows the relative error during iterative solutions of sparse matrix triangular systems on SuiteSparse matrices [23]. These benchmarks are described in detail in §VI. The results demonstrate that the custom posit outperforms the standard posit and float counterparts of the same lengths.

Hardware design. A posit operator at its core needs a float operator, since, for a given value of regime, posit behaves like a float. Hence, a posit operation is strictly costlier than a float operation (ignoring the exceptions of IEEE float). The arithmetic unit contains posit-format decoders and encoders, shared among float adder and multiplier (fig. 10). The decoder finds the length of the regime field (with a priority encoder) and aligns the rest of the fields accordingly (with a barrel shifter) for addition and multiplication. The encoder aligns the output (with a barrel shifter) according to the output regime.

All the blocks in the arithmetic units support precision scalability to perform $1 \times 32b$, $2 \times 16b$ or $4 \times 8b$ operations. This runtime scalability is novel, and not available in other posit hardware generators [25], [24], [26]. Fig. 10 shows how 32b building blocks are constructed from two 16b blocks, which in turn are made of 8b blocks. The posit unit consumes $1.8 \times$ the area and power of a float counterpart (Table III), but enables 8b or 16b operations as discussed earlier. Table IV reports comparison with PACoGen [24], a state-of-the-art posit unit generator, which consumes $0.76 \times$ and $0.68 \times$ area and energy at 32b, respectively, due to the overhead of precision-scalability in our unit. On the other hand, for applications requiring only 8b precision, the 32b PACoGen unit consumes $3.7 \times$ the energy per operation of the precision-scalable unit.

VI. EXPERIMENTS

DPU is taped-out in TSMC 28nm technology with an active area of 2.0×1.9 mm² (fig. 11). Table V shows the postlayout area and power breakdown of the chip (estimated after

← 2.0mm →			
16 CU 16 CU Global scratch. 16 CU 16 CU 16 CU 16 CU	- loca - load	e addr 1 scrat 1 addr ructior	chpad
Technology	TS	SMC 281	nm
Active area	2.0 x 1.9 mm2		
Supply Voltage	0.6-0.9V		
Arithmetic representation	8/16/32b custom POSIT		
On-chip SRAM	864 kB		
	8b	16b	32b
Fmax (MHz)	288	281	278
Power (mW) @Fmax	228	227	228
Peak throughput (GOPS) @0.9V	73.8	35.9	17.8
Peak energy eff. (GOPS/W) @0.6V	538	267	126

Fig. 11. Chip micrograph and specifications

TABLE V Post-layout area and power breakdown

	Area		Power	
	mm^2	%	mW	%
64 Compute Units:				
PEs:				
Posit units	0.48	13	54.8	24
Rest of PE	0.50	13	37.4	16
Local scratchpads	0.27	7	13.6	6
Instr. mem, ld/st addr. mem	1.18	31	50.2	22
Rest of CU	0.24	6	22.6	10
Global scratchpads	0.54	14	21.0	9
Crossbar	0.19	5	29.3	13
Rest	0.40	11		
DPU	3.8 228.9			

Peak throughput @Fmax: 73.8 GOPS Peak efficiency : 538 GOPS/W

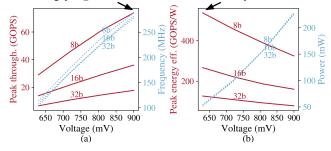


Fig. 12. Peak-performance scaling with voltage and precision

activity annotation). The memories occupy half of the area and consume 37% of the power. The asymmetric crossbar consumes 13% power, which would have been two times costlier if a conventional symmetric crossbar had been used.

A. Peak performance and voltage scaling

The chip's electrical performance is measured by scaling the voltage from the nominal 0.9V to 0.6V. The chip can operate at the maximum frequency of 288MHz at 0.9V and 8b precision, with a peak throughput of 73.8 GOPS (fig. 12(a)),

Application	Workload	Nodes (n)	Longest path length (l)	Parallelism (n/l)
	mnist	10414	26	400
	nltcs	13627	27	504
	msnbc	47334	28	1690
Probabilistic	bnetflix	55007	53	1037
	ad	66819	93	718
Circuits (PC)	bbc	77457	92	841
	c20ng	80962	81	999
	kdd	98211	54	1818
	baudio	121263	70	1732
	pumsbstar	149662	82	1825
	tols4000	5978	52	114
	bp_200	8406	139	60
	west2021	10159	136	74
	qh1484	11298	237	47
Sparse Matrix	sieber	22768	242	94
Triangular Solves	gemat12	74199	778	95
(SpTRSV)	dw2048	79240	929	85
	orani678	114275	634	180
	pde2961	140303	1357	103
	blckhole	150876	1264	119

and at the peak energy-efficiency of 538 GOPS/W at 0.6V (fig. 12(b)). The top 50 critical paths are in the posit arithmetic unit and the crossbar. Both the blocks can be pipelined to increase clock frequency further, but would have a negative impact on instruction scheduling due to higher posit unit latency, and would induce a potential throughput tradeoff due to increased access latency of the global scratchpad.

B. Workloads

The performance of the chip is benchmarked with compute DAGs from two different types of workloads listed in table VI. The DPU compiler takes as input a DAG in any of the popular graph formats (i.e. all formats supported by the NetworkX package [27]) and generates an execution binary that can be directly programmed to DPU. The experiments are performed with the DAGs that fit in the on-chip data memory (global and local scratchpads). The programming of memories, with an FPGA via a slow chip I/O interface, is not included in the throughput results.

Probabilistic circuits (PC). Probabilistic circuits (also called sum-product networks) are used in machine learning for reasoning, robust inference under uncertainty, and safety-critical tasks [3], [4], [19], [28]. Note that the term *circuit* is not used in the sense of VLSI circuits. A PC is an irregular DAG in which the nodes are either sum or product operations. The experiments are performed on a standard benchmark of density-estimation applications from [29].

Sparse matrix triangular solves (SpTRSV). Solving a matrix triangular system is a fundamental operation in linear algebra, used in various applications like robotics, optimization, autonomous navigation, etc. Real-world matrices usually turn out to be highly sparse and the resulting compute DAG highly irregular. Benchmarking is done on matrices of varying sizes from the SuiteSparse benchmark of real applications [23].

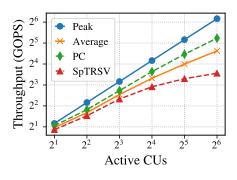


Fig. 13. Scaling of throughput with increasing active CUs at 8b precision

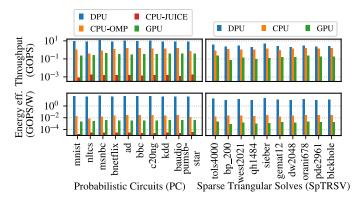


Fig. 14. Performance comparison. The DPU operating point is 0.9V and 32b.

C. Throughput scaling with different active CUs

The throughput of DPU is measured by keeping a different number of CUs active to evaluate the parallelization effectiveness for increasing parallel CUs (fig. 13). The PC throughput scales better than the SpTRSV because of higher DAG parallelism (table VI). Apart from DAG parallelism, other factors that lower average throughput compared to the peak are: (1) the impact of barriers on data-prefetching, and (2) global scratchpad access conflicts. Overall, the average throughput is $2.8 \times$ lower than the peak for 64 CUs.

D. Comparison with CPU and GPU

Since there is no previous silicon-proven chip targeting highly irregular DAGs, this experiment is designed to compare DPU's performance with state-of-the-art CPU and GPU implementations. The details of the platforms are as follows. **DPU:** The results are for 64 active CUs operating at 278MHz and 32b precision. **CPU:** An Intel(R) Xeon Gold 6154 CPU operating at 3GHz is used for comparison. For PC, a standard Julia-based library called Juice [30] (**CPU-JUICE**) and an highly-optimized OpenMP-based implementation [10] (**CPU-OMP**) are used for comparison. The SpTRSV performance is evaluated with the standard Intel Math Kernel Library (MKL v2021.1). The programs are compiled with GCC v4.8.5 compiler, -Ofast flag, and OpenMP v3.1.

GPU: The GPU baseline is evaluated with an RTX 2080Ti GPU operating at 1.3GHz, and the code compiled with the CUDA v10.2.89 compiler. For PC, an efficient CUDA code described in [31] is used for benchmarking. For SpTRSV, the

TABLE VI STATISTICS OF THE BENCHMARKED DAGS

 TABLE VII

 PERFORMANCE COMPARISON WITH OTHER PLATFORMS.

	DPU*	CPU	GPU		
Technology	28nm	22nm	12nm		
Frequency (GHz)	0.28	3	1.35		
Arithmetic representation	custom posit	float	float		
Peak throughput (GOPS)	17.8	3.4×10^{3}	13.5×10^{3}		
Avg. throughput (GOPS)	6.2	1.2	0.3		
Power (W)	0.23	55	98		
Avg. energy efficiency (GOPS/W)	27	0.02	0.003		
Workloads	PC and SpTRSV DAGs				

*DPU operating point is 0.9V and 32b precision

cusparseScsrsv_solve() function from the standard cuSPARSE library [32], [33] is used. For a fair comparison, the memory copy time from the host to GPU is not considered.

Fig. 14 and table VII summarizes the comparison results. All the platforms show higher performance for PC than Sp-TRSV due to the higher parallelism (table VI). Juice performs considerably slower than the OpenMP counterpart, despite using the same number of CPU cores. Overall, the DPU outperforms the CPU, which in turn beats the GPU. The DPU achieves an average throughput of 6.2 GOPS, a speedup of $5.1 \times$ and $20.6 \times$ compared to the CPU and GPU, at an average efficiency of 27 GOPS/W at 32b precision, showing the effectiveness of the specialized DPU architecture for irregular DAGs.

E. DPU's performance for a regular DAG

DPU's performance for *regular* DAGs would be an interesting result, quantifying the effectiveness of asynchronous CUs for a regular workload. Hence, as an additional experiment, performance is benchmarked for a regular DAG of dense matrix-vector multiplication (GEMV). For a 128x128 matrix, DPU achieves a throughput of 17.5 GOPS at a utilization of 97.5%, while consuming 414mW at 0.9V, 0.28GHz and 32b precision, resulting in an efficiency of 42 GOPS/W. This shows that DPU can achieve near-peak throughput for a regular DAG, although with an inefficiency that separate instructions and load/store addresses are used for every CU due to the absence of SIMD support. For reference, the CPU achieves 7.4 GOPS and 0.14 GOPS/W with the Intel MKL GEMV function cblas_sgemv().

VII. RELATED WORK

Neural-network processors exploiting sparsity like [1], [34], [35], [36], [37] have special hardware support to handle irregularity resulting from the sparsity. However, sparsity in our DAG workloads is typically more than 99%, significantly higher than NN sparsity (less than 70-80%). As a result, sparse NNs exhibit higher compute-to-memory fetch ratios and some repetitive structures that can be exploited, e.g., by using a systolic array of PEs, while the DPU needs different architectural techniques due to the ultra-high sparsity.

In recent years, architectures like [38], [39], [40], [41], [42] have been proposed for general graph-analytic workloads like PageRank, breadth-first search, single-source shortest paths,

etc. The key difference is that these architectures work well when a significant portion of the graph nodes are *active*, while -in compute DAGs only the nodes in a DAG layer are active -at a time due to the dependency-induced node ordering. In general graph analytics, the active nodes cannot be predicted at compile time, while they can be predicted for our target DAGs, which is heavily utilized in this work for reducing the number of barriers, aggressive data prefetching, etc.

The sparse processing unit (SPU) [43] uses hardware support for *stream-joins* which is similar to our decoupled streams (§IV-B). However, DPU uses a register-bank based PE for local data reuse, while SPU uses a coarse-grained reconfigurable dataflow array (CGRA). Such a dataflow array can be fully utilized when there are frequently recurring patterns in the DAG for which the array can be reconfigured, but irregular DAGs typically lack a single repetitive pattern. Further, the SPU consumes 16W (simulated) as opposed to DPU's 0.23W.

Overall, DPU is novel in targeting DAG applications with high sparsity-induced irregularity, with specialized features like hardware-supported synchronization, decoupled streamsbased execution, and application-dependent posit arithmetic.

VIII. CONCLUSION

This paper proposed DPU, a processor designed for energyefficient parallel execution of irregular DAGs. The DPU is equipped with 64 parallel compute units (CU), each executing a DAG subgraph independently. The CUs communicate via a high-bandwidth global scratchpad connected using a lowoverhead asymmetric crossbar. Synchronization of CUs, frequently needed for DAGs, happens in a single cycle using a specialized hardware unit. The instructions of CUs are decoupled into multiple streams for overlapping execution, resulting in $1.8 \times$ speedup. For the arithmetic operations, the CUs are equipped with precision-scalable custom posit units that can perform low-precision batch inference depending on the application requirement. The DPU is fabricated in 28nm technology, and benchmarked on irregular DAGs from probabilistic machine learning and sparse linear algebra. Measurement results show a mean speedup of $5.1 \times$ and $20.6 \times$ over state-of-the-art CPU and GPU implementations, with a peak performance of 73.8 GOPS and 538 GOPS/W. Thus, DPU takes a step towards supporting emerging irregular DAG workloads in energy-constrained platforms.

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REFERENCES

- [1] A. Parashar, M. Rhu, A. Mukkara, A. Puglielli, R. Venkatesan, B. Khailany, J. Emer, S. W. Keckler, and W. J. Dally, "Scnn: An accelerator for compressed-sparse convolutional neural networks," ACM SIGARCH Computer Architecture News, vol. 45, no. 2, pp. 27–40, 2017.
- [2] F. Dellaert and M. Kaess, "Factor graphs for robot perception," Foundations and Trends® in Robotics, vol. 6, no. 1-2, pp. 1–139, 2017.
- [3] K. Stelzner, R. Peharz, and K. Kersting, "Faster attend-infer-repeat with tractable probabilistic models," in *Proceedings of the 36th International Conference on Machine Learning, ICML*, vol. 97, 2019, pp. 5966–5975.
- [4] K. Zheng and A. Pronobis, "From pixels to buildings: End-to-end probabilistic deep networks for large-scale semantic mapping," in 2019 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS), 2019, pp. 3511–3518.
- [5] A. Suleiman, Z. Zhang, L. Carlone, S. Karaman, and V. Sze, "Navion: a fully integrated energy-efficient visual-inertial odometry accelerator for autonomous navigation of nano drones," in 2018 IEEE Symposium on VLSI Circuits. IEEE, 2018, pp. 133–134.
- [6] Y. Choi, A. Vergari, and G. Van den Broeck, "Probabilistic circuits: A unifying framework for tractable probabilistic models," Technical report, Tech. Rep., 2020.
- [7] H. Poon and P. Domingos, "Sum-product networks: A new deep architecture," in 2011 IEEE International Conference on Computer Vision Workshops (ICCV Workshops). IEEE, 2011, pp. 689–690.
- [8] T. A. Davis, Direct methods for sparse linear systems. SIAM, 2006.
- [9] E. Anderson and Y. Saad, "Solving sparse triangular linear systems on parallel computers," *Int. J. High Speed Comput.*, vol. 1, no. 1, p. 73–95, apr 1989. [Online]. Available: https://doi.org/10.1142/ S0129053389000056
- [10] N. Shah, W. Meert, and M. Verhelst, "Graphopt: constrained optimization-based parallelization of irregular graphs," *arXiv preprint* arXiv:2105.01976, 2021.
- [11] L. Perron and V. Furnon, "Or-tools," Google. [Online]. Available: https://developers.google.com/optimization/
- [12] A. Addisie, H. Kassa, O. Matthews, and V. Bertacco, "Heterogeneous memory subsystem for natural graph analytics," in 2018 IEEE International Symposium on Workload Characterization (IISWC), 2018, pp. 134–145.
- [13] J. M. Bull, F. Reid, and N. McDonnell, "A microbenchmark suite for openmp tasks," in *International Workshop on OpenMP*. Springer, 2012, pp. 271–274.
- [14] L. Zhang, M. Wahib, H. Zhang, and S. Matsuoka, "A study of single and multi-device synchronization methods in nvidia gpus," in 2020 IEEE International Parallel and Distributed Processing Symposium (IPDPS). IEEE, 2020, pp. 483–493.
- [15] P. Hammarlund, A. J. Martinez, A. A. Bajwa, D. L. Hill, E. Hallnor, H. Jiang, M. Dixon, M. Derr, M. Hunsaker, R. Kumar *et al.*, "Haswell: The fourth-generation intel core processor," *IEEE Micro*, vol. 34, no. 2, pp. 6–20, 2014.
- [16] J. Doweck, W.-F. Kao, A. K.-y. Lu, J. Mandelblat, A. Rahatekar, L. Rappoport, E. Rotem, A. Yasin, and A. Yoaz, "Inside 6th-generation intel core: New microarchitecture code-named skylake," *IEEE Micro*, vol. 37, no. 2, pp. 52–62, 2017.
- [17] S. Beamer, K. Asanovic, and D. Patterson, "Locality exists in graph processing: Workload characterization on an ivy bridge server," in 2015 IEEE International Symposium on Workload Characterization. IEEE, 2015, pp. 56–65.
- [18] M. Poletto and V. Sarkar, "Linear scan register allocation," ACM Transactions on Programming Languages and Systems (TOPLAS), vol. 21, no. 5, pp. 895–913, 1999.
- [19] L. I. Galindez Olascoaga, W. Meert, N. Shah, M. Verhelst, and G. Van den Broeck, "Towards hardware-aware tractable learning of probabilistic models," *Advances in Neural Information Processing Systems* 32 (NeurIPS), vol. 32, 2019.
- [20] N. Shah, L. I. G. Olascoaga, W. Meert, and M. Verhelst, "Problp: A framework for iow-precision probabilistic inference," in 2019 56th ACM/IEEE Design Automation Conference (DAC), 2019, pp. 1–6.
- [21] J. L. Gustafson and I. T. Yonemoto, "Beating floating point at its own game: Posit arithmetic," *Supercomputing Frontiers and Innovations*, vol. 4, no. 2, pp. 71–86, 2017.
- [22] D. Dua and C. Graff, "UCI machine learning repository," 2017. [Online]. Available: http://archive.ics.uci.edu/ml
- [23] T. A. Davis and Y. Hu, "The university of florida sparse matrix collection," ACM Transactions on Mathematical Software (TOMS), vol. 38, no. 1, pp. 1:1–1:25, 2011.

- [24] M. K. Jaiswal and H. K.-H. So, "Pacogen: A hardware posit arithmetic core generator," *Ieee access*, vol. 7, pp. 74586–74601, 2019.
- [25] R. Chaurasiya, J. Gustafson, R. Shrestha, J. Neudorfer, S. Nambiar, K. Niyogi, F. Merchant, and R. Leupers, "Parameterized posit arithmetic hardware generator," in 2018 IEEE 36th International Conference on Computer Design (ICCD). IEEE, 2018, pp. 334–341.
- [26] S. Tiwari, N. Gala, C. Rebeiro, and V. Kamakoti, "Peri: A configurable posit enabled risc-v core," ACM Transactions on Architecture and Code Optimization (TACO), vol. 18, no. 3, pp. 1–26, 2021.
- [27] A. Hagberg, P. Swart, and D. S Chult, "Exploring network structure, dynamics, and function using networks," Los Alamos National Lab.(LANL), Los Alamos, NM (United States), Tech. Rep., 2008.
- [28] N. Thoma, Z. Yu, F. Ventola, and K. Kersting, "Recowns: Probabilistic circuits for trustworthy time series forecasting," arXiv preprint arXiv:2106.04148, 2021.
- [29] Y. Liang, J. Bekker, and G. V. den Broeck, "Learning the structure of probabilistic sentential decision diagrams," in *Proceedings of the Thirty-Third Conference on Uncertainty in Artificial Intelligence UAI*, 2017.
- [30] M. Dang, P. Khosravi, Y. Liang, A. Vergari, and G. Van den Broeck, "Juice: A julia package for logic and probabilistic circuits," in *Proceedings of the 35th AAAI Conference on Artificial Intelligence (Demo Track)*, 2021.
- [31] N. Shah, L. I. G. Olascoaga, W. Meert, and M. Verhelst, "Acceleration of probabilistic reasoning through custom processor architecture," in 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE). IEEE, 2020, pp. 322–325.
- [32] M. Naumov, L. Chien, P. Vandermersch, and U. Kapasi, "Cusparse library," in GPU Technology Conference, 2010.
- [33] M. Naumov, "Parallel solution of sparse triangular linear systems in the preconditioned iterative methods on the gpu," *NVIDIA Corp., Westford, MA, USA, Tech. Rep. NVR-2011*, vol. 1, 2011.
- [34] J.-F. Zhang, C.-E. Lee, C. Liu, Y. S. Shao, S. W. Keckler, and Z. Zhang, "Snap: An efficient sparse neural acceleration processor for unstructured sparse deep neural network inference," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 2, pp. 636–647, 2021.
- [35] Z. Yuan, Y. Liu, J. Yue, Y. Yang, J. Wang, X. Feng, J. Zhao, X. Li, and H. Yang, "Sticker: An energy-efficient multi-sparsity compatible accelerator for convolutional neural networks in 65-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 465–477, 2020.
- [36] X. He, S. Pal, A. Amarnath, S. Feng, D.-H. Park, A. Rovinski, H. Ye, Y. Chen, R. Dreslinski, and T. Mudge, "Sparse-tpu: Adapting systolic arrays for sparse matrices," in *Proceedings of the 34th ACM International Conference on Supercomputing*, 2020, pp. 1–12.
- [37] H. Kwon, A. Samajdar, and T. Krishna, "Maeri: Enabling flexible dataflow mapping over dnn accelerators via reconfigurable interconnects," in *Proceedings of the Twenty-Third International Conference* on Architectural Support for Programming Languages and Operating Systems, 2018, pp. 461–475.
- [38] C.-Y. Gui, L. Zheng, B. He, C. Liu, X.-Y. Chen, X.-F. Liao, and H. Jin, "A survey on graph processing accelerators: Challenges and opportunities," *Journal of Computer Science and Technology*, vol. 34, no. 2, pp. 339–371, 2019.
- [39] P. Yao, L. Zheng, X. Liao, H. Jin, and B. He, "An efficient graph accelerator with parallel data conflict management," in *Proceedings* of the 27th International Conference on Parallel Architectures and Compilation Techniques, 2018, pp. 1–12.
- [40] A. Addisie, H. Kassa, O. Matthews, and V. Bertacco, "Heterogeneous memory subsystem for natural graph analytics," in 2018 IEEE International Symposium on Workload Characterization (IISWC). IEEE, 2018, pp. 134–145.
- [41] T. J. Ham, L. Wu, N. Sundaram, N. Satish, and M. Martonosi, "Graphicionado: A high-performance and energy-efficient accelerator for graph analytics," in 2016 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO). IEEE, 2016, pp. 1–13.
- [42] G. Li, G. Dai, S. Li, Y. Wang, and Y. Xie, "Graphia: an in-situ accelerator for large-scale graph processing," in *Proceedings of the International Symposium on Memory Systems*, 2018, pp. 79–84.
- [43] V. Dadu, J. Weng, S. Liu, and T. Nowatzki, "Towards general purpose acceleration by exploiting common data-dependence forms," in *Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture*, 2019, pp. 924–939.



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