Guest Editorial Introduction to the Special Issue on the 2021 Symposium on VLSI Circuits

THIS Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS highlights some of the outstanding papers presented at the Symposium on VLSI Circuits, held June 13–19, 2021. The Symposium was held fully virtually in 2021, as it was in 2020, to prioritize the safety of attendees during the COVID-19 pandemic. The virtual platform provided numerous live events to encourage the participants to enjoy interactive communication. In addition to live Q&A sessions with the authors, the demonstration session integrated into social communication hours provided a place for the participants to communicate live with each other, as well as direct discussion with the demo presenters. During the panel sessions, the panelists answered questions from the audience on the spot with open discussions.

Founded in 1987, the Symposium on VLSI Circuits is jointly sponsored by the IEEE Solid-State Circuits Society and the Japan Society of Applied Physics in cooperation with the Institute of Electronics, Information, and Communications Engineers and the IEEE Electron Devices Society. The Symposium on VLSI Circuits is jointly organized and co-located with the Symposium on VLSI Technology and thus provides excellent opportunities for interactions among integrated circuit and technology experts on topics of mutual interest. As the new normal emerges, the VLSI Symposia are committed to developing new ways to deliver content and to providing enhanced opportunities for interaction.

The 2021 VLSI Symposium on Circuits received 300 submissions. The program committees selected 102 papers for presentation, including processors, system-on-a-chip (SoC), machine learning accelerators, digital circuits, memories, power conversion circuits, biomedical circuits, analog amplifiers and filters, data converters, sensors and displays, wireless and wireline communications, frequency generation, and clock circuits. This issue of the journal contains 20 outstanding articles selected as highlights of presentations from the 2021 Symposium. The journal articles described the research work presented at the 2021 Symposium in greater detail than the papers provided in the Symposium digest. The articles were subject to the standard journal review process. We enjoyed working with the authors of these articles and hope that the technical details presented in these articles will be interesting and useful to the readers of the journal. The following is a summary of the contents of this Special Issue.

The first two articles in this issue present efficient implementations of domain-specific processors. Versa is an energy-efficient 36-core systolic multiprocessor from the University of Michigan, with dynamically reconfigurable interconnects and memory. The trade-off between efficiency and dynamic reconfigurability is demonstrated on a range of common computational kernels. OmniDRL is an energy-efficient processor for deep reinforcement learning (DRL) training and acceleration on edge devices from the Korea Advanced Institute on Science and Technology (KAIST). By implementing hardware support for sparsity in the datasets, the processor achieves very high peak energy efficiency with DRL workloads.

The next two articles explore the use of non-traditional device technologies for processing machine-learning workloads. Chimera, from Stanford University and TSMC, explores deep neural network (DNN) training and inference for edge devices, using a RISC-V core, a DNN accelerator and on-chip resistive RAM (RRAM). To be able to process a practical ResNet-18 network without external DRAM, the authors place six Chimera chips on a printed circuit board and demonstrate a complete system functionality. Hermes core, from IBM Research, demonstrates a mixed-signal approach to processing neural network workloads using phase-change memory added to a 14 nm CMOS process.

An article from Yonsei University and Samsung proposes an SRAM write-assist technique to address the impact of interconnect scaling in recent CMOS technology nodes. They demonstrate an improvement in both writeability and performance of a 32-kb SRAM macro with a modest area penalty in a 28 nm CMOS process.

The two articles that follow cover the biomedical applications. The authors from the National University of Singapore present a programmable patient-specific closed-loop epilepsy tracking SoC that features one-shot learning and online tuning, alleviating the need for training data from a broad range of patients. An article from the University of Michigan details the design of a near-infrared neural recording chip for motor prediction in patients. The design is tolerant to environmental light, and its functionality is validated with both *in-vivo* and pre-recorded signals.

An article from Samsung features a two-chip supply modulation solution for efficient RF power amplification using a switched-mode supply modulator and a linear-assisted hybrid modulator to support simultaneous transmission on LTE and 5G bands. Together, the two chips implement an envelope-tracking power amplifier with 23 dBm output power and high efficiency.

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Intel Labs have used a pair of dies in the same package to demonstrate a high-current, high switching frequency buck DC–DC converter. The article presented a low-voltage GaN NMOS power transistor, co-packaged with a standard CMOS companion chip to achieve up to 94.2% efficiency.

The next two articles advance the state-of-the-art in analog-to-digital converters (ADCs). An OTA-free 1-1 MASH ADC is described by the research group of the University of Buffalo, Arizona State University, and NXP Semiconductors. The architecture that uses a passive noise-shaping (NS) SAR as the first stage and a ring VCO as the second stage addresses the challenge of driving a large input capacitor for high-resolution NS-SAR ADCs. The Interuniversity Microelectronics Centre (IMEC) presents a single-channel, fully dynamic pipelined-SAR ADC with relaxed architectural trades-offs. The use of ring amplification and background calibration achieves 10.1 ENOB and 75.5-dB SFDR with 3.3 mW at 500 MS/s.

Three articles on sensor and analog circuit techniques improve energy efficiency and advance the functionality of sensor systems. Samsung Electronics demonstrates a global-shutter CMOS image sensor with pixel-level ADC and in-pixel memory. The sensor performs at a high-speed of 1200 fps and a low-power consumption of 116.2 mW with a video rate. For low-power Internet-of-Things (IoT) systems, the University of Michigan presents an acoustic analog front-end based on a delta-sigma-modulated sample-and-average common-mode feedback technique. The design in the 180-nm CMOS process demonstrates 192 nW power consumption. For class-D amplifiers widely used in audio applications, the Delft University of Technology and Goodix Technology present a dual-loop architecture that suppresses LC filter nonlinearity by 49 dB and makes the amplifier robust to $\pm 30\%$ variations at its cutoff frequency.

Two clocking articles showcase improvements in the quality of clock generation. Tsinghua University presents a fast chirp-rate and wide chirp-bandwidth digital PLL. The type-II FMCW PLL detects frequency error as its input, which enables self-adapted gain tracking and generates a precise triangular chirp with 2.27 GHz bandwidth and 18.2 μs period at the center frequency of 12.5 GHz simultaneously. In an article from the Korea Advanced Institute of Science and Technology and the University of Michigan, a temperature-compensated crystal oscillator with a pulsed-injection XO driver achieves an accuracy of ± 4.2 ppm from -20 °C to 85 °C and an Allan deviation floor of 34 ppb while consuming 43 nW.

To address increasing demands on data bandwidth, Intel demonstrates a hybrid-integrated 4-λ micro-ring-modulator-based wavelength-division multiplexed optical transmitter for co-packaged optics. The transmitter supports up to 112 Gb/s per wavelength using high-bandwidth micro-ring modulators together with nonlinear equalization. For in-package die-to-die communication, researchers at Xilinx describe a design of a 1.24-pJ/b 112-Gb/s PAM4 transceiver test chip in a 7 nm FinFET. The transceiver achieves $<1^{-12}$ BER over 20 mm channel at 112 Gb/s.

The Special Issue concludes with two wireless communications articles. For 5G relay systems, a 28-GHz phased-array transceiver from the Tokyo Institute of Technology employs 24-GHz wireless power transfer to realize the battery-less relay operation. The transmitter with vector-summing backscatter covers the 360° phase range with a 7-bit resolution and achieves a -2.2 dBm saturated EIRP. A second article from the University College Dublin proposes an interleaving switched capacitor RFDAC, using an edge combiner within the output stage to implicitly triple its effective clock frequency and enable the mm-wave operation.

This Special Issue required substantial efforts from the authors and the reviewers to meet the high standards of quality maintained by the journal. We would like to thank them for their efforts. We would also like to thank the Japan/Far East and North America/Europe Technical Program Committees of the Symposium on VLSI Circuits for coordinating and successfully running the conference, and for recommending articles for this Special Issue. We highly appreciate their work and the support of the Symposium's Executive Committees. Finally, we would like to thank the Journal Editor-in-Chief Dr. Pavan Hanumolu for his guidance, and the staff of the IEEE Transactions and Journals Department for their invaluable assistance in publishing this issue.

In closing, we encourage readers to attend the 2022 Symposium on VLSI Technology and Circuits to be held June 12–17, 2021. After over four decades of parallel existence, the Symposium on VLSI Technology and the Symposium on VLSI Circuits have merged into one Symposium on VLSI Technology and Circuits to facilitate better integration of the two technical fields. The 2022 Symposium will be organized as a hybrid event with both live sessions on-site to enable networking opportunities, and on-demand sessions to allow access to selected talks and panels to those who cannot travel. We also look forward to meeting you at the Symposium. Please visit the Symposium website, www.vlsisymposium.org, for more details.

YUSUKE OIKE, *Guest Editor*
Sony Semiconductor Solutions
Kanagawa 243-0014, Japan
e-mail: yusuke.oike@sony.com

BORIVOJE NIKOLIĆ, *Guest Editor*
Department of Electrical Engineering
and Computer Sciences
University of California at Berkeley
Berkeley, CA 94720 USA
e-mail: bora@eecs.berkeley.edu

Yusuke Oike (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 2000, 2002, and 2005, respectively.

He joined Sony Corporation, Tokyo, in 2005, where he was involved in the research and development of architectures, circuits, and devices for image sensors. From 2010 to 2011, he was a visiting scholar at Stanford University, CA, USA. He is currently appointed as a Distinguished Engineer of Sony Group Corporation, Tokyo. Currently, he is in charge of developing CMOS image sensors as a Deputy Senior General Manager at Sony Semiconductor Solutions, Kanagawa, Japan.

Dr. Oike was a member of the 2012–2016 ISSCC Technical Program Committees. He is currently the General Co-Chair of the IEEE Symposium on VLSI Technology and Circuits.

Borivoje Nikolić (Fellow, IEEE) received the Dipl.Ing. and M.Sc. degrees in electrical engineering from the University of Belgrade, Belgrade, Serbia, in 1992 and 1994, respectively, and the Ph.D. degree from the University of California at Davis, Davis, CA, USA, in 1999.

In 1999, he joined the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, USA, where he is currently a National Semiconductor Distinguished Professor of engineering.

Dr. Nikolić received the NSF CAREER Award in 2003, the College of Engineering Best Doctoral Dissertation Prize, the Anil K. Jain Prize for the Best Doctoral Dissertation in Electrical and Computer Engineering at the University of California at Davis in 1999, and the City of Belgrade Award for the Best Diploma Thesis in 1992. For work with his students and colleagues, he has received the best paper awards at the IEEE International Solid-State Circuits Conference, Symposium on VLSI Circuits, IEEE International SOI Conference, European Solid-State Device Research Conference, European Solid-State Circuits Conference, S3S Conference, Design Automation Conference, and the ACM/IEEE International Symposium of Low-Power Electronics. From 2014 to 2015, he was a Distinguished Lecturer of the IEEE Solid-State Circuits Society. He is a Technical Program Chair for the 2022 Symposium on VLSI Technology and Circuits.