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A Millimeter-Wave CMOS Series-Doherty Power Amplifier With Post-Silicon Inter-Stage Passive Validation

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***Abstract*— This article presents a wideband series-Doherty power amplifier (SDPA) for millimeter-wave (mm-wave) fifth-generation (5G) applications. It features a compact two-step impedance inverting-based series-Doherty power combiner that provides broadband close-to-perfect power back-off (PBO) efficiency enhancement. The amplitude-to-amplitude (AM–AM)/amplitude-to-phase (AM–PM) performance of the load-modulated Doherty power amplifier for broadband operation is analyzed. We also devise a post-silicon inter-stage passive validation (PSIV) approach to evaluate the mm-wave chip prototype utilizing the embedded voltage root mean square detectors. The proposed SDPA is realized in a 40-nm bulk CMOS, and it delivers 20.4 dBm P_{SAT} with 39.1%/34% PAE at 0-/6-dB PBO. Over a 23.5–30 GHz band, its PAE is >24% at 6-dB PBO. At 27 GHz, applying a "2 GHz 16-quadratic-amplitude modulation (QAM) orthogonal frequency-division multiplexing (OFDM)" signal, the proposed SDPA generates 10.2 dBm average power with 18.9% average PAE. The average error vector magnitude is better than −24.5 dB without digital predistortion for a "400-MHz 64-QAM OFDM" signal while generating an average output power of 8.8 dBm with 15% PAE. The AM–AM/AM–PM of the realized SDPA is investigated by employing a "50-MHz 64-QAM OFDM" signal, validating our analysis and showing that the linearity limitation of DPAs is systematic and predictable. Utilizing the proposed PSIV approach, the frequency response of the input/inter-stage passive circuits is measured, indicating an excellent agreement with 3-D electromagnetic (EM) simulation results.**

***Index Terms*— Doherty power amplifier (DPA), impedance inverter, power amplifier (PA), root mean square (rms) detector, series-DPA (SDPA), transformer, wideband.**

I. INTRODUCTION

MILLIMETER-WAVE (mm-wave) fifth-generation (5G) communication systems employ phased arrays to overcome the free-space path loss while providing high data throughput and low-latency line-of-sight links [1]–[3]. They typically employ spectrally efficient complex modulation schemes, such as high-order quadratic-amplitude modulations (QAMs) with high peak-to-average-power ratios (PAPRs) [4]. As shown in Table I, they pose stringent requirements on power amplifier's (PA's) in-band linearity, verified by the error vector magnitude (EVM), and out-of-band spectral purity, examined by adjacent channel leakage ratios (ACLRs) [5], [6].

TABLE I
5G SYSTEM REQUIREMENTS [5], [6]

PAPR for various modulation schemes (Filter roll-off factor = 0.25)					
Modulation	16QAM SC	64QAM SC	QPSK OFDM	16QAM OFDM	64QAM OFDM
PAPR	6.9dB	7.1dB	9.7dB	10.4dB	11dB
3GPP minimum EVM requirement					
Modulation	BPSK	QPSK	16QAM	64QAM	256QAM
Required EVM	30% (-10.5dB)	17.5% (-15dB)	12.5% (-18dB)	8% (-21.9dB)	3.5% (-29.1dB)
FR2 5G application scenarios and requirements (Antenna gain=5dB & connection loss=2dB)					
Scenario	Handset	Access point		Base station	Backhaul
$EIRP_{AVG}$	30dBm	45dBm		55dBm	60dBm
# of antennas	4-6	32		64	256
P_{AVG}	11-15dBm	12dBm		16dBm	9dBm
P_{1dB} (PAPR=11dB)	22-26dBm	23dBm		27dBm	20dBm
Targeted PAE_{AVG}	20%	20%		20%	20%

Meanwhile, low-cost nanoscale CMOS technologies are exploited to enable maximum integration, compact die area, and high yield. Nevertheless, generating the required power levels using CMOS technologies is challenging, especially with their limited supply voltage and maximum oscillation frequency (f_{max}). Table I presents the average and peak power requirements of 5G application scenarios. For instance, in the backhaul application with 16 × 16 antenna arrays, the average/peak PA power should exceed 9 dBm/20 dBm. Furthermore, since the PA governs the overall performance of the transmitter (TX), its average efficiency directly determines the system efficiency, thus its thermal handling capability [5], [7].

Several mm-wave linear PAs are proposed to address the 5G specifications [8]–[14]. To alleviate the efficiency issue, outphasing TXs offer high average efficiency, but they demand significant baseband overhead to generate outphasing signals and intensive digital predistortion (DPD) [15]–[19]. In contrast, load-modulated balanced amplifiers (LMBAs) [20], [21] and Doherty PAs (DPAs) [22]–[38] are "RF-in–RF-out" power back-off (PBO) efficiency enhancement front-end solutions that support wideband modulations. The LMBA structure con-

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sists of two main PAs and an auxiliary PA combined through a quadrature-hybrid coupler. Apart from its intrinsic wideband operation, the LMBA's power combiner complexities require a large die area, giving rise to a high insertion loss, thus diminishing its peak PAE. On the other hand, mm-wave DPAs are inherently narrowband due to their lumped-element quarter-wave transmission line (QTL) impedance inverter, necessary for load modulation. However, the broadband operation is achievable by increasing the complexity of the Doherty power combiner, compromising its passive efficiency [24], [29], [32]. Also, their optimum PAE at PBO is narrowband in these architectures while providing broadband $P_{1\,\mathrm{dB}}$ [33], [34]. Therefore, realizing a compact mm-wave front-end with high average efficiency over broad operating frequencies while satisfying the tight element-to-element $\lambda/2$ lattice spacing requirement of the phased arrays is still challenging.

This article introduces a series-DPA (SDPA) architecture with a two-step impedance inverting-based power combiner [39]. In addition to its broad $P_{1\,\mathrm{dB}}$ bandwidth operation, it supports the desired 5G band, 24–30 GHz, with $>24\%$ 6-dB PBO PAE. The design strategy is first to investigate the limitations of the basic Doherty topologies by examining their operational bandwidth. Choosing the SDPA structure, we then synthesize a compact power combiner comprising two identical transformers, a coupled line connection, and a capacitor. In [40], we recently presented a TX architecture with a balanced amplifier and similar series-Doherty power combiner while employing common-source PAs at each branch. Nevertheless, its main contributions were antenna impedance mismatch resilience and additional I/Q image rejection. In this work, double-neutralized cascode push-pull PAs are utilized in main/auxiliary paths to ensure stability over the entire operating band while generating the required output power with high PAE at both peak power and 6-dB PBO.

Moreover, the proposed DPA features embedded voltage root mean square (rms) detectors to verify the system's reliability. We proposed a post-silicon inter-stage passive circuit validation (PSIV) approach to evaluate the mm-wave front-end chip prototype utilizing the embedded rms detectors. The proposed PSIV approach can prevent discrepancies caused by modeling inaccuracy in the final product. It becomes particularly crucial when accounting for all the parasitic is not always possible in the simulation [41].

This article is organized as follows. Section II reviews PDPA and SDPA topologies and investigates their bandwidth and linearity limitations. The proposed two-step SDPA is presented in Section III. Section IV elaborates on circuit implementation details of the DPA prototype fabricated in the 40-nm bulk CMOS technology. The proposed post-silicon inter-stage passive validation (PSIV) approach is described in Section V, comparing simulation and measurement results. Section VI presents the experimental results, and we conclude the article in Section VII.

II. DPA Topologies Bandwidth Limitations

Fig. 1 exhibits simplified DPA topologies [42] and their current/voltage profiles. In general, a DPA is a combination

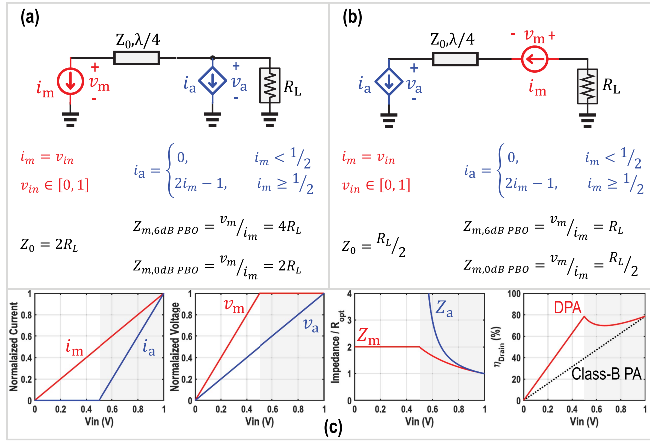


Fig. 1. Simplified form of (a) PDPA and (b) SDPA at their designated carrier frequency. (c) Currents, voltages, impedances, and drain efficiency of the PDPA/SDPA.

of the main PA (i_m), which determines the output power, and the auxiliary PA (i_a) that modulates the main PA's load (Z_m) to keep its drain voltage (v_m) at the maximum swing, maintaining the maximum efficiency. Therefore, in Fig. 1(a) and (b), the main PA is modeled as an independent current source (i_m) while the auxiliary PA is modeled as a current-controlled current source (i_a). Besides, a QTL is employed as an impedance inverter to realize load modulation. The DPA can be configured either in PDPA or SDPA. However, the main and auxiliary PA's current forms are the same as demonstrated in Fig. 1(c). As shown, owing to the load modulation, the overall drain efficiency obtains a peak efficiency at 6-dB PBO, improving the efficiency by $\times 2$ over a conventional class-B PA.

A. Gain and Phase Deviation Caused by Q Modulation

The linearity limitations of conventional DPAs are investigated in the literature [43], [44]. However, the mm-wave CMOS DPA design requires thorough analysis to address 5G stringent design specifications. As illustrated in Fig. 1, a QTL is used as an impedance inverter to maintain load modulation. However, the QTL acts as a perfect impedance inverter only at its designated center frequency (f_c), thus deviating from f_c affects its performance. In addition, an inductor (L) is typically utilized to absorb the parasitic capacitor (C) of the PA, adding an LC resonator at f_c to the Doherty combiner. Subsequently, as shown in Fig. 2(a), the resonator's quality factor (Q) is modulated by load modulation resulting in magnitude and angle deviations. Likewise, the bandwidth of the QTL varies while its load modulates from $2Z_0$ to Z_0, where Z_0 is QTL's characteristic impedance. Fig. 2(b) exhibits the S-parameter simulation results of a QTL at 28 GHz, showing gain and phase deviations.

In mm-wave DPAs, the device parasitic capacitors are absorbed in either a transformer-based [26]–[31] or coupled line-based [32]–[34] baluns. In either case, the described phenomenon is directly translated into amplitude-to-amplitude (AM–AM) and amplitude-to-phase (AM–PM) distortions in wideband operation.

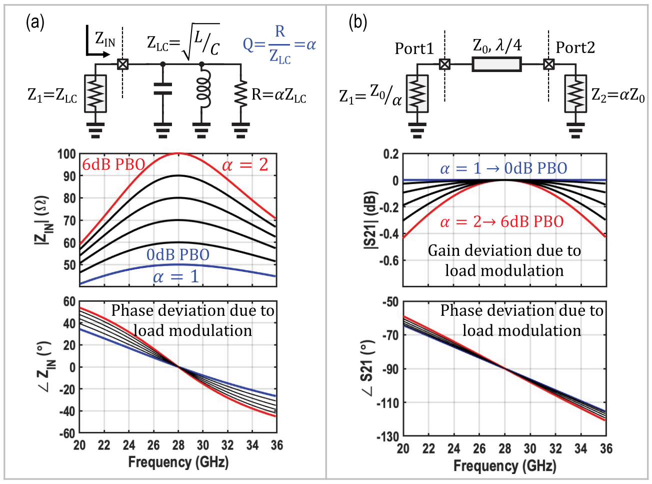


Fig. 2. (a) Q-modulation of an RLC resonator at 28 GHz showing magnitude and angle deviation of its impedance. (b) Gain and phase deviations of a QTL under load modulation.

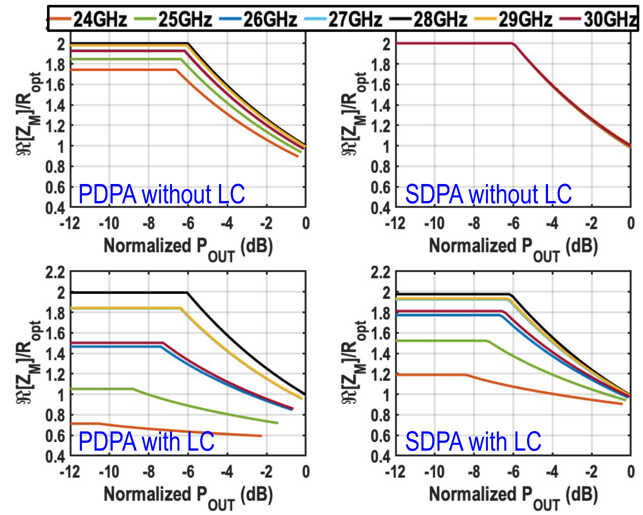


Fig. 4. Real part of main PA's load, normalized to R_{opt}, for PDPA and SDPA with and without LC resonators.

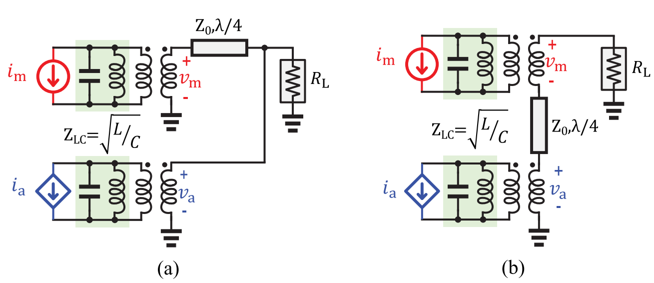


Fig. 3. Practical forms of (a) PDPA and (b) SDPA with ideal transformers and inductors to resonate out PAs' parasitic capacitors.

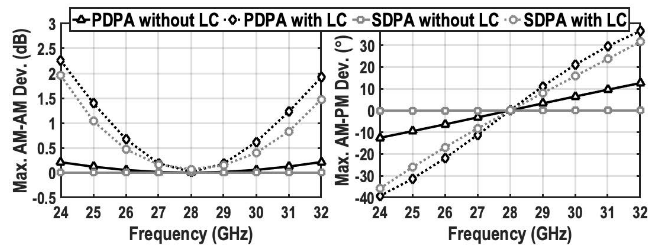


Fig. 5. Maximum AM–AM/AM–PM deviations of PDPA and SDPA with and without LC resonators.

B. Bandwidth Analysis of PDPA and SDPA

Fig. 3 demonstrates practical mm-wave PDPA and SDPA models. The current sources are connected to the matching network by an ideal 1:n transformer. Note that employing transformers is inevitable for connecting the push-pull PAs to its Doherty combiner at mm-wave frequencies. Besides, the LC resonators are considered alongside the current sources to model their absorbed device capacitors. Applying the current waveforms shown in Fig. 1(c), the normalized main PA's load impedance is depicted versus normalized output power at various frequencies (Fig. 4). As demonstrated, even without an LC, due to the QTL at the main PA path, the load modulation of PDPA and output power slightly degrade when operated away from its center frequency (28 GHz). Adding LC resonators exacerbates PDPA's performance.

On the other hand, SDPA offers frequency-independent output power with ideal load modulation. It is due to its main PA acting as a high-impedance power device, which is modeled as an ideal current source, and perfectly isolates the auxiliary PA from the output. Besides, since the main PA directly drives the resistive output load, the output power is frequency independent. However, the auxiliary PA is no longer isolated from the output by adding an LC resonator alongside the main PA, causing output power and load modulation degradation, as shown in Fig. 4. Nevertheless, it can be observed that even with an LC resonator, the SDPA provides a broader load modulation and much more stable output power than PDPA, where the output power deviations of SDPA and PDPA are 0.4 and 2.2 dB, respectively (see Fig. 4, bottom).

Moreover, the AM–AM and AM–PM of PDPA and SDPA are simulated with and without LC resonators. As depicted in Fig. 5, without an LC resonator, the maximum AM–AM/AM–PM deviations of PDPA slightly increase when operated away from its center frequency (28 GHz), while SDPA's AM–AM/AM–PM deviations are always zero. Adding LC resonators exacerbates their AM–AM/AM–PM performance, becoming 2.3 dB/$-40°$ and 1.9 dB/$-36.5°$ for PDPA and SDPA, respectively. It indicates that even though the SDPA offers significantly broader load modulation performance, the Q modulation phenomena shown in Fig. 2 degrade the AM–AM/AM–PM distortions of both topologies almost equally.

In summary, in both configurations with realistic device capacitance, load modulation creates AM–AM and AM–PM distortions when a DPA operates far from its center frequency. However, SDPA clearly shows broader load modulation and output power as an efficiency enhancement PA, making it a suitable choice to support the mm-wave 5G operational band (e.g., 24–30 GHz). Furthermore, in practice, lossy components mitigate the AM–PM distortions by diminishing Q modulation of LC resonators and QTLs. Moreover, we can infer that

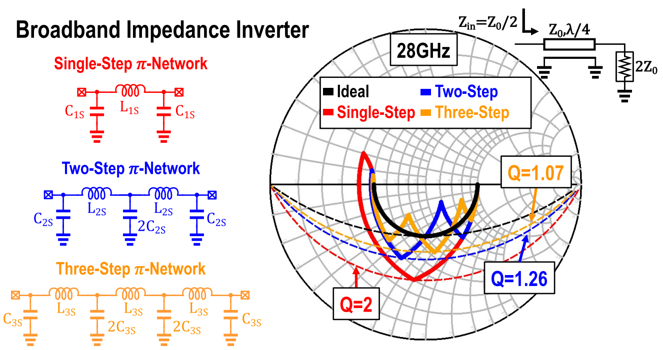


Fig. 6. Single-, two-, and three-step C–L–C π-network QTL implementations and their inversion paths from $2Z_0$ to $Z_0/2$.

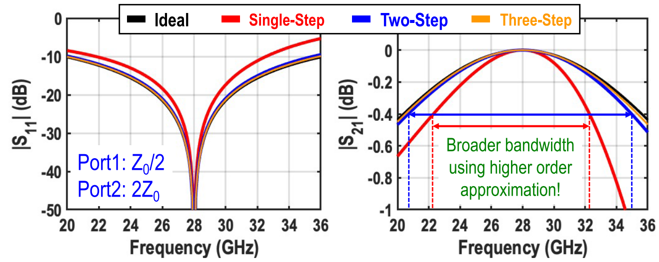


Fig. 7. Simulated S_{11} and S_{21} of different QTLs.

extending the load modulation backward (e.g., 12-dB PBO) exacerbates Q modulation, thus worsening the AM–AM/AM–PM deviations. Additionally, as suggested in [29], by employing static phase aligners in the main and auxiliary PAs, the frequency coverage can be extended at the cost of the die area overhead.

C. Wideband Lumped-Element Two-Step Impedance Inverter

Heretofore, an ideal QTL is considered as the impedance inverter in the earlier discussions and simulations. However, the impedance inverter of an mm-wave DPA is often realized by a lumped-element QTL to address phased array systems' strict die area restrictions. The designated QTL plays a critical role in a Doherty power combiner performance. Therefore, in this section, three possible lumped component implementations of the QTLs are investigated. Fig. 6 illustrates the single-step ($\lambda/4 \rightarrow \theta_{1S} = 90°$), two-step ($2 \times \lambda/8 \rightarrow 2 \times \theta_{2S} = 90°$), and three-step ($3 \times \lambda/12 \rightarrow 3 \times \theta_{3S} = 90°$) capacitor–inductor–capacitor (C–L–C) π-network QTLs. Considering an n-step lumped element QTL with Z_0 characteristic impedance, L_{nS} and C_{nS} can be calculated as [25]

$$L_{nS} = \frac{Z_0 \sin \theta_{nS}}{\omega_c} \tag{1}$$

$$C_{nS} = \frac{\tan \frac{\theta_{nS}}{2}}{Z_0 \omega_c} \tag{2}$$

where $\theta_{nS} = 90°/n$ and ω_c is designated center angular frequency ($\omega_c = 2\pi \times f_c$).

The inversion paths of a $2Z_0$ impedance to $Z_0/2$ of an ideal QTL compared to three C–L–C π-networks are plotted in the smith chart depicted in Fig. 6. Considering that the quality factor represents the bandwidth ($Q = (\omega_c/\Delta\omega)$, where $\Delta\omega$ is the half-power bandwidth) during impedance inversion, the inversion path of single-step touches constant $Q = 2$ line while the two-step and three-step cross $Q = 1.26$ and $Q = 1.07$. Therefore, the broadband operation is achievable by a higher-order approximation of the QTL. Comparing the simulated Q of QTLs, Fig. 6 indicates that a two-step structure compared to a single-step one improves the bandwidth by 59%, whereas it becomes 87% using a more complicated three-step counterpart. Fig. 7 exhibits S-parameter simulation results of different QTLs, where Port1 and Port2 are $Z_0/2$ and $2Z_0$, respectively. As demonstrated, S_{11} of a single step is a narrow band, while two-/three-step QTLs provide the matching condition as good as an ideal QTL. Likewise, S_{21} of the single-step QTL exhibits narrower bandwidth compared to the three other QTLs. Consequently, choosing a two-step QTL improves the bandwidth reasonably while trading off its passive complexity.

III. Proposed Series-Doherty Power Combiner

Fig. 8 unveils the proposed transformer-based two-step series-Doherty power combiner in four progressive steps considering identical main and auxiliary PAs. First, the SDPA introduced in Fig. 3(b) is depicted by replacing the ideal QTL with the proposed two-step C–L–C π-network [Fig. 8(a)]. The phase shift of the QTL's first and second steps (θ_1 and θ_2) are considered different as a degree of freedom, while their combined phase must be 90°. However, θ_1 and θ_2 should be almost the same to benefit from bandwidth improvement. The shunt inductors (L_M) resonate out the main/auxiliary PAs parasitic capacitors (C_P) at the desired frequency. Besides, n is chosen to provide the PAs' optimum load (R_{opt}).

As shown in Fig. 8(b), a series inductor (L_3) is employed to absorb the output pad's parasitic capacitor (C_L). Additionally, the shunt inductors are moved to the secondary side of the transformers (L'_M). By assuming $L_1 = L_3 = L_K$, L'_M, and L_K can be considered magnetizing and leakage inductors of a nonideal transformer, respectively. Consequently, the ideal transformers and their corresponding inductors are replaced by nonideal transformers with a k_m coupling factor, as demonstrated in Fig. 8(c). Besides, the C_1 shunt capacitor of the impedance inverter is absorbed into the parasitic capacitor of the auxiliary PA ($C_P \rightarrow C_P + C'_1$).

Lastly, the second single-ended π-network is replaced by a three-port coupled lined with a differential input and single-ended output to improve ground signal path loss and diminish the auxiliary PA's unbalanced signals. The progressive steps of this transformation are demonstrated in Fig. 9. First, the single-ended π-network is converted to a differential network. As the characteristic impedance must stay the same, the value of inductances becomes half of its single-ended counterpart $((L_S/2))$. Since self-coupling of a differential inductor is inevitable, the inductors are replaced by a coupled line assuming a positive coupling. The positive coupling factor (k_S) reduces the differential inductance by $(1 - k_S)$, thus the required inductance becomes larger ($L'_S = (L_S/2(1 - k_S))$). As the last step, the output was modified to a single-ended

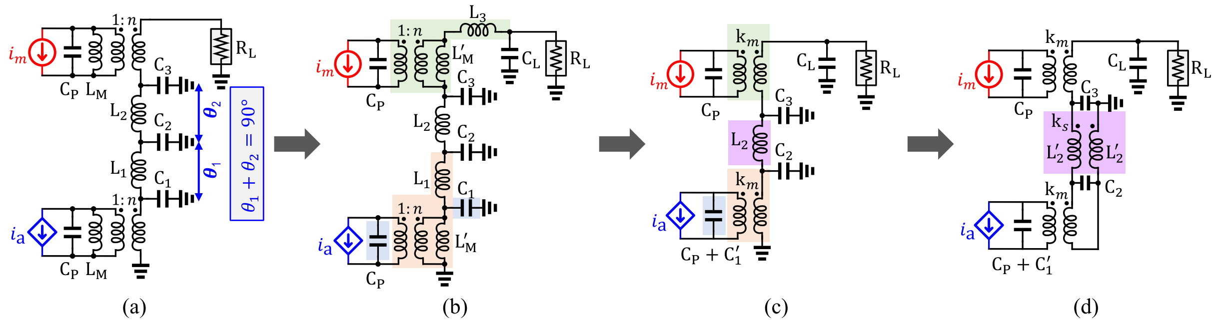


Fig. 8. (a) SDPA with two-step C–L–C π-network. (b) Output pad's parasitic capacitor (C_L) and a series inductor (L_3) for impedance matching are added, while L_M moved to the secondary sides of the transformers. (c) Ideal transformers and their corresponding inductors are replaced by non-ideal transformers with a k_m coupling factor. (d) Second π-network series inductor (L_2) is replaced by a coupled-lines connected as a triaxial balun.

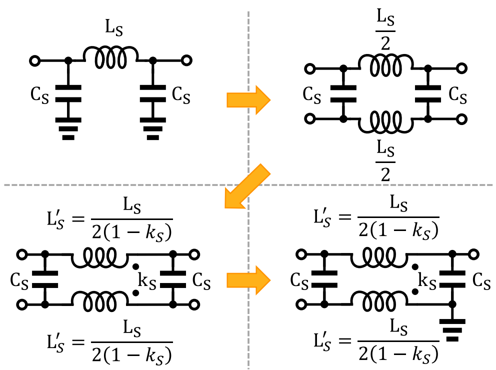


Fig. 9. Progressive steps of replacing the two-port single-ended π-network with a three-port differential-to-single-ended network.

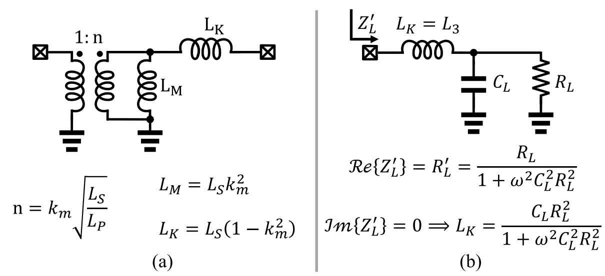


Fig. 10. Equations of (a) lumped-element model of a transformer and (b) L-network impedance matching.

connection intact. However, in practice, since a single-ended connection changes the parasitic capacitors' states, a minor modification is required to recover the desired performance. Note that k_S is a degree of freedom to adjust the length of the lines and achieve the optimum layout. Also, C_3 is removed for further Doherty phase alignment.

A. Proposed Series Doherty Combiner Design Framework

In this section, the closed-form design equations of all parameters introduced in Fig. 8 are derived. Fig. 10 reflects the equations of the lumped-element model of a transformer [45] and L-network impedance matching, which will be employed to synthesize the proposed series combiner. The primary and secondary inductors of the transformer are denoted as L_P and L_S, respectively.

To begin with, the primary inductor of the transformer, exploited to absorb the parasitic capacitor of the PA (C_P), can be calculated as

$$L_P = \frac{1}{\omega_c^2 C_P}. \tag{3}$$

Using the equations introduced in Fig. 10, the converted load can be expressed as

$$R_L' = \frac{R_L}{1+Q^2} = \frac{R_L}{1+\omega_c^2 C_L^2 R_L^2}. \tag{4}$$

Note that we assume C_P and PA's optimum load (R_{opt}) are extracted according to the desired peak output power. Besides, the turn ratio of the transformer can be expressed as follows:

$$R_{\text{opt}} = \frac{R_L'}{2n^2} \Rightarrow n = \sqrt{\frac{R_L'}{2R_{\text{opt}}}} = k_m\sqrt{\frac{L_S}{L_P}}. \tag{5}$$

Moreover, using the equations shown in Fig. 10, we calculate

$$L_3 = L_K = \left(1-k_m^2\right)L_S = \frac{R_L^2 C_L}{1+\omega_c^2 C_L^2 R_L^2}. \tag{6}$$

Then, by solving (5) and (6), L_S and k_m can be derived as follows:

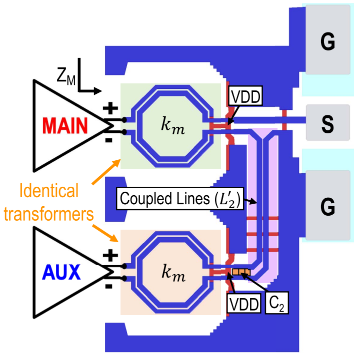
$$L_S = R_L'\left(R_L C_L + \frac{L_P}{2R_{\text{opt}}}\right) \tag{7}$$

$$k_m = \sqrt{\frac{L_P}{2R_{\text{opt}}R_L C_L + L_P}}. \tag{8}$$

Since we assumed $L_1 = L_3$, using (1) and (2), the phase shift of the first step π-network and its corresponding capacitors can be calculated as

$$\theta_1 = \sin^{-1}\frac{2\left(1-k_m^2\right)L_S\omega_c}{R_L'} \tag{9}$$

$$C_1 = \frac{2\tan\frac{\theta_1}{2}}{R_L'\omega_c}. \tag{10}$$



	Components	Value	
Transformer Parameters	Secondery Side Connection	Diff.	Single-ended
	L_P	198pH	206pH
	L_S	164pH	178pH
	k_m	0.65	0.67
	Passive Efficiency	86.7%	85.6%
Lamped Elements	C_2	290fF	
	L'_2	172pH	
	k_S	0.66	
	R_{opt}	56.2Ω	

Fig. 11. Layout of the proposed series-Doherty power combiner and its 3-D EM simulated parameters.

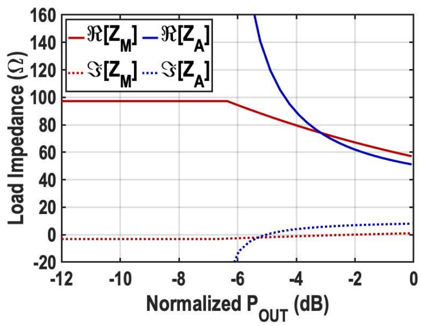


Fig. 12. Real (solid) and imaginary (dotted) parts of main and auxiliary PAs' load impedance versus normalized output power at 28 GHz.

Consequently, considering that $\theta_2 = 90°–\theta_1$, the inductor and capacitors of the second step π-network are expressed as

$$C_3 = \frac{2\tan\frac{90°-\theta_1}{2}}{R'_L\omega_c} \tag{11}$$

$$L_2 = \frac{R'_L \sin(90° - \theta_1)}{2\omega_c}. \tag{12}$$

Since $C_2 = C_1 + C_3$, all design parameters are calculated. The last step is to choose k_S based on layout consideration and to calculate the required L'_2 using (see Fig. 9)

$$L'_2 = \frac{L_2}{2(1-k_S)}. \tag{13}$$

In summary, first, the parasitic capacitors of the output pad (C_L) and the push-pull PA (C_P) are estimated from the available technology. Then, by employing the introduced framework, all initial design parameters can be calculated using (3)–(13). Lastly, we realize the SDPA in the available technology and optimize its performance through electromagnetic (EM) simulations. Note that employing advanced technologies with lower parasitic capacitors leads to better agreement between the initial calculated values based on first-order models and the final realized parameters obtain from EM simulations.

B. Layout and EM Simulation Results

The layout of the proposed series-Doherty combiner is depicted in Fig. 11. It consists of two identical transformers

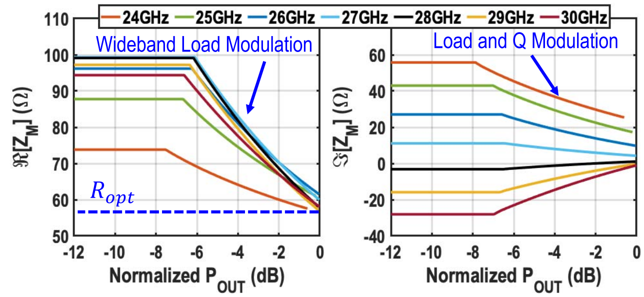


Fig. 13. Real (left) and imaginary (right) parts of the main PA's load impedance at various frequencies.

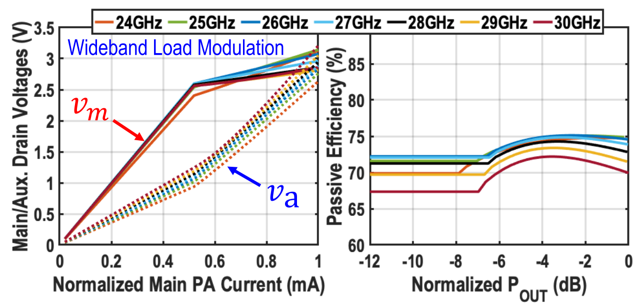


Fig. 14. Main and auxiliary PAs' drain voltages and the passive efficiency of the proposed series-Doherty combiner at various frequencies.

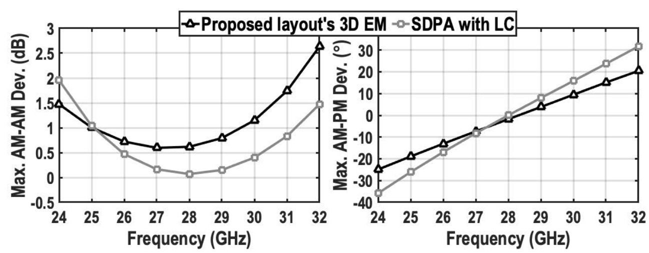
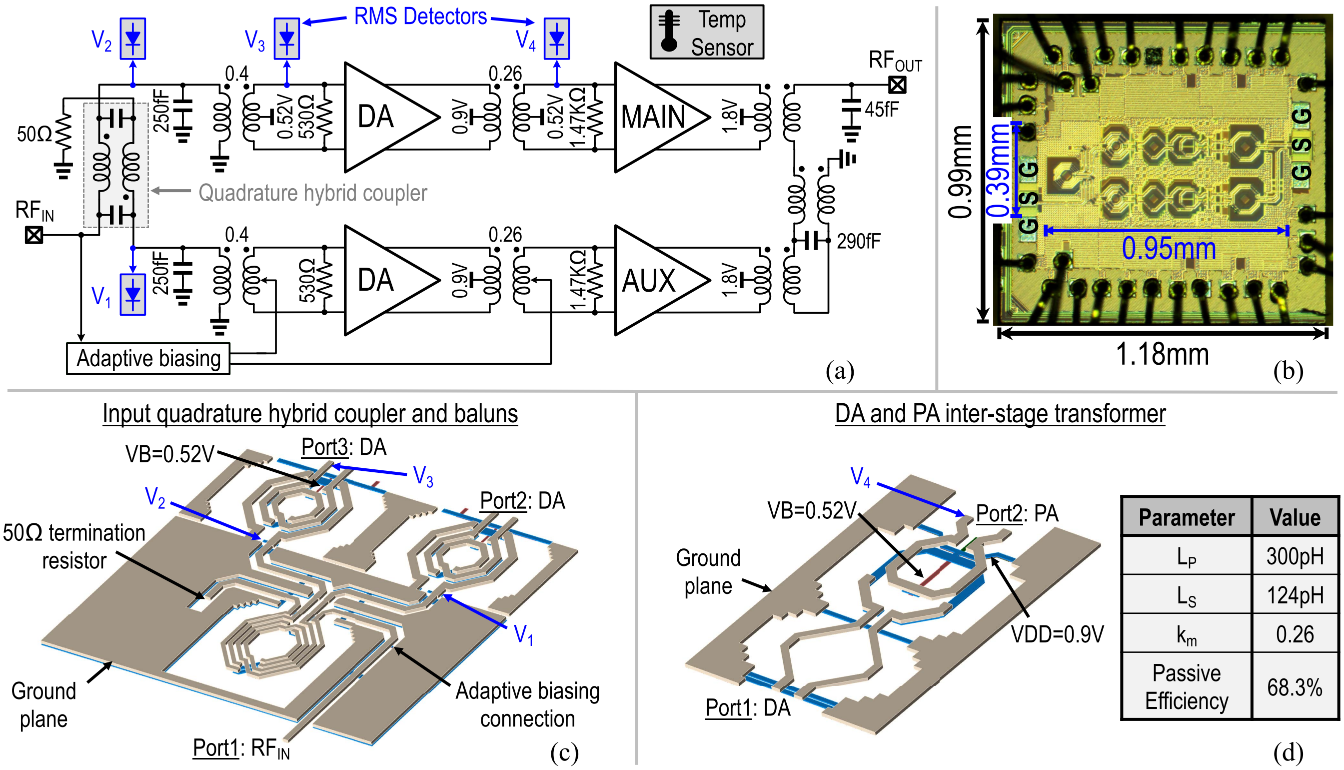


Fig. 15. Maximum AM–AM/AM–PM deviations using 3-D EM model of the proposed series-Doherty combiner compared to ideal SDPA with LC resonators.

with a coupling factor of $k_m = 0.65$ to provide the optimum load of the PAs. The passive efficiency reported in Fig. 11 is calculated based on the maximum passive efficiency formula introduced in [46]. Nonetheless, due to the capacitive coupling between the primary and secondary sides of the transformer, its parameters are slightly different when configured as a balance-to-unbalance (balun) converter. Therefore, since the configurations of the transformers are different for main and auxiliary PAs, the calculated parameters should be adjusted to achieve the desired performance. The real and imaginary parts of main and auxiliary PA's load impedance are exhibited in Fig. 12. According to simulations with an ideal PA model, the proposed layout offers wideband load modulation and efficiency enhancement. Fig. 13 shows the simulated main PA's real and imaginary impedance versus normalized output power in the 24–30 GHz band. Additionally, the main and auxiliary PAs' drain voltages and the passive efficiency of the proposed series-Doherty power combiner are demonstrated in Fig. 14.



Parameter	Value
L_P	300pH
L_S	124pH
k_m	0.26
Passive Efficiency	68.3%

Fig. 16. (a) Detailed schematic of the DPA architecture, (b) die photograph, (c) 3-D view of the input QHC and baluns, and (d) DA and PA inter-stage matching transformer.

Moreover, the AM–AM/AM–PM using the proposed combiner's 3-D EM simulation results are illustrated in Fig. 15. Compared to an ideal loss-less SDPA with *LC* resonators (see Fig. 3), the inherent loss of the power combiner alleviates PA's AM–PM while worsening its AM–AM performance.

IV. Circuit Implementation

The proposed SDPA is implemented in 40 nm bulk CMOS technology. The chip occupies an area of 1.18 mm × 0.99 mm, while its core area is 0.39 mm × 0.95 mm. Fig. 16 exhibits a detailed schematic of the PA architecture, the die photograph, and a 3-D view of the input/interstage passive circuits. A quadrature hybrid coupler (QHC) is employed to generate the 90° phase advance for the DPA and provide wideband input impedance matching. Fig. 17 demonstrates the schematic and *S*-parameter simulation results of the input QHC including the 50-Ω coplanar transmission lines insertion losses. In the simulation, Port1, Port2, and Port3 are input, auxiliary path, and main path, respectively. Its insertion loss is 1.05 dB while providing more than 21-dB isolation between two PAs. Each main/auxiliary branch consists of an input balun, a neutralized driver amplifier (DA), a double-tuned transformer as an inter-stage matching network, and a cascode PA. Adaptive biasing circuits modulate the biases of the auxiliary branch to perform Doherty load modulation. Moreover, four embedded voltage rms detectors are utilized to measure all mid-stage signal levels (V_1–V_4) of the proposed DPA structure. Also, a temperature sensor, that is, a diode-connected bipolar transistor, is employed to measure chip temperature and calibrate the rms detectors.

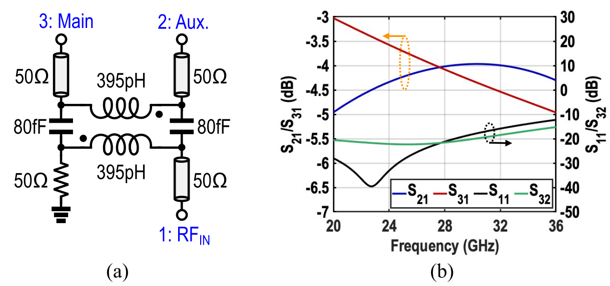


Fig. 17. (a) Schematic of the input QHC and (b) its *S*-parameter simulation results.

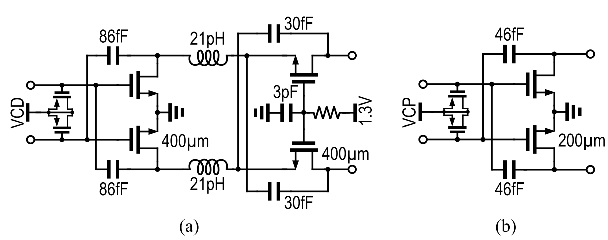
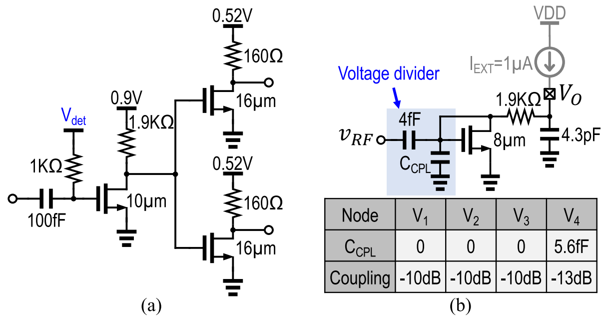


Fig. 18. Schematic of (a) double-neutralized cascode PA and (b) common-source DA.

Fig. 18 depicts the detailed schematic of cascode PA and DA. In [9], the drain–source capacitors of the common-gate



Node	V_1	V_2	V_3	V_4
C_{CPL}	0	0	0	5.6fF
Coupling	-10dB	-10dB	-10dB	-13dB

Fig. 19. (a) Schematic of the adaptive biasing circuits and (b) schematic of the rms detector with its capacitive coupler.

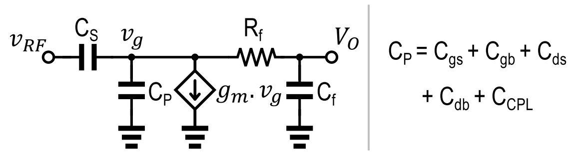


Fig. 20. Simplified small-signal model of an rms detector.

transistors are used to boost the gain, owing to the common-gate transistor's high gain (>1) in a class-AB operation with a sizeable quiescent current. In this work, to realize class-B main/auxiliary PAs, two pairs of neutralization capacitors are used for common-source and common-gate transistors to maximize output-to-input isolation of the PA, resulting in unconditional stability [47]. Besides, two 21 pH inductors align voltage and current wave phases, thus improving the drain efficiency [8]. Each common-source transistor of PA/DA consists of eight/four unit cells with a transistor aspect ratio of 50 μm/40 nm, optimized to mitigate the impact of device parasitics and interconnections [41]. The cascode transistors comprise five unit cells with a transistor aspect ratio of 80 μm/40 nm. Besides, two varactors are utilized at the PA and DA inputs to improve their AM–PM profiles [48].

Fig. 19 illustrates the schematic of the adaptive biasing circuits and the rms detector [49]. Adaptive biasing circuits consist of a single-ended envelope detector and two drivers for DA and PA. Using the detection bias voltage of the envelope detector (V_{det}), the load modulation can be adjusted. The rms detectors are biased with an external 1 μA current source to work in the subthreshold region. Due to the exponential subthreshold voltage-to-current profile of the nMOS, the rms of the input RF signal is down-converted to dc [49]. As demonstrated, capacitive coupling is employed to sense the signal at each node. The series capacitor (4 fF) and shunt capacitors, for example, C_{CPL} and nMOS's parasitic capacitor, form a capacitive voltage divider. Therefore, large C_{CPL} is chosen at the nodes with large swing voltages. Since the series capacitor is 4 fF, the input capacitor of the rms detector is significantly small, and thus its loss is negligible.

V. Post-Silicon Inter-Stage Passive Validation

Although the front-end passive stages (e.g., PA and LNA matching networks) directly determine the system's performance in the mm-wave circuit design, the inter-stage passive networks also affect the overall performance [10], [50]. They include matching networks of inter amplification stages, quadrature local oscillator (LO) generators (e.g., QHC) [40], passive phase shifters [51], splitters, and combiners. In inter-stage matching networks, achieving a broad operating band with reasonable insertion loss is challenging. For instance, in an mm-wave PA, as the transistors' gate resistance is optimized to achieve high $f_{\max}$, they provide high-Q parasitic capacitors. Subsequently, using a transformer to absorb the parasitic capacitors results in overall a high-Q resonator, thus, narrow bandwidth. Therefore, adding an extra resistor to enhance the related operational bandwidth is inevitable. Since the additional resistor decreases power gain, it establishes a critical design tradeoff between bandwidth and PAE, significantly affecting the PA performance.

Therefore, to fully evaluate a prototype chip, it is crucial to measure the performance of the inter-stage passive circuits. Typically, the designers fabricate these circuits separately to measure their passive performance, increasing die area and measurement cost. Nonetheless, considering the variable parasitic capacitance of the active devices, the "dynamic" performance of inter-stage passive networks may vary compared to a standalone implementation. Besides, process/temperature variation and aging can also influence the performance, whereas their effect cannot be measured separately.

This section proposes a PSIV approach to measure the inter-stage matching network bandwidth with negligible insertion loss, die area, and power consumption overhead.

A. Proposed PSIV Approach and Its Limitations

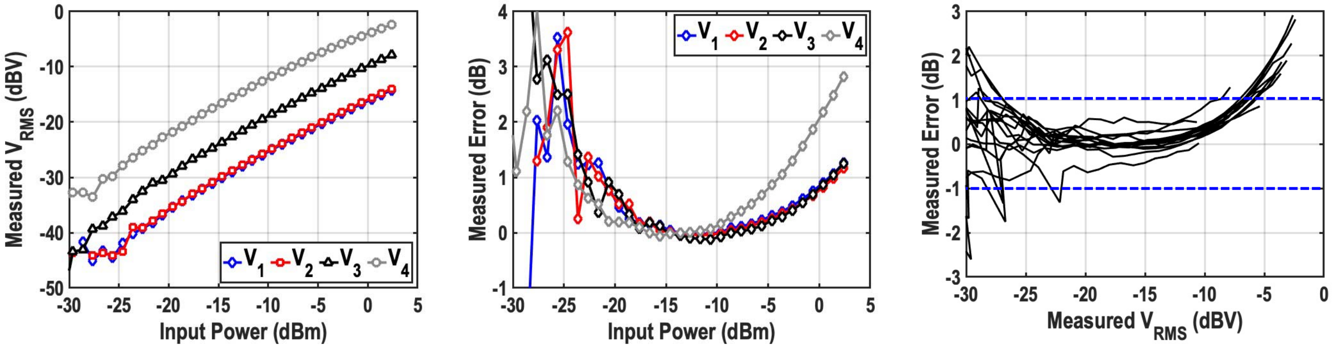
To realize the proposed PSIV approach, we used the earlier introduced rms detectors to quantity the voltage level at each stage [52]. Then, the voltage gain can easily be calculated by dividing the measured voltages. Subsequently, by sweeping the frequency, the inter-stage gain is obtained versus frequency which represents the bandwidth of the designated inter-stage passive network.

The accuracy of PSIV approach is mainly defined by rms detectors' performance and their error mismatches. Fig. 20 depicts a simplified small-signal model of the rms detectors, dismissing all parasitic resistances. Assuming $(1/|j\omega C_f|) \ll R_f$, and $(1/|j\omega C_P|) \ll R_f||(1/g_m)$, the capacitive coupling ratio (A_{CP}) can be determined as

$$A_{\text{CP}} = \frac{v_g}{v_{\text{RF}}} \cong \frac{C_S}{C_S + C_P}. \tag{14}$$

The basic theory of a nonlinear device is analyzed in [53]. In the square-law detection region, the detected low-frequency current Δi is proportional to the microwave power dissipated in the nonlinear device P_D. The ratio $\Delta i/P_D$, which is called current responsivity and denoted by β, determines the dc output voltage to microwave rms voltage detection gain. As shown in [53] and [54], the detection gain is expressed as

$$\beta = \frac{\Delta i}{P_D} = \frac{V_O}{v_{g,\text{rms}}^2} = \frac{i''(v_g)}{2i'(v_g)} = \frac{q}{2nkT} \tag{15}$$



(a) (b) (c)

Fig. 21. (a) Measured rms voltages at various nodes versus PA input power. (b) Measured error of each rms detector compared to an ideal rms detection line. (c) Detection error of V_4 at the 20–34 GHz band versus its measured output voltage.

where n is an ideality factor, V_O is the dc output voltage, and $\upsilon_{g,\mathrm{rms}}$ is rms of υ_g. Also, $i(\upsilon_g)$ represents the drain current, whereas its first and second derivations are proportional to the dc output and rms voltages, respectively [53]. Subsequently, considering the capacitive coupling ratio, the overall detector gain is

$$\frac{V_O}{\upsilon_{\mathrm{RF,rms}}^2} = \beta \times A_{\mathrm{CP}}^2 = \frac{q}{2nkT} \times \left(\frac{C_S}{C_S + C_P}\right)^2. \tag{16}$$

According to (16), the overall gain can be configured by adjusting C_{CPL} to reduce the coupling ratio, as shown in Fig. 19. $C_{\mathrm{CPL}} = 5.6$ fF is chosen for V_4 to reduce its voltage coupling ratio by -3 dB. Moreover, since β depends only on the ideality factor and temperature, the detection gain is independent of bias and geometry. Therefore, the detection gain variation over process that mainly depends on capacitors' mismatches does not impose any sizing constraint on the device.

Fig. 21(a) demonstrates the measured rms voltages at various nodes versus PA input power at 25 GHz. It affirms 6.2 dB passive voltage gain of DA input transformer (1:2 turn ratio) and 6.9 dB DA voltage gain. The measured rms voltages are compared to an ideal rms detection line, and the errors are presented in Fig. 21(b). Since the rms detectors are employed in an energy-efficient PA, the power consumption increases at the higher input power levels. Thus, the chip temperature increases accordingly. The chip temperature is measured using an on-chip sensor, showing only a 3.8° increase during measurement, thanks to the proposed highly efficient PA structure. Note that each input power level is applied for a relatively long time to ensure the chip temperature reaches its steady-state mode during the measurement.

Even though (16) shows detection gain directly depends on temperature, the detection accuracy is mostly limited by the device's dynamic range rather than temperature. For instance, V_4 shows a more significant error than V_3 because it experiences 6.9 dB larger voltages while its coupling factor is only 3 dB less than V_3. Therefore, choosing an appropriate coupling ratio at each stage is essential to keep the detectors' signal levels the same to experience almost the same inaccuracy, thus mitigating their error in calculating the gain. Nevertheless, the interstage gain can be measured at the back-off power levels, where all rms detectors provide significantly high accuracy. Fig. 21(c) exhibits the detection error of V_4 at various frequencies versus its measured output voltage.

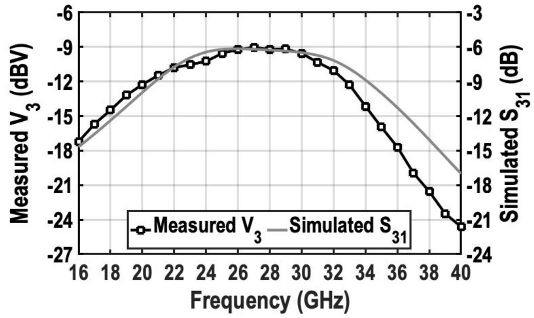


Fig. 22. Measured rms voltage at DA's input while the input power is 0 dBm (left axis) and the 3-D EM simulation results (right axis).

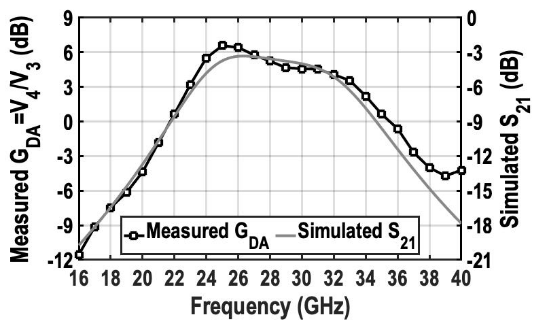


Fig. 23. Measured DA's gain using rms voltages at inputs of DA and PA (left axis) and the 3-D EM simulation results (right axis).

B. Inter-Stage Passive Circuits Evaluation Results

Fig. 22 exhibits the measured rms voltage at the DA input (V_3) while the input power is 0 dBm (left axis). Besides, the S-parameter simulation adopting the order of the ports as mentioned in Fig. 16(c) is plotted (right axis). The simulated 3 dB bandwidth ($\mathrm{BW}_{3\,\mathrm{dB}}$) is 21–34 GHz while it became 20–32.7 GHz on the prototype chip. Furthermore,

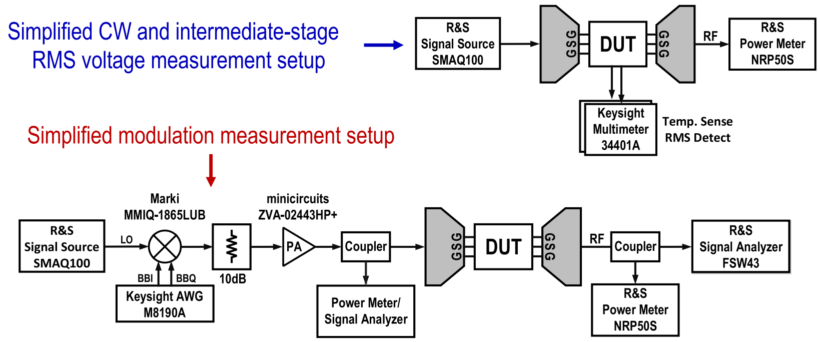


Fig. 24. Simplified CW and modulation measurement setups.

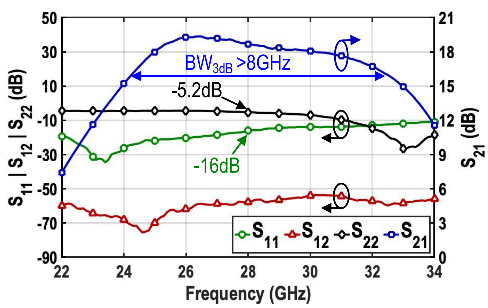


Fig. 25. S-parameter measurement results of the proposed SDPA.

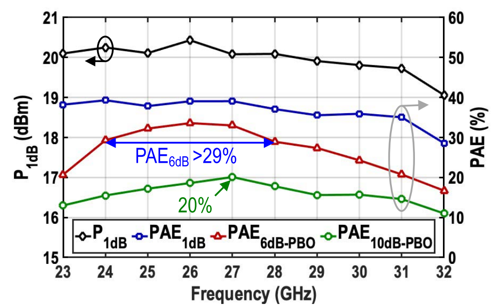


Fig. 27. Measured output power and PAE at 0-/6-/10-dB PBO versus frequency.

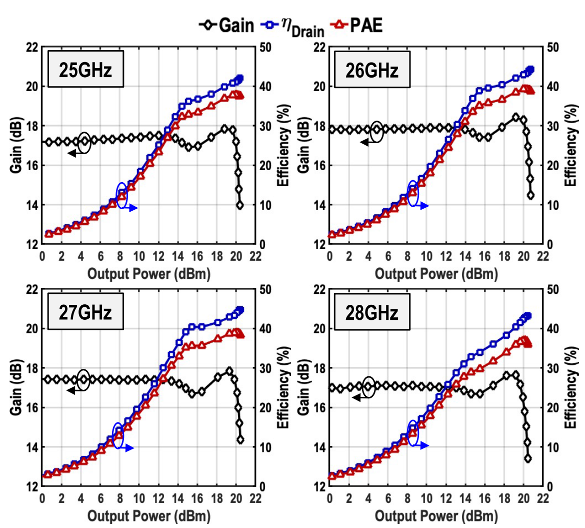


Fig. 26. Measured gain, last-stage drain efficiency, and PAE versus output power at various frequencies.

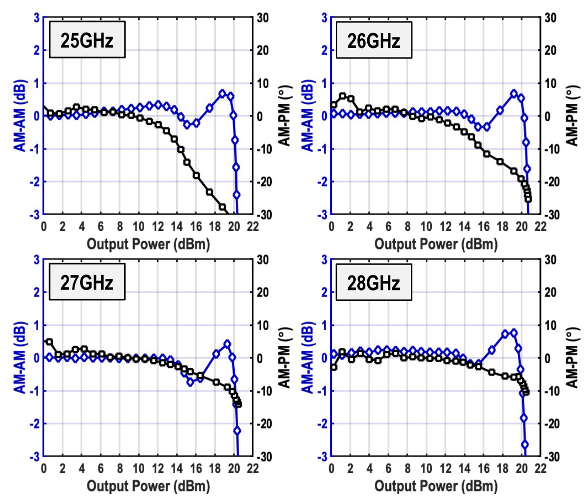


Fig. 28. Measured AM–AM and AM–PM distortion versus output power at various frequencies.

as illustrated in Fig. 23, the DA gain is measured using $G_{\mathrm{DA}} = (V_4/V_3)$ and compared to the corresponding inter-stage matching network's [see Fig. 16(d)] S-parameter simulations. Despite the more in-band ripple mainly exacerbated by DA's active devices, it exhibits an excellent agreement between measurement and simulation. It achieves more than 10 GHz $\mathrm{BW}_{3\,\mathrm{dB}}$ slightly higher than the simulations.

VI. Measurement Results

All measurements are performed using a high-frequency probe station. The dc supplies, bias voltages, and rms detector pads are wire-bonded directly to an FR4 printed circuit board (PCB). In this work, 1.8 V supply voltage is used for the PAs, and 0.9 V for the DAs. Fig. 24 exhibits the continuous wave (CW) and modulated signal measurement setups. The power loss of the probes is obtained from the specific measured S-parameter files provided by the producer. The insertion loss of the cables and the directional couplers are measured and de-embedded.

A. Continuous-Wave Measurement Results

The small-signal S-parameter performance is measured using the Keysight N5227A network analyzer. As Fig. 25

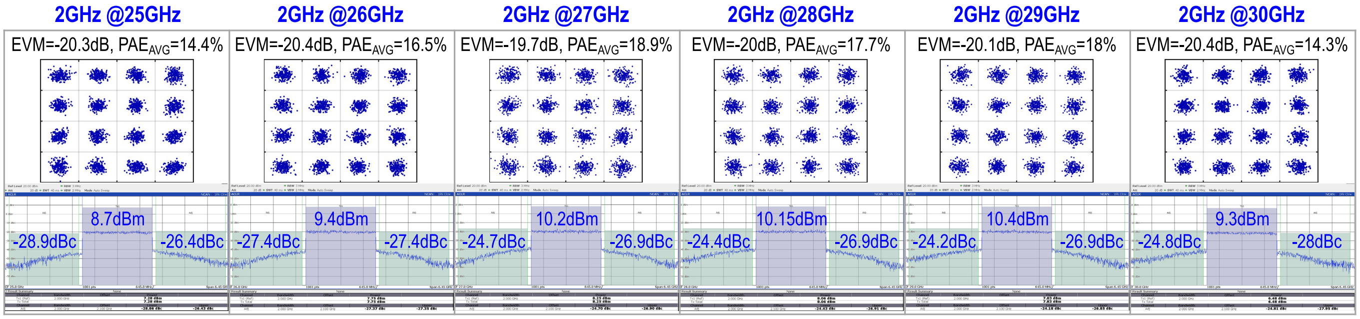


Fig. 29. Measured constellations/spectrums for a “2 GHz 16-QAM OFDM” signal at various frequencies.

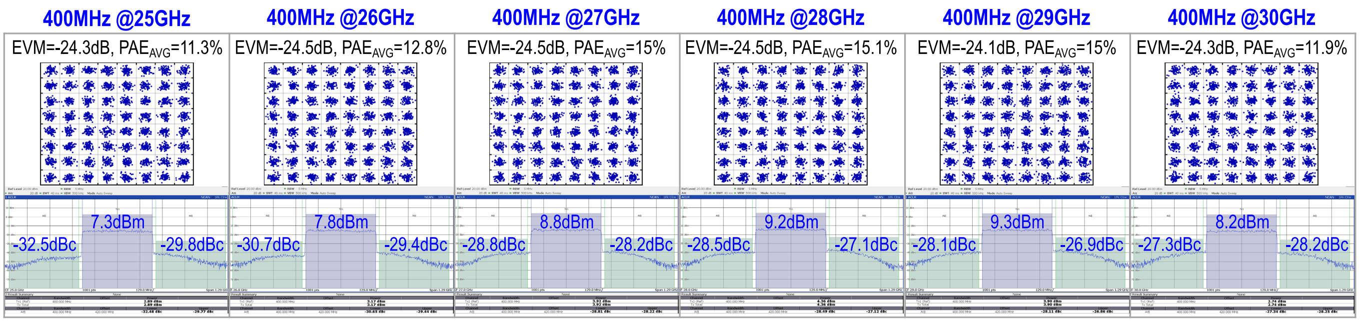


Fig. 30. Measured constellations/spectrums for a “400 MHz 64-QAM OFDM” signal at various frequencies.

demonstrates, the PA achieves more than 8 GHz small-signal $\mathrm{BW}_{3\,\mathrm{dB}}$, where its S_{12} and S_{11} are less than -54 and -12.8 dB, respectively. At 28 GHz, PA's S_{22} is -5.2 dB while its input matching is -16 dB. The PA offers 18.3 dB small-signal gain at 28 GHz.

The large signal CW measurement results are reported in Fig. 26 for various operational frequencies. At 27 GHz, the $P_{1\,dB}$ and P_{SAT} are 20.2 and 20.43 dBm, respectively. Its PAE at $P_{1\,dB}$, 6-dB PBO, and 10-dB PBO are 39.1%, 34%, and 20%, respectively. Moreover, as shown in Fig. 27, the PA provides more than 19 dBm $P_{1\,dB}$ over a 23–32 GHz band (i.e., -1 dB bandwidth). The proposed DPA's 6-dB PBO PAE is >29% over the 24–28 GHz band and >24% over the 23.5–30 GHz band. Besides, a slow amplitude-modulated ramp signal (2 μs) is applied to measure AM–PM distortion, employing the modulation measurement setup shown in Fig. 24. The measured AM–AM/AM–PM distortions are demonstrated in Fig. 28 for various frequencies. Note that the input varactors of the DAs and the PAs (see Fig. 18) are used to minimize AM–PM distortions at each operational frequency.

B. Modulated Signal Measurement Results

The PA dynamic performance is verified by wideband modulated signals such as “16-QAM OFDM” and “64-QAM OFDM” signals. As demonstrated in Fig. 24, the baseband I/Q-modulated signals are generated with an arbitrary waveform generator (Keysight AWG M8190A) and upconverted using a Marki I/Q mixer. A directional coupler is employed at the output to provide the signal for an R&S FSW43 signal analyzer, while an R&S NRP50S measures the output power. Fig. 29 exhibits measured constellations and spectrums of a 2 GHz 16-QAM OFDM signal at 25–30 GHz carrier frequencies. Without using any DPD, the DPA achieves almost -20 dB EVM while the PAPR is 9.5–10 dB. At 27 GHz, the

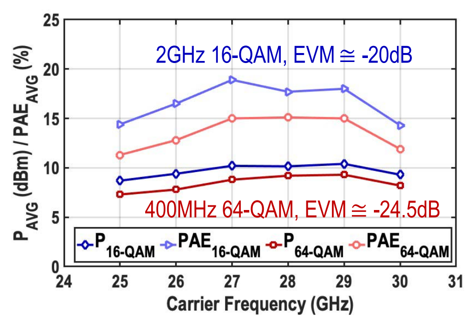


Fig. 31. Measured average output power and PAE of 16-/64-QAM signals with ∼10 dB PAPR at $-20/-24.5$ dB EVM versus carrier frequency.

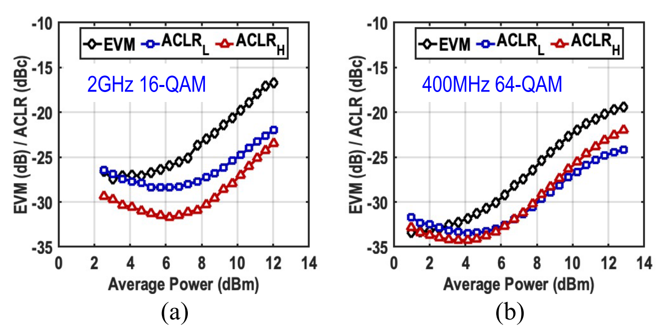


Fig. 32. Measured EVM/ACLRs versus P_{AVG} at 27 GHz for (a) “2 GHz 16-QAM OFDM” signal and (b) “400 MHz 64-QAM OFDM” signal.

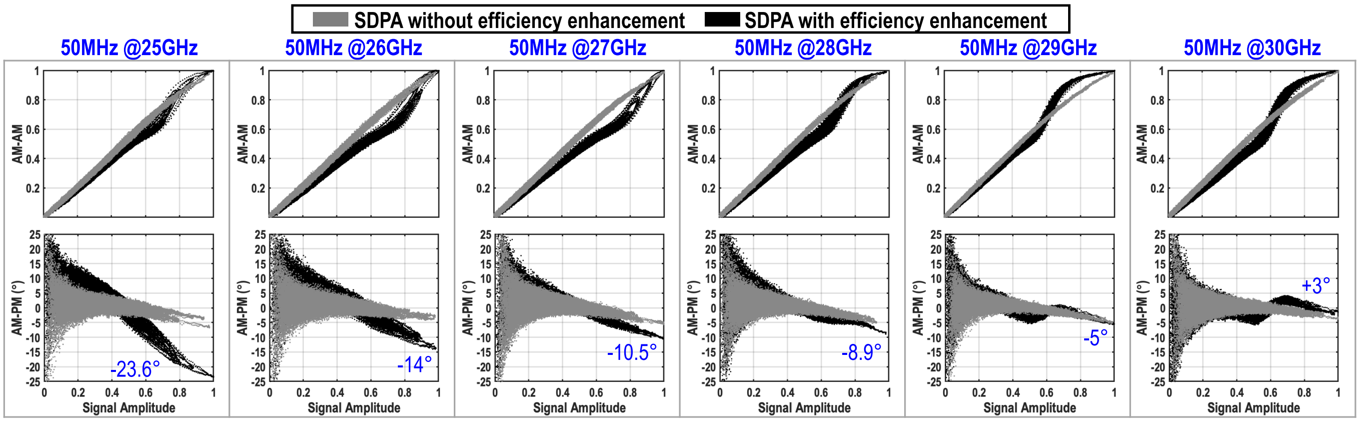


Fig. 33. Measured AM–AM/AM–PM of the proposed SDPA with ($V_{\mathrm{det}} = 0.37$ V) and without ($V_{\mathrm{det}} = 0.9$ V) efficiency enhancement employing "50 MHz 64-QAM OFDM" signals with 10–10.5 dBm P_{AVG} and 8.6–9.4 dB PAPR.

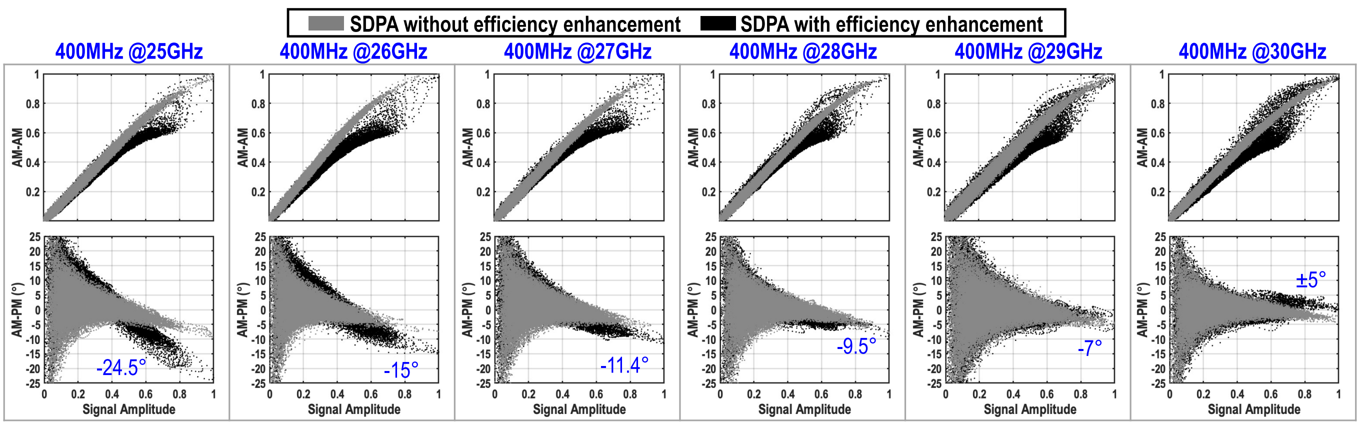


Fig. 34. Measured AM–AM/AM–PM of the proposed SDPA with ($V_{\mathrm{det}} = 0.37$ V) and without ($V_{\mathrm{det}} = 0.9$ V) efficiency enhancement employing "400 MHz 64-QAM OFDM" signals with 10–10.5 dBm P_{AVG} and 9.3–11.1 dB PAPR.

proposed DPA generates 10.2 dBm average power (P_{AVG}) with 18.9% average PAE.

A 64-QAM OFDM signal is utilized to verify the performance of the proposed DPA for the mm-wave 5G system. Fig. 30 shows the measured constellations and spectrums for a 400 MHz signal with 9.3–10.1 dB PAPR. At 27 GHz, with 8.8 dBm P_{AVG} and 15% PAE, PA achieves an EVM of −24.5 dB and an ACLR of −28.8 dBc/−28.2 dBc without DPD. As summarized in Fig. 31, over 25–30 GHz carrier frequencies, the DPA supports a 400 MHz 64-QAM OFDM signal with >7.3 dBm P_{AVG} and >11.3% average PAE. Besides, Fig. 32 demonstrates the measured EVM/ACLRs versus P_{AVG} at 27 GHz.

As discussed in Section II, the load modulation dramatically increases the maximum AM–AM/AM–PM deviations by modulating the Q of the passive network. To support the described analysis, in addition to the AM–AM/AM–PM results illustrated in Fig. 28, the AM–AM/AM–PM of the proposed PA (black) is reported for various frequencies employing a "50 MHz 64-QAM OFDM" signal with 10–10.5 dBm P_{AVG} (Fig. 33). Here, to elaborate more, the measured AM–AM/AM–PM performance of the proposed PA, which reconfigured ($V_{\mathrm{det}} = 0.9$ V, see Fig. 19) to operate without

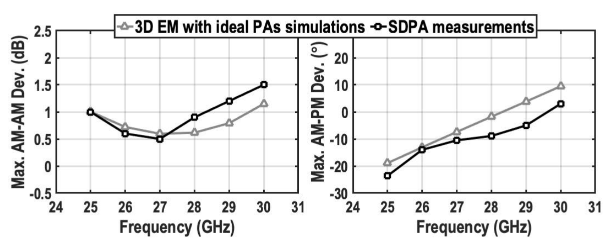


Fig. 35. Measured maximum AM–AM/AM–PM deviations of the realized SDPA compared to its 3-D EM simulations (Fig. 15.)

efficiency enhancement (gray), is presented. In other words, the PA performance is measured when its auxiliary PA is always on, performing as a simple power combining without any load modulation.

As demonstrated in Fig. 33, the AM–PM deviation is as high as 23.6° at 25 GHz, and it decreases while operating at the higher frequencies. On the other hand, the maximum AM–PM deviation of the SDPA without efficiency enhancement is −3° to −5°, and relatively stable over the bandwidth of interest, thus confirming the load modulation impact on the linearity as analyzed earlier.

TABLE II

SILICON-BASED mm-WAVE PAs PERFORMANCE COMPARISON

	Mm-Wave Doherty PAs									Mm-Wave LMBAs		Linear Mm-Wave PAs		
	This work			Wang ISSCC'19 [28]	Hu JSSC'19 [29]	Mannem JSSC'21 [34]	Huang ISSCC'21 [33]	Kim RFIC'21 [31]	Pashaeifar JSSC'21 [40]	Qunaj ISSCC'21 [21]	Chappidi IMS'20 [20]	Vigilante JSSC'18 [48]	Shakib ISSCC'17 [10]	Wang JSSC'21 [14]
Architecture	Two-step impedance inversion series-DPA			Mixed-signal DPA	Multiband DPA	Role-exchange DPA	Continuous Coupler DPA	Parallel-series DPA	Balanced series-DPA	Doherty-Like LMBA	LMBA	Transformer based network	Analog linear PA	Distributed Balun based PA
Technology	40nm CMOS			45nm SOI	130nm SiGe	45nm SOI	45nm SOI	28nm CMOS	40nm CMOS	28nm CMOS	65nm CMOS	28nm CMOS	40nm CMOS	45nm SOI
Supply (V)	1.8 (PA), 0.9 (DA)			2	1.5	2, 1	2, 1	1.8	1	1	1.1	0.9	1.1	2
Freq. (GHz)	24 to 32			27	28 to 42	26 to 60	26 to 60	24 to 30	24 to 30	36	26 to 40	29 to 57	27	25.8 to 43.4
Core area (mm^2)	0.37			0.52	1.76#	0.67	0.62	0.16	1.38	1.44#	1.47#	0.16	0.27	0.21
Gain (dB)	17.4 (27GHz)			19.1	18.2 (28GHz)	16*	15.5*	16.5	N/A	18	12.5*	20.8	22.4	20.5
P_{SAT} (dBm)	20.43			23.3	16.8	22.62 (32GHz)	22	18.8	NR	22.6	20	16.6	15.1	20.4 (28GHz)
P_{1dB} (dBm)	20.2			22.4	15.2	NR	21.5	17.5	20	19.6	NR	13.4	13.7	19.1
PAE_{SAT} (%)	38.2			40.1	20.3	41.9	40.5	30	NR	32	23.3	24.2	33.7	45
PAE_{1dB} (%)	39.1			39.4	19.5	NR	39.9	NR	39.8†	30.5	NR	12.6	NR	42.5
PAE_{6dB} (%)	34			33.1	13.9	31.5	32.8	22	31†	24.2	23.3‡	NR	15.1	
Modulation scheme	16-QAM OFDM	64-QAM OFDM	64-QAM OFDM	SC 64-QAM	SC 64-QAM (28GHz)	1-CC 64-QAM 5G NR FR2	1-CC 64-QAM 5G NR FR2	8-CC 64-QAM OFDM	8-CC 64-QAM OFDM	SC 64-QAM	SC 64-QAM	SC 64-QAM (34GHz)	8-CC 64-QAM OFDM	2-CC 64-QAM 5G NR FR2
Data rate (Gb/s)	2GHz	400MHz	100MHz	6	3	200MHz	200MHz	800MHz	800MHz	12	6	3	800MHz	800MHz
PAPR (dB)	9.6	9.7	8.6	6.5	6	9.64	9.64	10	10.8	≈6	NR	8.3	9.7	11.78
EVM_{rms} (dB)	-19.7	-24.5	-25.1	-25.3	-27**	-24	-25.4	-25	-27.1	-25	-27	-25	-25	-25.1
ACLR (dBc)	-24.7/-26.9	-28.8/-28.2	-36.3/-27.1	-29.6	-28.4	-28.8	-27/-25.8	-25.9	-33.4/-32.1	NR	-29	-30.2	-31/-29	-25.6
P_{avg} (dBm)	10.2	8.8	9.8	15.9	9.2	10.7	9.5	11.4	8.4	16	10.6	8.9	6.7	11.3
PAE_{avg} (%)	18.9	15	17.7	29.1 (27.6††)	18.5†	14.5	15.5	18.1	10.8†	22	12.1†	4.4	11	16.6

Chip area. *Graphically estimated. ‡Last stage drain efficiency at 4dB PBO. †Last stage drain efficiency **EVM normalized to peak signal. ††Efficiency with digital circuits.

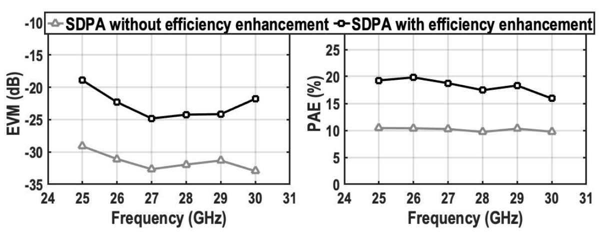


Fig. 36. Measured EVM and average PAE (P_{AVG} = 10–10.5 dBm) of implemented SDPA with and without efficiency enhancement.

Furthermore, the measured AM–AM/AM–PM distortion of a 400 MHz 64-QAM OFDM signal measured at 10–10.5 dBm P_{AVG} at various carrier frequencies is presented in Fig. 34. Due to the memory effect, the measured AM–AM/AM–PM profiles are worse than the 50 MHz 64-QAM OFDM signal. In this regard, the adaptive biasing limited bandwidth poses more time-related errors in the efficiency enhancement mode, leading to a more significant memory effect.

Fig. 35 shows the simulation results of ideal PAs AM–AM/AM–PM deviations using 3-D EM models and compares them to the measured performance. As demonstrated, there is good agreement between simulation and measurement results, proofing that although the load modulation degrades the linearity performance, its behavior is predictable and stable.

Lastly, Fig. 36 depicts the measured EVM and average PAE of a "50 MHz 64-QAM OFDM" signal for the realized SDPA with and without efficiency enhancement. It demonstrates almost $\times 2$ average PAE improvement over the 5G band. This close-to-perfect broadband load modulation is a significant advantage of the proposed SDPA architecture. However, Fig. 36 also shows compromising the in-band linearity due to inherent AM–AM/AM–PM distortions of DPAs.

Table II summarizes the measured performance of the proposed SDPA and compares it to that of prior-art silicon-based mm-wave PAs. The realized SDPA satisfies the 5G requirements by providing >20 dBm P_{SAT} with $>36\%$ PAE_{SAT} over the 24–30 GHz band. It also provides 34% PAE at 6-dB PBO, the highest among mm-wave DPAs. Besides, considering that the Doherty combiners typically occupy a large die area, the realized SDPA is reasonably compact, only larger than [31].

In [33] and [34], impressive broadband DPA architectures are presented, achieving $PAE_{6\,dB}$ as high as 32.8%. However, their excellent performance occurs mostly at 30–38 GHz, operating less efficiently at other prevailing mm-wave 5G bands (e.g., 24–30 GHz and 37–43.5 GHz). For instance, in [34], the $P_{SAT}/PAE_{SAT}/PAE_{6\,dB}$ at 29 and 38 GHz are 21.8 dBm/33.1%/18.6% and 22.6 dBm/30.6%/25.3%, respectively. Meanwhile, our proposed SDPA provides state-of-the-art efficiency enhancement over the 24–30 GHz band (see Fig. 27).

VII. CONCLUSION

This article introduces three significant contributions.

1) A two-step impedance inverting-based series-Doherty combiner is proposed featuring broadband load modulation, compact footprint, and a simple design structure without demanding advanced technology. Additionally, a step-by-step design framework is presented where all design parameters have been derived based on 5G specifications.
2) We reveal the inherent linearity limitation of DPAs, namely AM–AM/AM–PM distortions, caused by Q modulation. We meticulously discussed and exhibited this phenomenon all the way from the basic ideal component modeling and post-layout 3-D EM simulations up to the modulated signal measurements.

3) A PSIV approach is presented to enhance prototype evaluation and address simulation shortcomings. It can also facilitate long-term operation monitoring.

The chip prototype is realized in 40 nm bulk CMOS technology. The proposed SDPA achieves state-of-the-art performance over the 24–30 GHz band. Overall, the experimental results have demonstrated an excellent agreement between our analysis, simulations, and measurement results.

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