Guest Editorial Introduction to the Special Issue on the 2022 IEEE International Solid-State Circuits Conference (ISSCC)

THE International Technical Program Committee (ITPC) of the IEEE International Solid-State Circuits Conference (ISSCC) selects outstanding articles from the papers presented at the conference and invites the authors to submit an extended manuscript to the Special Issue of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC). This November issue contains the selected papers from the Imagers, microelectromechanical systems (MEMS), and Displays (IMMD) and the Technology Directions (TD) sub-committees. Papers from Analog, Data Converters, Power Management, RF, and Wireless subcommittees are included in the December issue. Finally, the January issue will contain papers from Digital Architectures and Systems, Digital Circuits, Machine Learning, Memory, and Wireline subcommittees.

I. IMAGERS, MEDICAL, MEMS, AND DISPLAYS

The IMMD subcommittee selected five outstanding articles from the 22 papers presented at the ISSCC 2022 IMMD sessions. The first group of this Special Issue includes two articles advancing imaging range sensors. The second group includes three articles aimed at body/brain interfaces and ultrasound and beamforming applications.

The National University of Singapore and the University of California Berkeley coauthor the first article. It advances the frame rate of ultrasound imaging systems to address challenges in 3-D depth sensing from unmanned aerial vehicles, also known as drones. This application specific integrated circuit (ASIC) implements fully integrated ultrasound transmitter (TX) and receiver circuits in a compact size. The one-shot TX driver provides more than $2\times$ driving voltage and the chip achieves real-time 3-D image streaming at 24 frames/s. The second article, from Ulsan National Institute of Science and Technology, presents an 80×60 single photon avalanche diode (SPAD) imaging array for flash LiDAR applications under high background light conditions. It uses a novel, iterative, up/down counter approach to minimizing histogramming requirements in the pixel. The pixel-level coincidence detection circuit allows the chip to achieve long-range detection (45 m), with high resolution (100 ps) and fast conversion in outdoor applications.

In the second section, devoted to advancements in medical device circuits, the first article is co-authored by Yonsei and Kangwon National Universities. It is an important design and demonstration of a Body Coupled Communications (BCC) powered implant that addresses the problems created by physical tethers. This four-channel CT-$\Delta\Sigma$M circuit achieves 6.6 μVrms input noise (10 kHz BW), input range of 300 mV, and a dynamic range of 83.3 dB with 8.6 μW power (FoM of 174 dB). The entire functionality of the wireless neural implant is validated through *in-vivo* experiments on rats. The second article, from the Delft University of Technology, presents a highly integrated ultrasound ASIC for 3-D intracardiac echocardiography probes. This work demonstrates a pitch matched (160 μm) transmitter and receiver front end with beam forming for an area-efficient, high-speed (1000 volume/s) imaging. The final article advances the employment of machine learning techniques to improve the effectiveness of closed-loop brain stimulation. EPFL and Cornell university present a high channel count neuromodulation system on a chip (SOC) with on-chip machine learning for accurate disease state detection. The chip is verified in *in-vivo* neural recording and rest-state tremor in Parkinson's diseases in humans.

II. TECHNOLOGY DIRECTIONS

Among the five outstanding articles selected by the TD subcommittee, the first two articles propose cryo-CMOS ICs for interfacing cryogenic quantum processors, as required to relax the interconnect bottleneck between the cryogenic qubits and the room-temperature control electronics. The following two articles push the boundary for ultra-low-power voice-activated wake-up detectors for IoT nodes by exploring AI edge-computation techniques based on time-domain and analog processing. Finally, the last article demonstrates advances in the number of electrodes and noise performance for electrocorticography brain implant systems.

The first article by IBM reports a cryo-CMOS microwave driver for superconducting qubits. As the target quantum-computing system does not allow time/frequency multiplexing, the circuit is optimized for minimum power consumption while still enabling arbitrary waveform generation to ensure flexibility and output spectral purity. A general-purpose digital processor supporting waveform generation and optimized for low power consumption is co-integrated with an I/Q 10-bit 1-GSa/s current-steering digital to analog converter (DAC) and an I/Q RF 4.5–5.5-GHz up-converter. Dissipating 23 mW when operating at an ambient temperature of 3.5–5 K, the proposed 14-nm cryo-CMOS controller is shown to drive a transmon qubit without limiting the qubit inherent performance.

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The second article by POSTECH also describes a cryo-CMOS IC for controlling superconducting qubits. The flexibility in the microwave qubit driver is traded off for power consumption, resulting in 12-mW power consumption at an operating temperature of 3.5 K over an output frequency from 4.6 to 8.1 GHz. In addition to four such microwave drivers, the proposed 40-nm CMOS controller co-integrates $2\times$ 20-mW I/Q receiver chains for qubit readout and two phase-locked loops (PLLs) intended for generating multiple carriers to target potential groups of qubits across the spectrum.

The third article from the University of Macau proposes a voice activity detector (VAD) composed of a time-domain feature extractor followed by a binary neural network (BNN) classifier. The 1-bit features are directly extracted from the audio samples by an analog switched-capacitor convolutional neural network (CNN). The computation and gain quantization in the CNN are optimized by exploiting the switched-capacitor nature of the circuit both to reduce area and power and to relax the constraints on the quantizer producing the 1-bit input to the BNN. The resulting 28-nm CMOS chip only occupies 0.8 mm^2 and dissipates 108 nW while ensuring $>90\%$ accuracy with 50-ms latency.

The fourth article from the University of Zürich, ETH Zürich, and KAIST demonstrates a keyword-spotting chip comprising an analog feature extractor and a digital recurrent-neural-network (RNN) classifier. The microphone input is converted into a PWM-modulated signal by a VCO-based voltage-to-time converter and successively processed by a time-domain processing circuit including a bank of ring-oscillator-based band-pass filters. The aim is to exploit time-domain processing to better benefit from technology scaling with respect to more traditional voltage-domain solutions. The proposed 65-nm CMOS keyword-spotting circuit achieves $>86\%$ accuracy with 12 ms latency, a die area of 2 mm^2, and a power dissipation of 23 μW.

The fifth article by IMEC and KU Leuven shows a μECoG brain implant system comprising a flexible actively-multiplexed μECoG array and an incremental-$\Delta\Sigma$ FDSOI CMOS readout. The feedback in the $\Delta\Sigma$ modulator is provided with a bulk-DAC via the bulk of the input transistors to improve the area and power efficiency. By adopting a thin-film technology for the electrode array and optimally partitioning the system between the array and the CMOS readout, the system can acquire signals from 256 electrodes with competitive noise performance, as demonstrated by the electrical and *in-vivo* measurements.

The Guest Editors would like to thank all the authors and anonymous reviewers for contributing and ensuring high-quality manuscripts under a tight schedule. We would also like to thank all the members of the IMMD and TD international technical program sub-committees (ITPCs), the ISSCC session chairs, Pavan Hanumolu, the former JSSC Editor-in-Chief, Dennis Sylvester, the current Editor-in-Chief, Danielle Marinese, and the JSSC staff for assistance and guidance.

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She has been with MIT Lincoln Laboratory, Lexington, MA, USA, since 1996, where she is currently a Senior Member of the Technical Staff with the Space Systems and Technology Division. She did pathfinding work in the development of low-power, scientific-grade CCD, CMOS, and photon-counting image sensors, including the design, fabrication, and characterization of several generations of stacked image sensors. Her publications include the first 3-D-per-pixel interconnected and megapixel-scale CMOS image sensor. Her recent work focuses on the development and application of custom electro-optics systems to problems in remote sensing and astronomy, including over 20 fielded systems. Among her accomplishments is the development of the large-area (17.3 cm^2), deep depletion (100-μm-thick silicon) devices for NASA's Transiting Exoplanet Science Satellite, which has discovered over 5800 candidates and 233 confirmed exoplanets to date.

Dr. Suntharalingam has served on the technical organizing committee for over two dozen international conferences and workshops, including the IEEE Solid State Circuits Conference, the IEEE International Electron Devices Meeting, and the IEEE International SOI Conference. She is currently the Vice Chair of the Department of the Air Force Scientific Advisory Board and has served in leadership position for the Stanford National Accelerator Laboratory (SLAC) Linac Coherent Light Source Detector Advisory Committee. She was a recipient of a NASA Silver Achievement Medal, an Asteroid Designation (#454505), an MIT Lincoln Laboratory Technical Excellence Award, and an MIT Excellence Award, among other honors.

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Dr. Sebastiano was co-recipient of the 2008 ISCAS Best Student Paper Award, the 2017 DATE Best IP Award, the ISSCC 2020 Jan van Vessem Award for the Outstanding European Paper, and the 2022 CICC Best Paper Award. He was a Distinguished Lecturer of the IEEE Solid-State Circuit Society. He is on the Technical Program Committee of the ISSCC, the RFIC Symposium, and the IMS. He is currently an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.