A Time-Mode-Modulation Digital Quadrature Power Amplifier Based on 1-bit Delta–Sigma Modulator and Hybrid FIR Filter

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***Abstract*— This article proposes a time-mode-modulation (TMM) digital quadrature power amplifier (PA), which can realize high power efficiency at power back-off (PBO) by applying the 1-bit delta–sigma modulator (DSM) and hybrid finite impulse response (FIR) filter. The 1-bit DSM and digital mixer encode the multi-bit baseband I/Q input signal into a 1-bit signal for on/off controlling the 1-bit PA to realize the TMM operation. Capacitor arrays are not required in the proposed PA, and redundant power dissipation on charging the capacitor array in conventional switched capacitor PAs (SCPAs) is avoided. Furthermore, a hybrid FIR filter comprising a two-tap digital FIR filter and a two-tap transformer (XFMR) combined semi-digital FIR filter suppresses the DSM quantization noise (QN) to avoid efficiency degradation. The XFMR combined semi-digital FIR filter is insensitive to mismatches, which maintains the high linearity of the 1-bit TMM PA. The proposed TMM PA is fabricated in 65-nm CMOS. Without digital pre-distortion (DPD), it achieves 26.4% power-added efficiency (PAE) with 40-MSymbol/s 64-quadrature amplitude modulation (QAM) signal and 20.9% PAE with 20-MSymbol/s 256-QAM signal at 2.6 GHz.**

***Index Terms*— Delta–sigma modulator (DSM), finite impulse response (FIR) filter, power amplifier (PA), quadrature, transformer.**

I. Introduction

SPECTRAL efficiency is crucial in modern wireless communication standards to satisfy the ever-increasing demand for higher data throughput with highly congested spectrum resources. Information-dense higher order quadrature amplitude modulation (QAM), such as 256 QAM [1], is widely used to improve spectrum efficiency. However, high-order modulation schemes often produce an output signal with a high peak-to-average power ratio (PAPR). This causes the power amplifier (PA) to work at power back-off (PBO). Nevertheless, the power efficiency of PA at the PBO region is usually low. Therefore, as the most power-hungry building block in a wireless transceiver, the PBO power efficiency of the PA must be improved to enhance the system efficiency and extend the battery lifetime of handheld devices. Moreover, the linearity of the PA is also important, since a very low error vector magnitude (EVM) is required to demodulate the high-order QAM signal.

With the scaling down of the CMOS process and the decreasing breakdown voltage, the linear PA will work in a smaller quiescent current, and the efficiency is limited. Moreover, the linearity also degrades with the limited voltage headroom. On the contrary, digital switching type PAs, such as Class-D and Class-E, can benefit from the scaling down of CMOS and achieve higher switching speed and lower loss. Therefore, digital PAs are widely used to implement RF transmitters (TXs) [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12].

Several TX architectures adopting digital PAs are investigated, such as envelope elimination and restoration (EER) [13], polar modulation [8], [9], [10], [11], [12], [14], out phasing [15], and RF pulsewidth modulation [16]. However, converting the input signal from the Cartesian domain (I and Q inputs) to a polar coordinate system (amplitude and phase) is required in these structures. Such conversion substantially extends the bandwidth of the output amplitude and phase signal, and a wide-bandwidth phase modulator is inevitable in digital polar TXs, which introduces additional non-linearity and power consumption. On the other hand, digital quadrature TXs [6], [7], [17], [18] do not suffer from the bandwidth extension and offer a simple structure without a complex phase modulator, which is a good candidate for achieving high system efficiency.

Nevertheless, the widely used switched capacitor PA (SCPA) shows degraded PBO efficiency. A capacitor-based voltage divider (Fig. 1) in SCPA precisely controls the output

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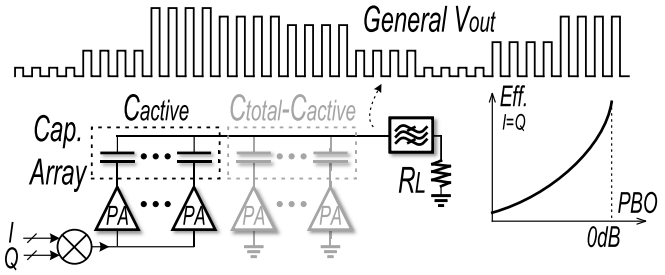


Fig. 1. Block diagram of a conventional SCPA.

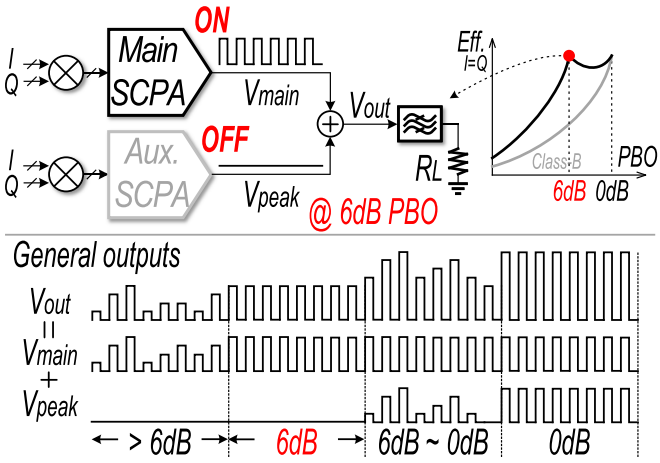
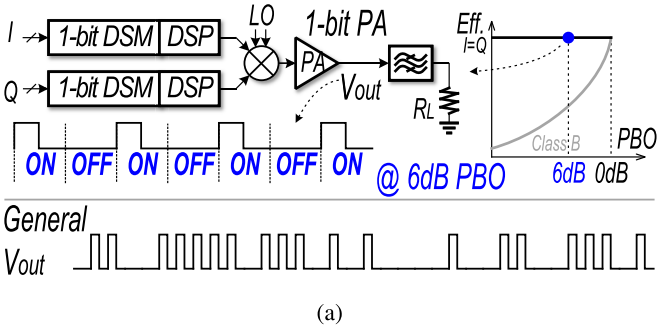
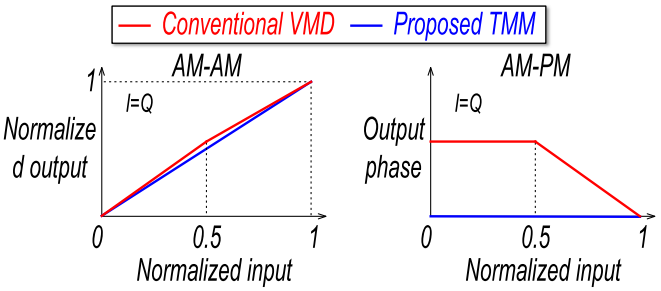


Fig. 2. Block diagram of a conventional VMD SCPA.



(a)



(b)

Fig. 3. (a) Block diagram of the proposed TMM PA with 1-bit output. (b) Conceptual non-linearity comparison with conventional VMD PA.

amplitude by changing the ratio of the active and total capacitance. However, redundant charge/discharge of the capacitor array introduces power loss, which causes rapid efficiency degradation at PBO [19].

Several techniques have been proposed to enhance the PBO efficiency of SCPA. In Class-G SCPAs [20], an additional supply rail is added to create an efficiency peak at 6-dB PBO, at the cost of additional power management hardware. In sub-harmonic switching (SHS) SCPAs [21], [22], PA switches at one-third of the carrier frequency to add an efficiency peak of 9.5-dB PBO. However, SHS SCPA requires harmonic traps in the matching networks, which suffer from area penalty.

Voltage-mode Doherty (VMD) [23], [24] is another method to improve the PBO efficiency of SCPA. As shown in Fig. 2, VMD SCPA comprises two identical SCPAs, the main PA and the auxiliary PA. At 0-dB PBO, both PAs work at their peak outputs. At 6-dB PBO, the auxiliary PA is turned off, while the main PA works at its peak output, generating an output voltage equal to half of the peak output voltage. Therefore, the capacitor array is not required at 6-dB PBO, and the efficiency at 6-dB PBO is equal to the peak efficiency. VMD PA can only achieve operation without capacitor array at 0/6-dB PBO. Switched capacitor operation is still required at other PBO levels to cover the full amplitude range. Therefore, efficiency at other PBO levels is low due to the capacitor array loss.

Unlike the VMD PA, which implements on/off control of the PA in the voltage domain, in this article, we propose a time-mode-modulation (TMM) PA that realizes the on/off PA control in the time domain [25], as shown in Fig. 3(a). At 6-dB PBO, the TMM PA is turned on for one carrier cycle and turned off for the next cycle. In this way, the average fundamental output voltage will be half the peak output voltage, which is 6-dB PBO. Since TMM PA does not need a capacitor array at 6-dB PBO, there is no capacitor array loss, and its efficiency at 6-dB PBO is expected to be the peak efficiency. To extend the TMM operation to PBO levels other than 0/6 dB without using a switched capacitor array, 1-bit delta–sigma modulators (DSMs) and digital signal processing (DSP) are utilized. The DSMs upsample the multi-bit I/Q inputs and convert them to 1 bit. Next, the DSP and the mixer encode the DSM outputs into a 1-bit PA input signal. The 1-bit PA input signal controls the on/off of the 1-bit digital PA for TMM operation. As a result, the amplitude information is encoded into the density of the output pulses. In the general output voltage depicted in Fig. 3(a), more pulses represent higher output power, and fewer pulses represent lower output power. Therefore, the capacitor array is completely eliminated to realize modulation, and the efficiency is expected to be the peak efficiency at any PBO levels (suppose the ideal PA cell and capacitor array loss is the only source of power loss).

Moreover, VMD SCPA suffers from non-linearities caused by the mismatches between the main and auxiliary SCPAs. For example, the gain and delay mismatches between the two sub-PAs introduce AM–AM and AM–PM distortion, respectively [Fig. 3(b)]. In quadrature digital PAs, extremely complex 2-D digital pre-distortion (DPD) must be applied to linearize the PA [26], [27], which introduces additional power consumption and hardware overhead at the system level. On the contrary, in the proposed TMM PA, only one PA cell is used, and the output is a two-level signal. Therefore, the

proposed TMM is intrinsically linear, and power-consuming DPD can be avoided.

This article is organized as follows. Section II introduces the operation principle of prior arts. Section III introduces the proposed TMM PA with a hybrid finite impulse response (FIR) filter. Section IV analyzes circuit non-ideal factors. Section V introduces the system implementation. Measurement results are provided in Section VI, and Section VII concludes this article.

II. Operation Principle of Prior Arts

The most important step in realizing the TMM is to encode the multi-bit I and Q inputs into 1 bit. Several DSM-based TX architectures have been investigated. In the digital TX based on 1-bit bandpass (BP) DSM [29], direct conversion is realized in the digital domain. The local oscillator (LO) signal upconverts the baseband I/Q signal to yield the digital modulated signal at the carrier frequency. The 1-bit BP-DSM converts the modulated signal into 1 bit, and the noise shaping suppresses the quantization noise (QN) in the signal band. A digital clock at least twice the carrier frequency is required to ensure the carrier is within the Nyquist bandwidth. Therefore, the digital logic and the 1-bit digital PA are switching at a high-speed clock, which is extremely power-consuming. Nevertheless, modern wireless communications are conducted at GHz carriers. Therefore, multi-GHz DSP is necessary to implement this structure, which is difficult using the CMOS process. For example, to support communication at 3.5-GHz carrier, Maehata et al. [30] adopt an extremely high clock frequency of 10 GHz.

Unlike the 1-bit BP-DSM-based TX, the TX based on 1-bit low-pass (LP)-DSM is depicted in Fig. 4(a) [28], which relaxes the clock requirements. Since BP-DSM is not the target of this article, in the following context, DSM refers to LP-DSM unless otherwise mentioned. In Fig. 4(a), the DSMs clocked at the carrier frequency f_c convert the I and Q inputs into 1 bit. The 1-bit DSM outputs DSM_i and DSM_q toggles between ± 1. When the I or Q input to the DSM is positive, DSM outputs more $+1$ than -1 s, and vice versa. When the input is near zero, the DSM outputs an equal number of $+1$ and -1 s. Fig. 4(a) (top left) shows the example of DSM waveforms.

Next, the digital mixer upconverts the DSM outputs into 1-bit PA input at the RF frequency. Since the output of each DSM can only be either $+1$ or -1, the mixer will only have four different input combinations, namely, $[+1, +1]$, $[-1, +1]$, $[-1, -1]$, $[-1, +1]$. According to the specific input combination, the mixer selects a 1-bit signal with one of four different phases (45°, 135°, 225°, 315°) as the output, as shown in Fig. 4(b). The 1-bit mixer output then drives the 1-bit PA. The two-level PA output voltage is shown in Fig. 4(a) (top right).

Although conventional 1-bit DSM-based TX can encode multi-bit I and Q inputs into 1-bit PA output, the DSM introduces large QN when converting the multi-bit input into 1 bit. Fortunately, the DSM has a high sampling rate and a high-pass noise transfer function (NTF), which can suppress the QN at the signal band around dc [Fig. 4(a) (bottom left)], and ensures a decent signal-to-noise ratio (SNR). Nevertheless,

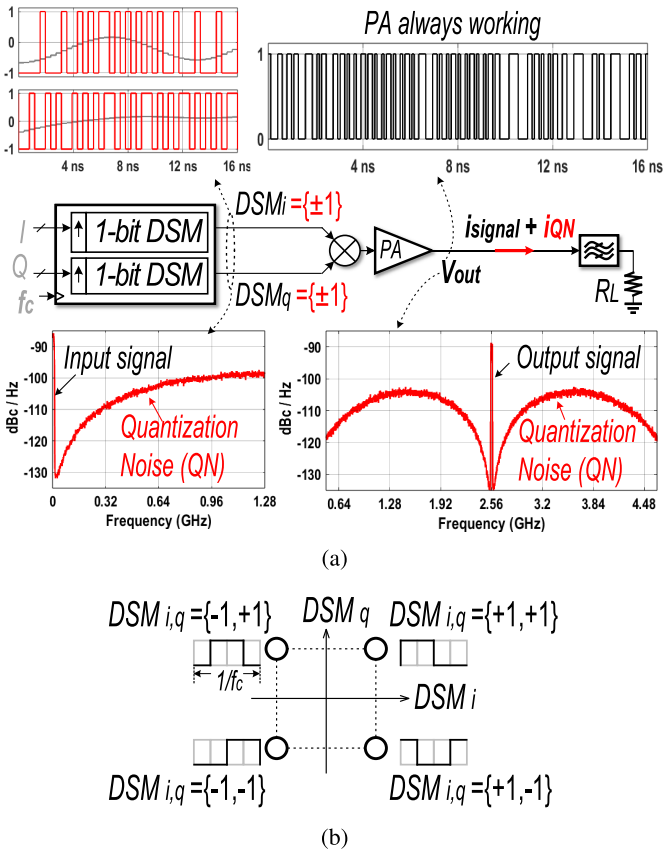


Fig. 4. (a) Block diagram, waveform, and spectra of conventional 1-bit DSM-based TX [28]. (b) Output waveforms of the mixer.

the QN is pushed to high frequencies by the NTF. After the mixer upconverts the DSM outputs to the carrier frequency, the modulation signal and the QN are both converted to the carrier frequency. The QN near the carrier frequency f_c is low, while the QN at other frequencies is high, as shown in the output voltage spectrum in Fig. 4(a) (bottom right).

Besides the modulation signal, the QN in the output voltage V_{out} will also stimulate a current (i_{QN}) in the load, which draws current from the supply and increases power consumption. Therefore, the ideal PA power efficiency can be given by (assume ideal PA and QN are the only source of power loss)

$$\eta_{\mathrm{ideal}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{QN}}} \tag{1}$$

where P_{out} and P_{QN} are the power of the modulated signal and QN, respectively.

Equation (1) indicates that the DSM QN will severely degrade the power efficiency. To make matters worse, the DSM output cannot be 0 in this architecture. Thus, the PA is always working and cannot be turned off for TMM operation to save power.

III. Proposed TMM PA With Transformer Combined FIR Filter

According to the analysis of Section II, we should have two design targets: suppress the DSM QN and realize the TMM operation by turning off the PA. In the proposed architecture shown in Fig. 5, a hybrid FIR filter is proposed to achieve both targets simultaneously.

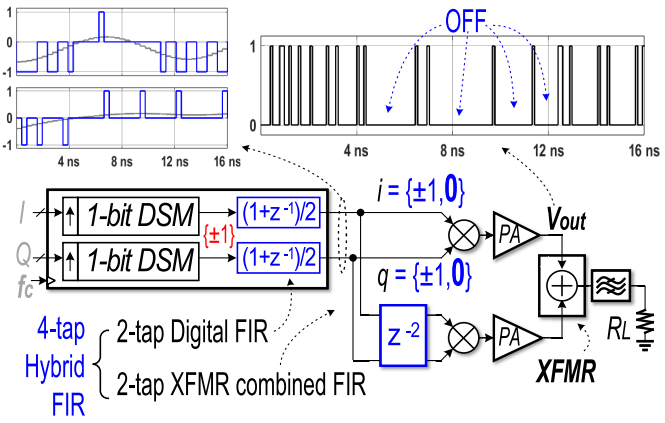


Fig. 5. Block diagram and waveform of the proposed TMM PA with hybrid FIR filter.

A. Achieving TMM Operation

As shown in Fig. 5, the applied four-tap hybrid FIR filter comprises two parts: the two-tap digital FIR filter after the DSM and the following two-tap transformer combined semi-digital FIR filter. Since the DSM output can be $+1$ or -1, the output becomes $\pm 1, 0$ after passing through the digital FIR filter, as shown in Fig. 5 (top left). Unlike the conventional 1-bit DSM-based quadrature PA, in the proposed PA, the mixer input can be 0. This is crucial because the 0 can turn off the PA for TMM operation.

On the other hand, the i and q outputs of the digital FIR filter are 2-bit signals (one sign bit); each has three different states. Therefore, the mixer will have nine different input combinations. The conventional mixer shown in Fig. 4(a) cannot be utilized. The digital mixers widely used in the switched-capacitor-based digital TXs [31], [32] can achieve the upconversion of the 2-bit input, as shown in Fig. 6(a). In the conventional mixer mapping schemes, 50% duty cycle signals with four different phases ($45°, 135°, 225°, 315°$) represent the four states (states 1, 3, 7, and 9) of which $i \neq 0$ AND $q \neq 0$. Three-level signals with four different phases ($0°, 90°, 180°, 270°$) represent the four states (2, 4, 6, and 8) of which $i \neq 0$ OR $q \neq 0$. Furthermore, in the remaining OFF state when $i = q = 0$, the mixer output is 0 (state 5). Although this mixer can achieve upconversion, the three-level output requires a 2-bit PA, which may cause non-linearity and degrade the EVM.

To encode the 2-bit DSM outputs into two-level PA output, the mixer mapping scheme shown in Fig. 6(b) is proposed. Note that when $i \neq 0$ AND $q \neq 0$ (states 1, 3, 7, and 9), the output of the proposed mixer is 50% duty cycle two-level signal with four different phases, which is the same as the outputs of the conventional mixer. However, when $i \neq 0$ OR $q \neq 0$ (states 2, 4, 6, and 8), outputs of the proposed mixer are two-level 25% duty cycle signals with four different phases. In the remaining OFF state when $i = q = 0$, the mixer output is 0 (state 5) to turn off the PA for TMM operation. Fig. 5 (top right) shows the output waveform of the proposed PA. The PA output is an intrinsically linear two-level signal, and the PA can be turned off to realize the proposed TMM operation.

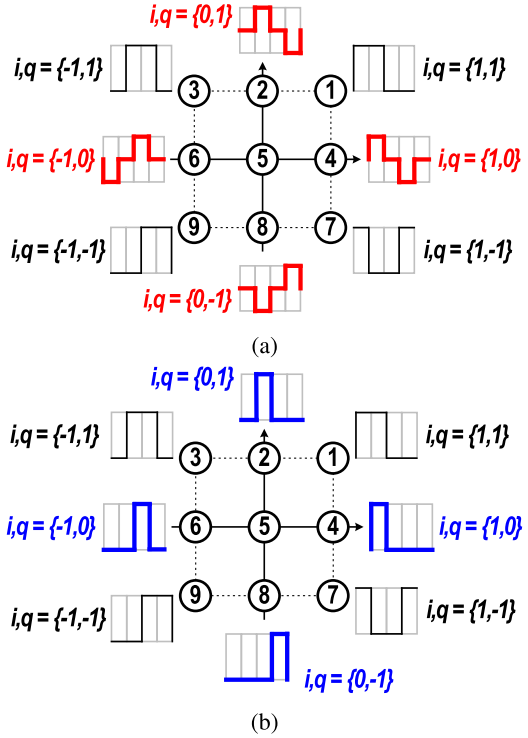


Fig. 6. Output voltages of (a) conventional digital mixer for digital quadrature PAs [31], [32] and (b) the proposed mixer.

B. DSM QN Suppression Using Hybrid FIR Filter

In the proposed PA architecture shown in Fig. 5, the digital FIR filter outputs i/q are upconverted by the proposed mixer and drive one sub-PA. i/q are delayed by two carrier cycles, then upconverted, and drive another sub-PA. The two sub-PA outputs are combined through a transformer (XFMR). Since the digital i/q signal is delayed in the digital domain and combined in the analog domain, this forms a two-tap XFMR combined semi-digital FIR filter. Unlike [32], which adopts a switched capacitor array to combine the semi-digital FIR filter outputs and results in large power loss, we choose the XFMR to combine the FIR outputs that avoid the capacitor array loss for high power efficiency. Considering the two-tap digital FIR filter and the two-tap XFMR combined FIR filter, we can derive that the output voltage of the proposed PA should be

$$V_{\text{out}} = \text{DSM}_{i/q} \times \frac{1}{2}\left(1 + z^{-1} + z^{-2} + z^{-3}\right) \times \text{LO}_{i/q}. \quad (2)$$

Therefore, a four-tap FIR response is implemented in the proposed PA with a two-feed XFMR.

Fig. 7 shows the simulated output spectrum and ideal efficiency [see (1)] of the proposed TMM PA with and without the four-tap hybrid FIR filter (without the FIR filter, it will become a conventional 1-bit DSM-based digital quadrature PA discussed in Section III). In the simulation, 20-MSymbol/s 64-QAM signal is adopted as the input, and the first-order DSMs clocked at $f_c = 2.6$ GHz convert the input into 1 bit. Since the on-chip matching network usually has a BP filter characteristic that can suppress some of the DSM QN, a BP filter with a Q value of 2 is added at the PA output for a more accurate simulation of the QN power.

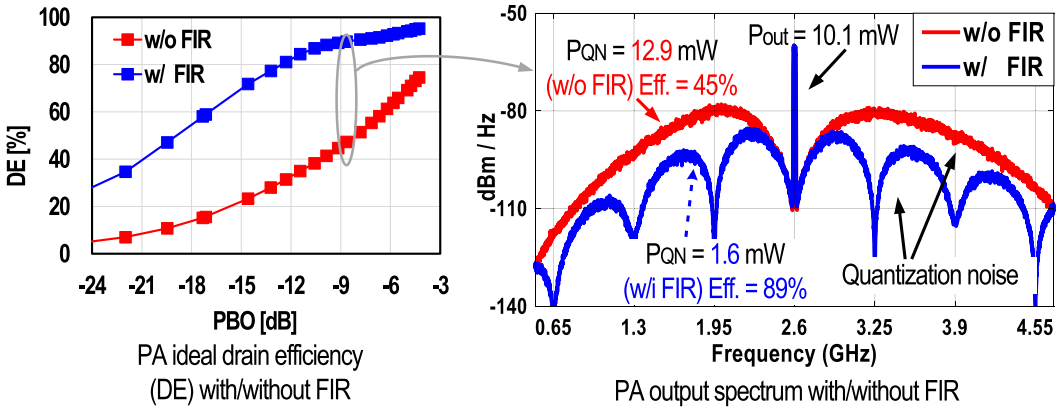


Fig. 7. [Rev. 1.1] [Rev. 2.8] Simulation results of the proposed TMM PA with and without the proposed FIR filter.

It can be seen from Fig. 7 that the proposed hybrid FIR filter significantly reduces the DSM QN power in the proposed PA. The associated ideal efficiency is improved compared with the case without FIR. At around 9-dB PBO, the output power is 10.1 mW, while the QN power with and without the FIR filter is 1.6 and 12.9 mW, respectively. The FIR filter contributes to around 8× QN power suppression. The ideal efficiency at this point improves from only 45% to 88%. However, increasing the number of FIR taps will further increase the QN suppression and improve efficiency. Nevertheless, combining more FIR taps requires either a more complex transformer that introduces significant area overhead or a multi-bit PA that suffers from low PBO efficiency.

IV. Circuits Non-Idealities

For further analysis, the non-ideal factors of the circuits should be considered.

A. PA With Non-Ideal Components

In the proposed structure, a 1-bit PA is adopted. A Class-D PA is chosen over Class-E PA, because Class-D PA requires fewer passive components and is, thus, more area-efficient. Although the theoretical efficiency of a Class-D PA is 100%, however, several non-ideal effects must be considered when implementing the PA, including conduction loss, switching loss, and passive loss [19], [24], [26]. Suppose R_{ON} is the switch-ON resistance of the PA, and conduction loss is the power dissipated in R_{ON}. C_{par} is the parasitic drain capacitance, which is charged at every rising edge of the PA output and causes switching loss. The passive matching network of the PA also attenuates the output power by a factor of α, which is passive loss. Note that R_{ON} decreases and C_{par} increases when the transistor size increases. The product of $R_{\mathrm{ON}}C_{\mathrm{par}}$ is a constant, and we can define the totem pole driver figure of merit $f_{\mathrm{SW}} = 1/(2\pi R_{\mathrm{ON}}C_{\mathrm{par}})$ [23]. Advanced process and good layout can improve f_{SW}.

The drain efficiency (DE) of the proposed TMM PA and the conventional VMD PA at different phases, including QN and all aforementioned non-ideal factors, is simulated and plotted versus PBO levels in Fig. 8. Fig. 8(a) and (b) shows the simulated results at 45° ($I = Q$) and 0° ($I = 0$), respectively.

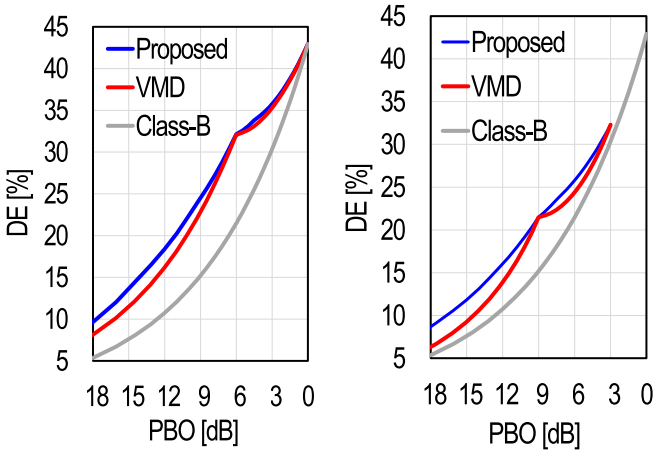


Fig. 8. Simulated efficiency of the proposed TMM PA and conventional VMD PA at different angles. Simulation including QN and non-ideal circuits (load $R_L = 5\ \Omega$, $R_{\mathrm{ON}}/R_L = 1/5$, $f_{\mathrm{SW}} = 25$ GHz, $\alpha = 0.7$, and quality factor of the load $Q_{\mathrm{loaded}} = 2$). (a) $I = Q$, 45°. (b) $I = 0$, 0°.

Here, we can see that the DE of the proposed PA outperformed the conventional VMD PA at different angles ($I = Q$ and $I = 0$). The efficiency is significantly improved compared with normalized Class-B PA.

B. Gain and Delay Mismatches Between the Two Sub-PAs

The proposed PA uses two sub-PA cells to construct the XFMR combined FIR filter. The effect of mismatches between the two sub-PAs should be analyzed. Fig. 9(a) shows the simplified mismatch model of a VMD PA when $0.5 < \mathrm{AM} < 1$, where AM is the normalized amplitude control code. The main PA is working at its peak (normalized amplitude 0.5), and its output suffers from a gain mismatch of Δ. The peak PA output suffers from a phase shift of ϕ caused by the delay mismatch between the two sub-PAs. Therefore, according to the phasor addition theory, suppose ϕ is small and $\cos\phi \approx 1$, $\sin\phi \approx \phi$, the output voltage of VMD PA is

$$V_{\mathrm{VMD}} = (\mathrm{AM} + 0.5\Delta) \times \sin(\omega t + \theta) \tag{3}$$

$$\theta = \arctan\frac{\mathrm{AM} - 0.5}{\mathrm{AM} + \Delta}\phi. \tag{4}$$

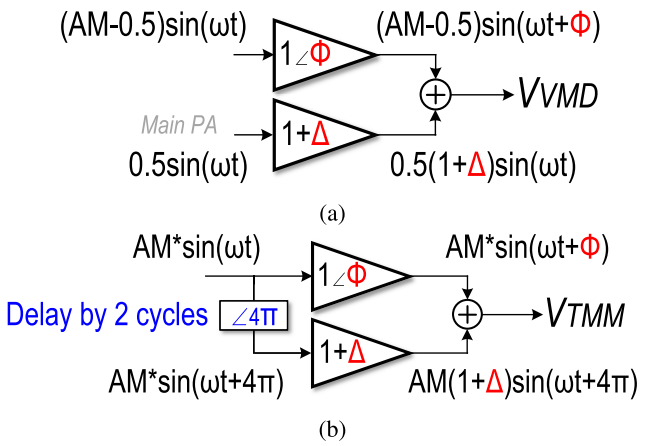


Fig. 9. Simplified mismatch model for (a) VMD PA and (b) proposed TMM PA with XFMR combined FIR filter.

Considering the situation of AM $<$ 0.5, when peak PA is off, and only the main PA is working, the output gain (G_{VMD}) and phase ($\mathrm{Ph}_{\mathrm{VMD}}$) of VMD PA are given by

$$G_{\mathrm{VMD}} = \begin{cases} 1, & 0 < \mathrm{AM} < 0.5 \\ 1 + 0.5\Delta/\mathrm{AM}, & 0.5 < \mathrm{AM} < 1 \end{cases} \tag{5}$$

$$\mathrm{Ph}_{\mathrm{VMD}} = \begin{cases} \phi, & 0 < \mathrm{AM} < 0.5 \\ \arctan\dfrac{\mathrm{AM} - 0.5}{\mathrm{AM} + 0.5\Delta}\phi, & 0.5 < \mathrm{AM} < 1. \end{cases} \tag{6}$$

Similarly, Fig. 9(b) shows the mismatch model for TMM PA with XFMR combined FIR filter. The output of the two sub-PAs has a delay of two cycles, translating into a phase shift of 4π. Similarly, the output gain (G_{TMM}) and phase ($\mathrm{Ph}_{\mathrm{TMM}}$) of the proposed PA are given by

$$G_{\mathrm{TMM}} = 1 + 0.5\Delta \tag{7}$$

$$\mathrm{Ph}_{\mathrm{TMM}} = \arctan\frac{1}{2 + \Delta}\phi. \tag{8}$$

It can be concluded from the above equations that the mismatches lead to AM-dependent gain and phase in the conventional VMD PA, which gives rise to non-linearity. On the contrary, the output gain and phase of the proposed PA are constant and not input-dependent. Therefore, the proposed PA is not sensitive to mismatches and is still intrinsically linear.

Behavioral simulation is performed to verify the previous calculations. A 20-MSymbol/s 64-QAM signal at a 2.6-GHz carrier is applied to both the VMD PA and the proposed TMM PA to verify the effect of mismatches on the signal integrity. Simulated EVMs with different mismatches are plotted in Fig. 10. The EVM of conventional VMD PA degrades rapidly with the increase of gain/delay mismatches, while the EVM of the proposed PA does not change, which proves that the proposed PA is not sensitive to mismatches. It should be mentioned that the delay mismatch will affect the FIR filter response, which causes ripple in the signal band. However, this is not a problem, since equalizers are widely adopted in the demodulators of modern wireless standards to compensate for the in-band gain variation. Therefore, the equalizer is enabled in the simulations of Fig. 10.

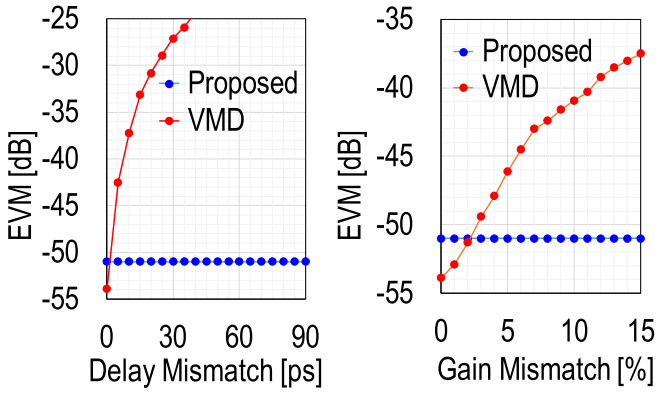


Fig. 10. Simulated EVM versus gain and delay mismatches between the two sub-PAs.

V. Implementation of the Prototype

A. Implementation of the Mixer

Fig. 11 shows the implementation of the proposed mixer in Fig. 6(b). I and Q are the baseband input signals, which are then encoded into 1 bit by the DSMs clocked at carrier frequency f_c. Next, DSM outputs are processed by the two-tap digital FIR filter. The 2-bit outputs of digital FIR are denoted as i and q in Fig. 11. $i+$ and $i-$ are the MSB and LSB of i, respectively. $q+$ and $q-$ are the MSB and LSB of q, respectively. Note that i and q are not encoded in standard digital format, i.e., 2's complement. They are encoded in a special way, as shown in Fig. 11 (top right). The three different values of i and q, -1, 0, and 1, are represented by the 2-bit digital codes 10, 00, and 01, respectively. Therefore, when $i = 1$, $i+ = 1$ and $i- = 0$.

The mixer is realized in a two-step manner. The square-wave signal at f_c drives two 2:1 multiplexers (MUXs), which convert $i+$, $i-$, $q+$, and $q-$ into 1-bit signals I_{in} and Q_{in}. I_{in} and Q_{in} serves as the input to the on-chip digital mixer. The on-chip digital mixer is another 2:1 MUX, but is driven by a square wave at twice the carrier frequency $2f_c$.

B. Implementation of the Overall PA

Fig. 11 also shows some waveform examples of the mixing process. Since DSM and digital FIR are clocked at f_c, i and q will update every RF cycle ($1/f_c$). In the off-chip MUX, the $I_{\mathrm{in}} = i+$ for the first half RF cycle, and $I_{\mathrm{in}} = i-$ for the next half RF cycle. Q_{in} is generated in the same way. Therefore, the sequence of $I_{\mathrm{in}} = [i+, i-]@2f_c$ and $Q_{\mathrm{in}} = [q+, q-]@2f_c$. A square wave at $2f_c$ drives the on-chip MUX. Therefore, its output updates every 1/4 RF cycles, and mixer output sequence $\mathrm{MIX}_{\mathrm{out}} = [I_{\mathrm{in}}, Q_{\mathrm{in}}]@4f_c = [i+, q+, i-, q-]@4f_c$. According to the i and q value in Fig. 11, the mixer should generate states 1, 8, 6, 5, and 7 in Fig. 6(b), sequentially. When comparing the waveform of $\mathrm{MIX}_{\mathrm{out}}$ with the states in Fig. 6(b), it can be seen that the two-step MUX-based mixer in Fig. 11 correctly realizes the mixing scheme in Fig. 6(b).

Fig. 12 shows the circuits of the implemented chip. The DSM is clocked at the carrier frequency to maximize the oversampling ratio of the DSM to increase the SNR. For a 20-MSymbol/s input signal with 8-dB PAPR and 2.6-GHz

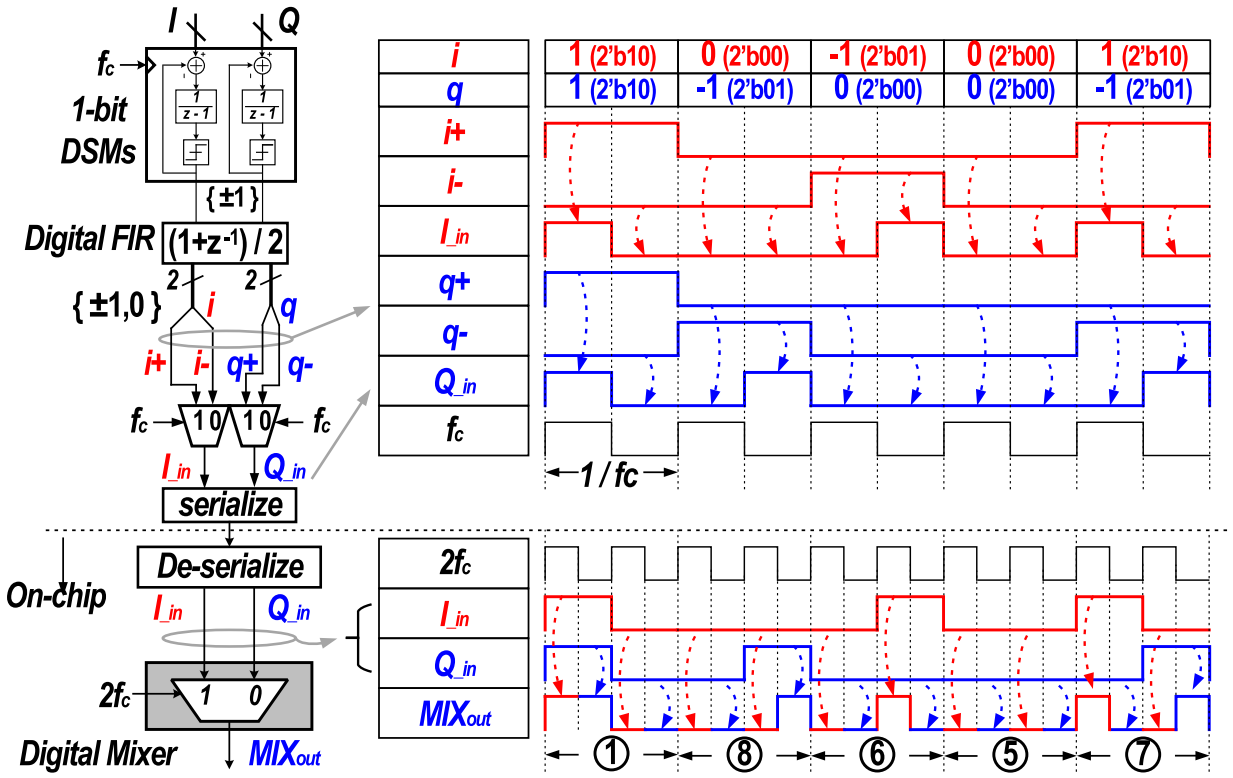


Fig. 11. Implementation of the proposed mixer and the waveform example.

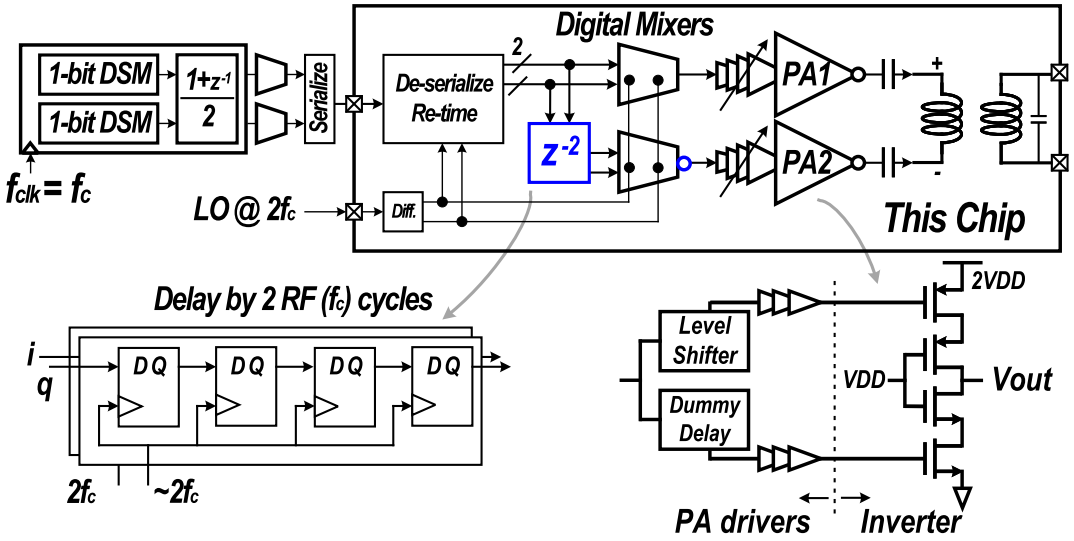


Fig. 12. Block diagram and circuits of the implemented chip.

clock, the DSM yields 52-dB SNR. High-speed digital logic, including DSMs and the digital FIR filters, is realized off-chip. The 2-bit input to the mixers is serialized to 1-bit and given to the chip. Therefore, we can reduce one input pad on the chip and use a normal ground–signal–signal–ground (GSSG) probe to measure the chip. The input is deserialized on-chip, then delayed, and drives the digital mixers. The chip's input LO is a square-wave signal at twice the carrier frequency. The LO is converted to a differential signal and clocks the on-chip de-serializer, re-timers, and mixers. Since the clock is twice the carrier frequency, four D-flip-flops (DFFs) are utilized to generate the delay of two RF cycles to form the two-tap XFMR combined semi-digital FIR filter. In the PA, 2.4-V supply and cascaded transistors are used to increase the output power [20]. Outputs of the two PAs are combined with an on-chip XFMR. In this implementation, we can demonstrate the working principle of the proposed PA without on-chip DSMs. However, implementing DSM is crucial, since it may be challenging to design high-speed logic, and the high-speed digital circuits may be power-hungry. Using commercial digital synthesis tools, we have synthesized the error-feedback DSMs and digital FIR filters.

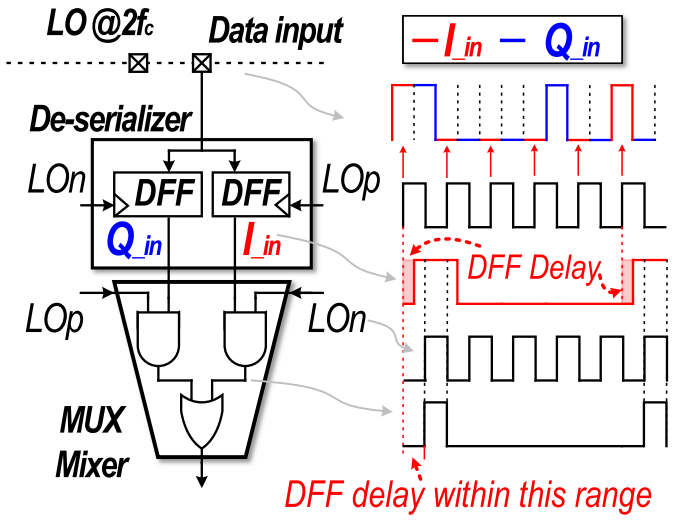


Fig. 13. Circuits of the de-serializer and the skew-free mixer.

The digital logics, including DSMs and digital FIR filters, can satisfy the timing requirements under 0.9 V/125 °C/ss-corner, 1.0 V/25 °C/tt-corner, and 1.1 V/−40 °C/ff-corner with 2.6-GHz clock. The power consumption is only 1 mW from post-layout simulations, which will have a negligible influence on the system's power efficiency.

C. Circuit Implementation of the De-Serializer and On-Chip Mixer

A big issue for the DSM-based PAs is the clock skew when re-timing the input digital signal [33]. However, in this chip, the on-chip mixer is realized skew-free. As depicted in Fig. 13, mixer inputs I_{in} and Q_{in} are serialized and given to the chip as the data input. Therefore, I_{in} and Q_{in} in the data input are interleaved. The de-serializer comprises two DFFs clocked by LOp and LOn. As shown in Fig. 13 (right), data input is re-timed by the rising edge of LOp and yields the I_{in} signal. The DFF will inevitably introduce a delay to its output, and the edge of I_{in} will lag LOp. I_{in} is then combined with LOn by an AND gate in the mixer. As we can see from the figure, if the rising edge of I_{in} is between the rising edge of LOp and LOn, the mixer can be skew-free. The delay between the rising edges of LOp and LOn is $1/4f_c$, which means that the DFF delay should be smaller than $1/4f_c$. Suppose the carrier frequency $f_c = 2.5$ GHz. DFF delay should be smaller than 100 ps, which can be satisfied in modern fine-line CMOS technologies.

VI. Measurement Results

A prototype chip is fabricated in a 65-nm CMOS process. Fig. 14 shows the chip micrograph. In the measurements, input signals to the chip are calculated using MATLAB, which are then loaded into an arbitrary waveform generator (AWG), Keysight M8195A. The AWG exports the input signals to the chip. A BALUN, Marki BAL-0006, converts the differential output of the PA into single-ended. Keysight UXR captures and demodulates the PA outputs.

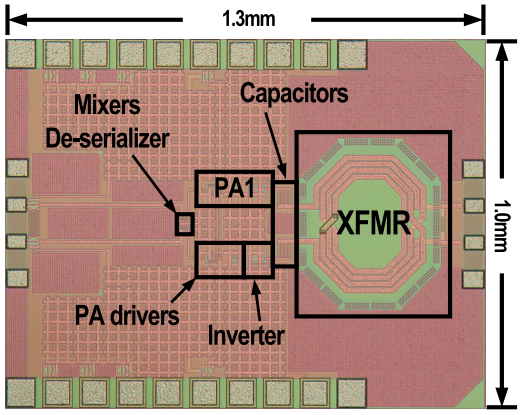


Fig. 14. Chip micrograph.

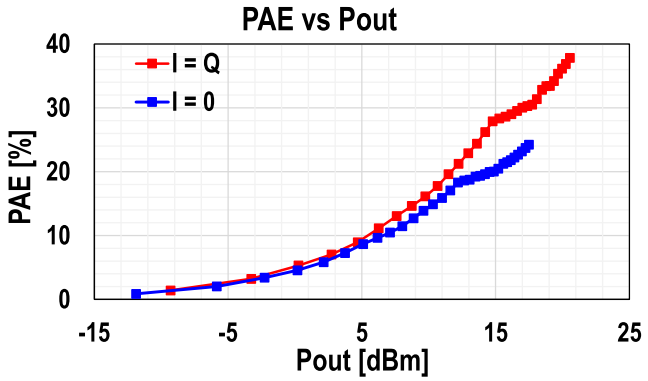


Fig. 15. Measured PAE versus output power with CW input.

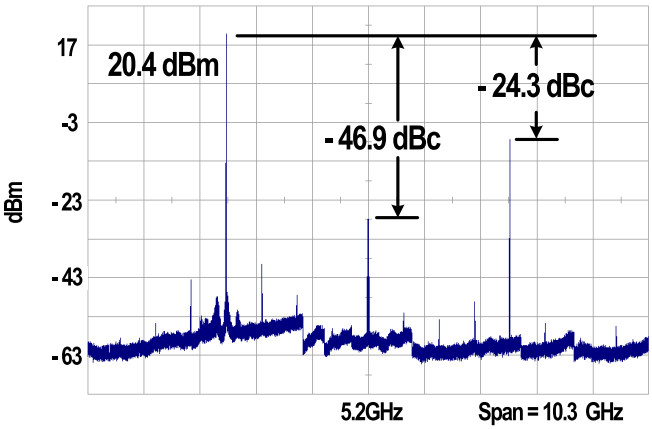


Fig. 16. Measured spectrum and harmonics with CW input.

A. CW Measurements

In continuous-wave (CW) measurements, the DSM inputs are swept from the minimum to the maximum for $I = Q$ and $I = 0$ path. A spectrum analyzer captures the power of the PA output (loss of off-chip BALUN and cable are de-embedded). Fig. 15 shows the power-added efficiency (PAE) versus output power. At a 2.6-GHz carrier, the proposed PA achieves 20.6-dBm peak output power, with a peak PAE of 37.8% under a 2.4-V supply. The PAE at 6-dB PBO of $I = Q$ path is 28.5%, 1.51× higher than the typical Class-B PA. Note that the power consumption of both the PA stage (inverter) and the PA drivers is included when calculating PAE. Fig. 16

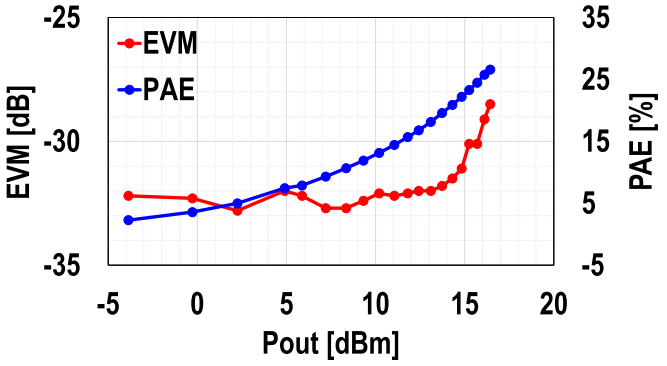


Fig. 17. Measured PAE and EVM versus output power with 20-MSymbol/s 256-QAM signal at 2.6-GHz carrier.

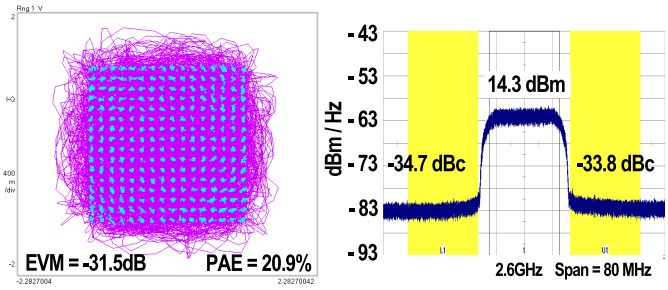


Fig. 18. Measured constellation and close-in spectrum with 20-MSymbol/s 256-QAM signal at 2.6-GHz carrier.

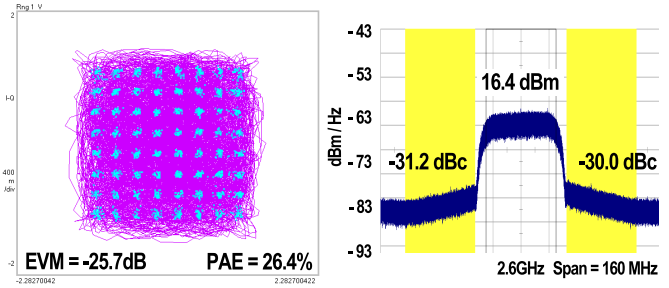


Fig. 19. Measured constellation and close-in spectrum with 40-MSymbol/s 64-QAM signal at 2.6-GHz carrier.

shows the measured spectrum and harmonics of the proposed PA. The second and third harmonics are −46.9 and −24.3 dBc, respectively.

B. Modulation Measurements

DPD is not applied in modulation measurements because of the good linearity provided by the proposed PA. With 20-MSymbol/s 256-QAM signal at 2.6-GHz carrier, the measured PAE and EVM versus output power is plotted in Fig. 17. At 14.3-dBm output power, the EVM is −31.5 dB, with a PAE of 20.9%, and Fig. 18 shows the measured constellation and close-in spectrum. The ACPR is −34.7/−33.8 dBc. Fig. 19 shows the measured constellation and close-in spectrum with 40-MSymbol/s 64-QAM signal. A high efficiency of 26.4% is achieved at 16.4-dBm output power, with an EVM of −25.7 dB. The ACPR is −31.2/−30.0 dBc.

The far-out spectrum of the proposed PA with and without the proposed hybrid FIR filter is depicted in Fig. 20.

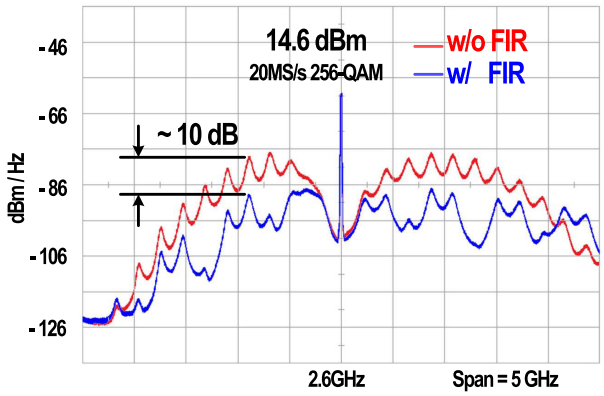


Fig. 20. Measured far-out spectrum with and without the hybrid FIR filter.

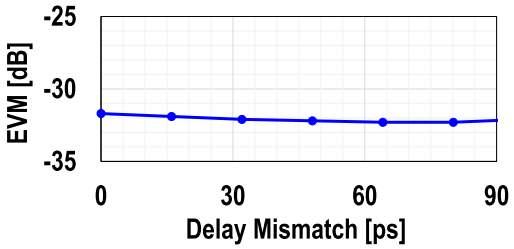


Fig. 21. Measured EVM versus delay mismatches.

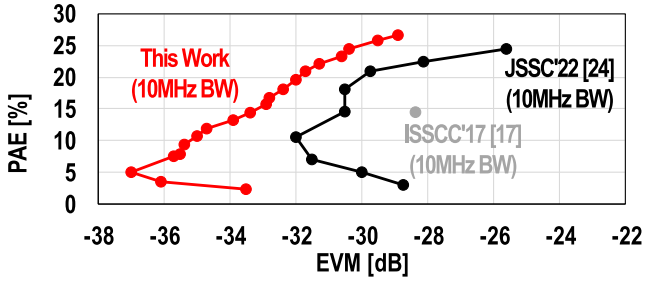


Fig. 22. Measured EVM versus PAE and comparison with prior arts.

Around 10-dB QN reduction is observed, contributing to high efficiency.

To prove the insensitivity to delay mismatches of the proposed PA, mixers are bypassed, and the two AWG outputs directly give the input signal to the PA. The delay mismatch of the two sub-PAs is controlled by changing the AWG output delays. Fig. 21 shows the measured EVM versus delay mismatch. The EVM has less than 1-dB variation with a delay mismatch as large as 90 ps.

Table I summarizes the performance of the proposed PA and compares it with other digital PAs. Compared with other DPD-less digital quadrature PAs [17], [22], at similar EVM levels, the proposed PA achieves higher efficiency and wider bandwidth. Also, it also supports 256 QAM. A 10-MSymbol/s 256-QAM signal is applied to the proposed PA to compare with [17] with similar bandwidth. Fig. 22 shows the measured PAE and EVM plots. The proposed PA achieves lower EVM and higher efficiency than prior arts at similar bandwidth. The proposed DPD-less TMM PA achieves comparable or better EVMs than digital PAs using DPDs [20], [21], [22], [34], [35], [36], demonstrating its good linearity. The PAE is also comparable to polar PAs. The hybrid FIR filter suppresses the

TABLE I
PERFORMANCE COMPARISON WITH OTHER DIGITAL PAS

	Tech. [nm]	PA Structure		Freq. [GHz]	PA VDD [V]	Peak Pout [dBm]	Peak PAE [%]	Average MOD.	Average BW [MHz]	Average Pout [dBm]	Average PAE [%]	Average EVM [dB]	DPD	OOB Emission [dBc/Hz]	HD2 /HD3 [dBc]	Core Area [mm2]
This Work	65	Quad	**1bit DSM Hybrid FIR**	2.6	2.4	20.6	37.8	**256QAM**	**20**	14.3	**20.9**	**-31.5**	No	-105.3	-46.9 /-24.3	0.34
								64QAM	**40**	16.4	**26.4**	**-25.7**			
ISSCC'17 [17]	28		Doherty SCPA	2.5	1.1	28.6	35	LTE	5	20.7	14.6	-30		N.A.	N.A.	1.14 *
JSSC'22 [24]	55		Doherty SCPA	0.85	2.4	29.3	43	64QAM LTE	10	22* 23.6	10* 24.4	-30* -25.6		N.A.	N.A.	1.2
TMTT'19 [32]	28 (SOI)		1bit DSM FIR C-DAC	0.9	1	4.6	28.2	LTE	10	-1.2	8.6	N.A.		-120 *	N.A.	0.047 #
JSSC'09 [28]	90		1bit DSM	0.65	1	3.1	N.A.	QPSK	5	-3.9	1	-38.1		-89 *	N.A.	0.15 #
JSSC'21 [18]	40		Doherty SCPA	2.8	1.1	24.2	32.7	256QAM	10	16.2	18.9	-32.3	Off-chip	-102	-25 /-20	0.83
JSSC'21 [26]	65		Class-G Doherty	2.2	2.55 /1.25	27.8	32.1	1024QAM	20	21	18.4	-43	Off-chip	N.A.	N.A.	0.9
JSSC'13 [20]	65	Polar	Class-G SCPA	2.15	2.8 /1.4	24.3	43.5 #	64QAM WLAN	20	16.8	33	-30.8	No	-120.5	N.A.	0.13 #
JSSC'19 [21]	65		Class-G SHS SCPA	2.25	3.6 /2.4	26.8	49.3 (DE)#	16QAM OFDM	5	16.6	35.7 (DE)#	-26	Off-chip	N.A.	-26 /-46	1 #
JSSC'19 [22]	65		Class-G SHS SCPA	1.9	3.6 /2.4	30	45.9 (DE)	16QAM OFDM	5	22.8	31.4 (DE)	-24.7	Off-chip	N.A.	N.A.	4.5 *
JSSC'23 [34]	40		Reconfig XFMR SCPA	2.4	2.5	32.7	35.5	256QAM	25	24.5	18.9	-32.1	Off-chip	-108.2	N.A.	0.99
JSSC'23 [35]	40		Doherty SCPA	1.8	2.5	28.9	37.2	256QAM	25	21.5	33.1 (DE)	-33.9	Self-Cal. (42.4 mW)	-114	-41.9 /-28.9	0.76
JSSC'16 [36]	65		Doherty Class-G	3.71	3 /1.65	26.7	43 (DE)	64QAM	1	16.8	24.5 (DE)	-28	Bias-Tuning	N.A.	N.A.	1.76 *

* Estimated from reported figures. # Off-chip inductors for matching networks.

DSM QN to improve efficiency, and the out-of-band emission is much smaller than the DSM-based TX without the FIR filter [28]. However, the out-of-band DSM QN is still higher than the emission of other SCPAs. Marin et al. [32] proposed to use a multi-tap FIR filter based on capacitor digital-to-analog converter (C-DAC) to suppress the DSM QN. Nevertheless, the switched capacitors in the C-DAC introduce significant power loss, and the efficiency degrades severely. Therefore, how to reduce DSM QN without sacrificing efficiency remains an open question.

VII. CONCLUSION

This article demonstrates a TMM digital quadrature PA with a hybrid FIR filter. The 1-bit PA is turned on and off sequentially to realize the TMM for efficiency improvement. The proposed TMM does not require a lossy capacitor array and is, thus, power-efficient. It is also intrinsically linear, since the output is 1 bit. The multi-bit I/Q input signals are encoded into 1-bit PA control code using 1-bit DSMs, a two-tap digital FIR filter, and the proposed digital mixer. A hybrid FIR filter comprising the two-tap digital FIR and another two-tap XFMR combined semi-digital FIR filter is also proposed to suppress the DSM QN to enhance efficiency. The XFMR combined FIR filter does not suffer from circuit mismatches. The implemented PA achieves state-of-the-art power efficiency and linearity at the same time. It can support 20-MSymbol/s 256 QAM without applying DPD with a PAE over 20%.

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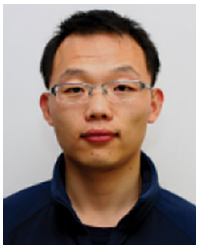
Dr. Sun serves as a reviewer for IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the *Microelectronics Journal* published by Elsevier, and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS.



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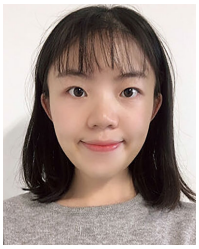
Dr. Liu serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I, and IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.



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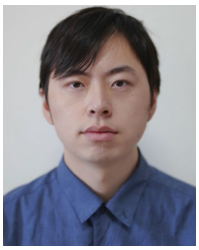

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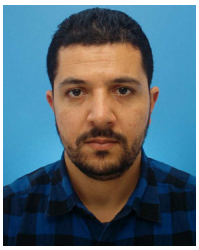

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