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DOI
10.1109/LATS49555.2020.9093667

Publication date
2020

Document Version
Accepted author manuscript

Published in
21st IEEE Latin-American Test Symposium, LATS 2020

Citation (APA)
Copetti, T., Medeiros, G. C., Taouil, M., Hamdioui, S., Poehls, L. B., & Balen, T. (2020). Evaluating the Impact of Ionizing Particles on FinFET -based SRAMs with Weak Resistive Defects. In *21st IEEE Latin-American Test Symposium, LATS 2020* Article 9093667 Institute of Electrical and Electronics Engineers (IEEE). https://doi.org/10.1109/LATS49555.2020.9093667

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Evaluating the Impact of Ionizing Particles on FinFET-based SRAMs with Weak Resistive Defects

Thiago Copetti[1], Guilherme Cardoso Medeiros[3], Mottaqiallah Taouil[3], Said Hamdioui[3], Letícia Bolzani Poehls[2], and Tiago Balen[1]

[1] Graduate Program on Microelectronics – PGMICRO, Federal University of Rio Grande do Sul, Porto Alegre, Brazil,
[2] School of Engineering, Pontifical Catholic University of Rio Grande do Sul, Porto Alegre, Brazil
[3] Computer Engineering Laboratory, Delft University of Technology, Delft, The Netherlands

***Abstract*— Fin Field-Effect Transistor (FinFET) technology enables the continuous downscaling of Integrated Circuits (ICs), using the Complementary Metal-Oxide Semiconductor (CMOS) technology in accordance with the More Moore domain. Despite demonstrating improvements on short channel effect and overcoming the growing leakage problem of planar CMOS technology, the continuity of feature size miniaturization allowed by FinFETs tends to increase sensitivity to Single Event Upsets (SEUs) caused by ionizing particles, especially in blocks with higher transistor densities as Static Random-Access Memories (SRAMs). Variation during the manufacturing process has introduced different types of defects that directly affect the SRAM's reliability, such as weak resistive defects. As some of these defects may cause dynamic faults, which require more than one consecutive operation to sensitize the fault at the logic level, traditional test approaches may fail to detect them and test escapes can occur. These undetected faults associated with weak resistive defects may affect the FinFET-based SRAM reliability during the lifetime. In this context, this paper proposes to investigate the impact of ionizing particles on the reliability of FinFET-based SRAMs in the presence of weak resistive defects. Firstly, a TCAD model of a FinFET-based SRAM cell is proposed in order to allow the evaluation of the ionizing particle's impact. Then, SPICE simulations are performed considering the current pulse parameters obtained with TCAD. In this step, weak resistive defects are injected into the FinFET-based SRAM cell. Results show that weak defects may have either a positive or negative influence on the cell reliability against SEUs caused by ionizing particles.**

Keywords—SRAMs, FinFET, Resistive Defects, TCAD, SEU, Reliability, Single Event Transient Modeling.

I. INTRODUCTION

Fin Field-Effect Transistor (FinFET)-based Static Random-Access Memories (SRAMs) represent one of the current state-of-the-art technologies for Systems-on-Chips (SoCs) since they are designed with high density and produced at the limit of the fabrication process. Furthermore, as FinFET is a recent technology, there is a need to evaluate and model its behavior with respect to defects and failures [1].

One major reliability issue in nanometer technologies are radiation-induced Single Event Effects (SEE), which are soft errors caused by ionizing particles [2]. In SRAM cells, a soft error may generate a bit inversion, a so-called Single Event Upset (SEU). This occurs when an ionizing particle strikes a reverse-biased PN junction (usually an off-state transistor's drain) initially generating a transient voltage pulse in a given circuit node. If the affected transistor belongs to the storage node of a cell, this transient may propagate through the feedback of the cross-coupled inverter, generating a bit-flip [3].

Another important reliability issue in FinFET memory technologies is related to weak resistive defects [1], which are caused by variability in the manufacturing process. These defects can be classified either as resistive-opens or resistive-bridge defects [4]. They can be classified as "weak" [5] if they are hard to detect, especially throughout performing traditional memory tests such as March tests [5]. These may then lead to test escapes, which might turn the FinFET device more prone to single events due to ionizing particle strikes in the field, as discussed in this paper.

It is known from the literature that radiation can lead to soft errors in FinFETs even at ground level [2], [6]. A number of works performed a comparative analysis regarding SEEs between FinFET and other technologies (conventional bulk CMOS and SOI) [2]. Also in [2], an analysis of FinFET-based SRAMs at different altitude levels was performed. Analysis of weak resistive defects have already been carried out for both planar SRAM cells [4] and for FinFET-based SRAM cells [7]. Further, an analysis of the radiation susceptibility of conventional CMOS SRAM cells in the presence of weak resistive defects is presented in [8]. Considering the existing work, we propose to analyze the influence of weak resistive defects on the FinFET-based SRAM robustness under single event effects. Because the FinFET structure is physically more complex than planar CMOS, a more precise and realistic simulation tool is necessary. Thus, a FinFET-based SRAM cell is modeled using a Technology Computer-Aided Design (TCAD) tool and simulations of ionizing particle impacts are carried out at physical level. Further, the transient current generated by such event is modeled at electrical level.

Hence, the main contributions of this paper are: 1) obtaining, by physical simulation, the minimum value of Linear Energy Transfer (LET) of an incident particle that results in a bit-flip (LET_{th}, or threshold LET) for FinFET SRAM cells designed in a technology equivalent to a 14 nm node; 2) the proposal of a SPICE model for the obtained current curves; and 3) investigating the impacts of resistive defects on the reliability of FinFET-based SRAM cells under single events.

II. BACKGROUND

FinFETs are transistors composed of thin vertical slices of silicon (known as fins) that are wrapped by the gate structure and built on top of a silicon substrate [1]. These fins comprise the channel region of the transistor. This work considers the

bulk FinFET model, in which the fins are directly connected to the substrate and the oxide is used to isolate each fin from the others.

A schematic of a standard 6T-SRAM is illustrated in Fig. 1. For sake of conciseness, this figure also shows the equivalent resistive defects and transient current modeling that are presented in Section III. This cell is composed of six transistors: two cross-coupled inverters (M_1 & M_2, M_3 & M_4), that store the digital information in nodes Q and its counterpart $\bar{Q}$, and the other two nFET transistors acting as Pass Gates (PG) (M_5 and M_6), responsible for isolating the cell during hold phase, and open the cell during read and write. The word line (WL) signal controls the two Pass Gates that are connected to the bit lines (BL and $\overline{BL}$) [4].

One of the main causes of test escapes of new technologies, as bulk FinFET is the weak defects, because this FinFET-based SRAM is more susceptible to dynamic faults than conventional planar CMOS-based SRAM [1]. Weak resistive defects are defects with resistive characteristics that cause small variation in the electric parameters of the device [10]. In SRAM cells, such defects can generate dynamic faults, which need multiple consecutive read operations to generate an error at logic level [9]–[11]. Weak defects can be classified as weak resistive-open and weak resistive-bridge defects. A resistive-open is modeled as a resistor between two nodes that share a connection, and a resistive-bridge is modeled as a resistor between two nodes that not should be connected [4], as illustrated in Fig. 1.

In [12], a comparison of SEE effects between a 16 nm bulk FinFET and a 28 nm bulk planar technology was carried out. This study shows that low-LET particles may cause transients in FinFETs when hitting the fin region. Therefore, FinFET technology has a very strong dependence on the ion strike location, unlike planar CMOS, which demonstrates less dependence on the position of impact is the same study reported that a strike between two fins produces a very small transient voltage. This effect happens in FinFETs due to their low charge collection efficiency, which means that a small fraction of the generated electron-hole pairs is collected at the FinFET drain during the silicon ionization, resulting in lower current pulses [2].

However, with the proximity of connections and the reduced supply voltage, FinFET-based SRAMs are becoming more susceptible to SEUs, even at ground level [6]. Traditionally, the major sources of radiation-induced soft errors at ground level or flight altitudes are: (1) alpha particles originated by the radioactive contamination existing in the packaging [13], [14]; (2) the high-energy neutrons from cosmic radiation (generating secondary reactions); and (3) the interaction of cosmic ray thermal neutrons with devices containing borophosphosilicate glass [14]. The work reported in [2] has shown that for SRAMs, protons, and muons are also among the particles able to generate SEUs at ground level in bulk FinFET technologies.

III. Methodology

Firstly, to evaluate the transient effects caused by ion strikes, a layout of a 14 nm FinFET-based SRAM cell was designed and modeled in Sentaurus™ TCAD tool. This technology node was chosen due to its current use by memory manufacturing companies. This section also describes the methodology carried out to simulate ionizing particle strikes at the physical level, and the SPICE modeling of resistive defects.

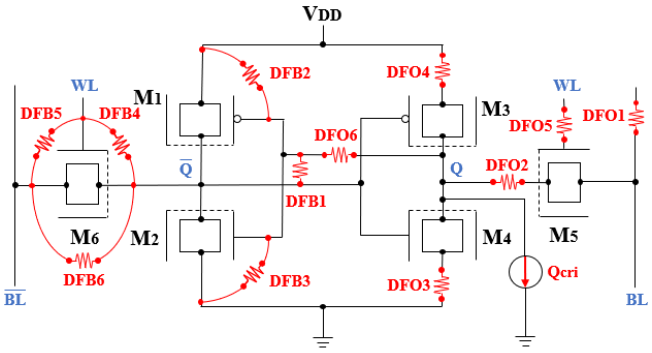


Fig. 1. FinFET-based SRAM cell with injected defects and transient current.

A. SRAM Cell Modeling in TCAD

To study the effects of SEUs, an initial FinFET SRAM 3D model was developed using Sentaurus™ TCAD. In comparison to SPICE simulations, this tool allows larger flexibility while controlling the device's physics aspects, including the impact location of ionizing particles and its associated LET. This study considers three models of FinFET-based SRAM cells: HD (High-Density), HP (High Performance) and LV (Low Voltage). Because of the discrete nature of fins, it is not possible to tune the transistor parameters to obtain an ideal robustness/area ratio as it would be feasible in planar CMOS. Therefore, each model has its configuration with a different distribution of fins in the cell's transistors. The SRAM cell structure is divided into three parts with their proper notation (PU:PG:PD), meaning respectively: Pull Up, Pass Gate and Pull Down [15]. As an example, the HD configuration adopts a (1:1:1) configuration, meaning that all the cell transistors are composed of a single fin.

The transistors designed with the Sentaurus™ tool were calibrated using the physical characteristics described by the 2015 ITRS [16], shown in Table I. The mesh grid configured in these simulations were generated given special attention to the active zones such as channel, source, and drain. Using the Sentaurus™ Device, the functional parameters of the circuit are implemented in order to validate it. Finally, the injection of the ionizing particle is modeled using the same tool.

B. Modeling Ion Strike

The heavy-ion injection in TCAD simulation follows the methodology presented in [12], considering a Gaussian charge distribution with a track radius of 10nm. To model the worst-case scenario of such particle strike, the charge track length should be longer than the fin height, with normal incidence over the drain of the sensitive transistor (off-state transistor). The sensitive transistor is the pull-down transistor when the node (inverter output) is charged with a logic '1', or the pull-up transistor when the node is '0'.

In the simulation setup, the input parameters for the heavy ions are given in charge per track length (pC/μm). To convert this value into the LET parameter the relation of 1 pC/μm is equivalent to a 97 MeV-cm²/mg LET in silicon [13]. For example, the alpha particles due to radioactive contamination

TABLE I. ADOPTED PHYSICAL PARAMETERS FOR FINFETS

Physical Parameters	Values (nm)
Physical Gate Length	26
Fin Width	8
Fin Height	42
Fin Pitch	42
Poly Pitch	90
Effective Width	92
Metal Pitch	56

in the packaging material can result in 0.015 pC/µm, which approximates 1.5 MeV-cm²/mg [13]. This analysis aims to find the threshold LET that causes a bit-flip in the cell. Considering this LET, the drain current in the affected transistor is evaluated, modeled, and compared with the traditional double exponential. The obtained current shape is modeled in SPICE to allow transient injections and resistive defects at the same time. This analysis is carried out in SPICE since TCAD simulations would demand a huge computational effort.

C. Injecting Resistive Defects

The electrical simulations to evaluate the robustness of a FinFET-based SRAM cell are performed using Hspice™ from Synopsys, adopting the Arizona State University's 14nm FinFET Predictive Technology Model (PTM) [17], combining single event transient with weak resistive defects. For this purpose, the injected charge to simulate single events in SPICE is set with a value lower than the excess charge observed when simulating a particle strike with LET=LET_{th}, while simultaneously injecting resistive defects. In this case, the values of defects' resistances are varied using an automated tool that interacts with the SPICE simulator. In this work, the critical resistance (R_{crit}) is the defect resistance threshold that results in a bit-flip when injected the ionizing particle. The methodology for resistive defects injection is the same used in [7] and [18]. Fig. 1 shows the classical defects presented in [4]. This effort is necessary to observe if resistive defects may change the cell's robustness to SEUs. The opposite situation was also verified, simulating an event depositing the critical charge (Q_{crit}) at the same time that resistive defects are injected, in order to determine if the single event effect (SEE) is attenuated due to a given defect.

IV. RESULTS AND DISCUSSION

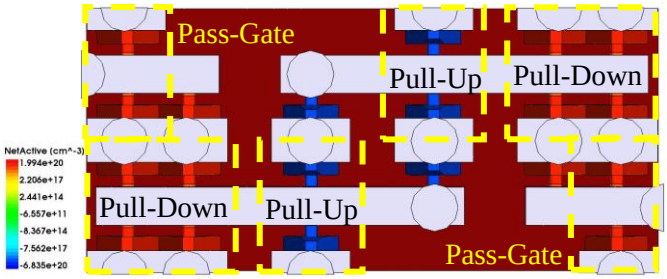
This section presents the results divided into three sub-sections: A) the modeling and validation of the FinFET-based SRAM cell in TCAD; B) TCAD-based SEE injection results and comparison with SPICE injections; C) the influence of resistive defects on cell reliability under single events.

A. SRAM Cell Validation

As described before, a FinFET-based SRAM cell was implemented based on the physical parameters described on the 2015 ITRS [16], and as presented in [15]. Three different models were adopted, whose configurations (number of fins of the transistors), along with the corresponding area, are shown in Table II. As an example, Fig. 2 shows an LV SRAM cell modeled in 3D-TCAD. Different from this exemplary cell, the HD configuration, the most compact, would not possess a fin column on each side of the cell, and the HP configuration would show two fins in the pass gate. To reproduce industrial devices, only HD and LV cells use source and drain regions

TABLE I. NUMBER OF FINS OF DIFFERENT SRAM CELLS DESIGN

Configuration	(PU:PG:PD)	Area (µm²)
HD	(1:1:1)	0.0558
LV	(1:1:2)	0.07092
HP	(1:2:2)	0.07092



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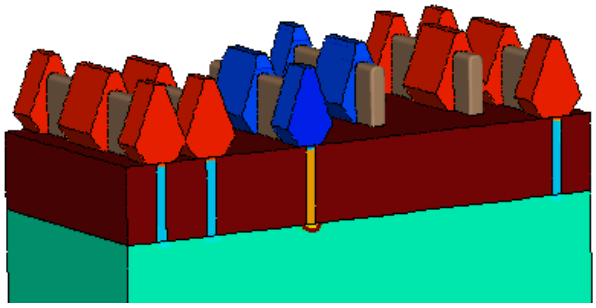


(b)

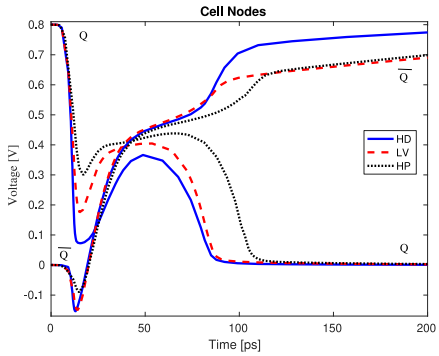
Fig. 1. FinFET LV SRAM cell implemented in this work: (a) top view; (b) 3D view without gate and metals.

with a polyhedron over the fin [15]. Note that these structures do not cause a considerable current variation in the transistor when compared with the HP cell. Electrically, the LV model has a more robust SNM for a read operation, and the HP model is faster during reading and writing operations [15].

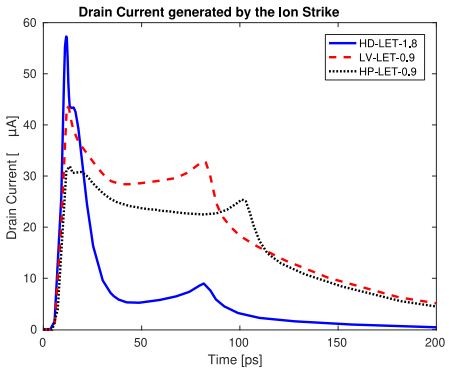
To validate if the electrical operation of the device is compatible with the 14 nm node used as target technology, the electrical behavior was compared to the drain current/gate voltage data from the Arizona State University's Predictive Technology Model (PTM) [17]. The I_D x V_G (drain current x gate voltage) behavior, as well as the obtained static noise margins of both models, agree with low discrepancies for all design variants of the SRAM Cell. Therefore, the cells developed in TCAD are suitable to model the cells designed in 14 nm node. The data used to support this conclusion is not shown in this paper, caused by limited space, besides not being this work's focus.

B. Results of TCAD single event transient simulations

The heavy-ion simulation considers the particle strike in the corresponding time of 10 ps. The parameters used to model the ion track were already described in Section III. Considering the cells' design with a depth of 1 µm, the deep length for the ion track was set as 0.9 µm. Fig. 3 presents the behavior of cells in a simulation in which an SEU is observed. Fig. 3(a) presents the bit-flip caused by ionizing particles with the lower LETs (threshold LET, or LET_{th}) in the different designed cells, or, in other words, when Q_{crit} is achieved. However, according to [3], the definition of critical charge in SRAMs is not as intuitive as



(a)



(b)

Fig. 2. (a) Bit-flip in the cell; (b) Current generated by the ion strike.

for logic circuits, where it is associated exclusively with the charge stored in the node and the drive strength of the restoration transistors. In SRAMs, the feedback plays an important role, collaborating with the behavior of the transient current pulse. Two ways of defining the critical charge can be found in the literature. The first one considers the value of deposited or collected charge that starts to generate bit-flips. The second definition considers the value of the charge flowing in excess during the transient current in the affected node, which considers also the charge flow due to the circuit dynamics (hence not merely the collected charge) [3]. Fig. 3 (b) shows the drain current observed for particles (with LET=LET_{th}) injected at one of the inverter's nFET transistors. One can notice a plateau region on the current pulses, corresponding to the occurrence of the feedback action. The feedback action tends to activate the nFET transistor, which is nominally off before the transient. As can be observed from Fig. 3 (a), the plateau happens while both transistors are simultaneously in conduction state (near the inverter trip point). Since the *n* devices of LV and HP cells are built with two fins, the current on this plateau is higher, which facilitates the inversion of the bit stored in the cell. Thus, it can be expected that the LET_{th} for these two models is similar.

The data presented in Table III demonstrates that the HD cell is the most robust when considering transients injected in pull-down transistors; the LET_{th} obtained with TCAD simulations is higher. The table's remaining columns show the charge which is injected to simulate the heavy-ion (Q_{dep}) and the excess charge (Q_{exc}), which is the charge disturbance on the affected node (integral of the transient current). Despite the

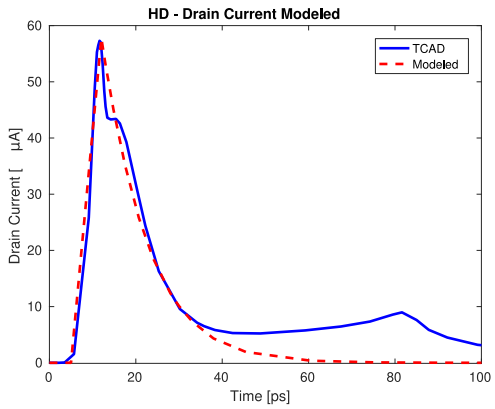
TABLE II. THRESHOLD LET AND DEPOSITED CHARGES (TCAD)

Cell	LET_{th} (MeV-cm²/mg)	Q_{dep} (fC)	Q_{exc} (fC)
HD	1.8	16.7	1.24
LV	0.9	8.34	3.79
HP	0.9	8.34	3.55

lower LET_{th}, one may notice that Q_{exc} is higher for LV and HP cells due to circuit dynamics. Another point that deserves attention is that not all the deposited charge is collected, as already discussed by [3]. Indeed, related works often consider the quantity denominated Q_{exc} as the critical charge in SPICE-based injection campaigns. However, it is clear that this may lead to an erroneous evaluation regarding the circuit's reliability, especially for SRAMs, as can be observed in Table III. According to [19], Q_{crit} values computed from 3D device simulation currents are approximately 3 times smaller than those found using current models. Therefore, this paper uses the value of LET_{th}, based on the values obtained with TCAD, for reliability comparison purposes. Additionally, for SPICE simulations, we use the quantity Q_{exc}, which is the charge disturbance on the circuit due to the impact of a particle with LET= LET_{th} on the drain of the sensitive transistor. From here on, this work avoids using the term critical charge during its analysis, since smaller LET values and deposited charges may result in a higher amount of excess charge as observed in TCAD simulations and in Table III.

The observed current curves in TCAD simulations were then modeled as current sources in SPICE. The well-established Messenger's double exponential model [20] is still being applied in related works to simulate SEEs due to its simplicity, even for recent FinFET technologies [6]. However, in some cases, this model may not accurately represent the current behavior. For instance, in this work, the double exponential is suitable to model a particle with LET=LET_{th} striking the pull-down transistor of the HD cell, because the current from the plateau has low effect in the bit-flip, while the same is not true to the LV and HP cell (Fig. 3 (b)). A previous work that investigated single events in FinFETs [6] considered the following values using the double exponential time constants for the execution of SPICE simulations: τ_1 = 2 ps and τ_2 = 20 ps (time constants of rising and falling exponentials, respectively). However, TCAD simulations in the present work showed that, for strikes on nFET of the HD configuration, the rising and fall times are similar, resulting in τ_1 = 6 ps, τ_2 = 9 ps, and ($t_{d2} - t_{d1}$) = 7 ps (t_{d1} and t_{d2} are the initial times of both exponentials). Therefore, the double exponential curve is shown in Fig. 4(a) was used to perform transient injections on HD cells in SPICE, though varying the current peak according to the desired injected charge. Both curves (TCAD and SPICE modeled double exponential) are shown in Fig. 4(a).

On the other hand, the pulse shapes observed for the LV and HP configurations are significantly different from the double exponential. Hence, following the methodology proposed by [21], a combination of three exponential sources in SPICE is proposed to represent the behavior. The first is the double exponential with τ_1 = 6 ps, τ_2 = 8 ps, and ($t_{d2} - t_{d1}$) = 7 ps with a short peak, the second source is a long double exponential with τ_1 = 6 ps, τ_2 = 100 ps, and ($t_{d2} - t_{d1}$) = 80 ps. Finally, an exponential curve with a slow rising time constant completes the modeling, whit τ_1 = 85 ps, τ_2 = 8 ps, and ($t_{d2} - t_{d1}$) = 80 ps. These curves are shown in Fig. 4(b).



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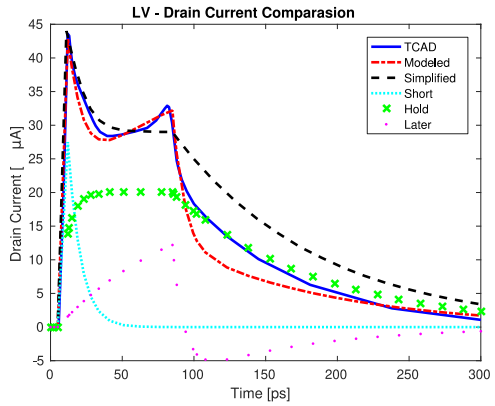

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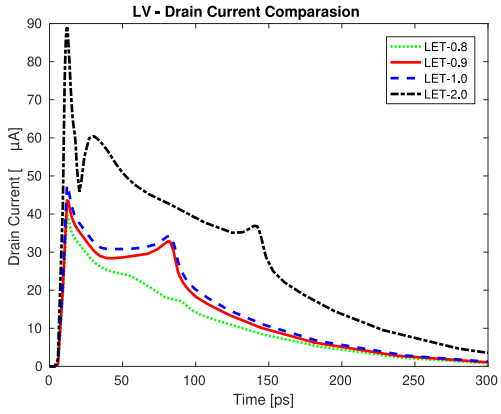

(c)

Fig. 3. Transient current modeled in spice for (a) HD cell and (b) LV cell and (c) comparison of curves with different particle LETs for LV cell (TCAD).

Although these three source models fit the observed transients very well, a further simplification may be executed. Fig. 4(c) shows a comparison of curves with different particle LETs for LV cell, including a simulation in which no bit-flip has occurred. Based on these and other performed simulations, it was verified that besides the current's peak value, the plateau amplitude and duration are the main parameters of the curve related to bit-flips. Therefore, the component of the later peak from the proposed curve can be removed to simplify the model, though keeping the plateau as shown in Fig. 4(b).

TABLE III. EXCESS CHARGE CONFIGURATION

Cell	Q_{exc_nom} (fC)	I_{peak} (µA)	$I_{plateau}$ (µA)
HD	1.01	63.5	-
LV	5.28	47.0	31.0
HP	5.46	47.9	32.1

TABLE IV. WEAK RESISTIVE DEFECTS THAT INCREASE THE SEU SENSITIVITY OF THE STUDIED SRAM CELLS

Cell	Q_{exc_alt} (fC)	I_{peak} (µA)	$I_{plateau}$ (µA)	R_{crit} (Ω)
HD	0.909	56.0	-	DFO2 = 399, DFO4* = 91
				DFB1 = 1.524M, DFB2* = 1.680M
				DFB3&4 = 710.6k, DFB6 = 1.680M
LV	4.77	41.6	28.0	DFO2 = 4.351, DFO4* = 920
				DFB1 = 209.5k, DFB2* = 1.145M
				DFB3&4 = 106.8k, DFB6 = 145.0k
HP	4.94	43.6	29.1	DFO2 = 3.480, DFO4* = 708
				DFB1 = 638.7k, DFB2* = 348.3k
				DFB3&4 = 163.1k, DFB6 = 348.4k

C. *Influence of resistive defects on SEU reliability*

Electric simulations were performed with Hspice™ using the 14 nm PTM technology, and simulating the ionizing particle as a current source in the pull-down transistor according to the models presented in the previous Section. The values of excess charge corresponding to the transient effects (Q_{exc_nom}), the peak current (I_{peak}) and the plateau current ($I_{plateau}$) are summarized in Table IV. Note that the values of Q_{exc_nom} were obtained by integrating the current pulse, considering the lower values of I_{peak} that resulted in bit-flips in the SPICE model, and modeling the same value of plateaus observed in TCAD. This way, some variations in Q_{exc_nom} were observed when compared to TCAD. This is due to the application of different technological parameters for the TCAD model and the SPICE PTM model.

Table V shows the observed values of critical resistances, along with the values of simulated excess charge and the correspondent current peak and plateau. For resistive open defects, the critical resistance is the lowest value that, considering the reduced value of Q_{exc_nom}, results in a bit-flip. For resistive bridges, the critical resistances are the highest values that render the cell susceptible to SEUs. The defects marked with '*' indicate that this defect was injected into a different inverter of the cell than the transient was injected into.

Looking at Table V it is possible to observe that weak resistive defects may indeed modify the cell robustness. Examples are DFO2 and DFO4, which are low resistance open defects, as well as DFB2 and DFB6, which represent high resistances for bridge defects (weak defects). These values of defects may not be detectable in production tests, even those considering dynamic faults, according to the results in [18].

The opposite situation was also investigated: simulating the nominal value of excess charge that generates a bit-flip in a healthy cell. It was possible to observe that some defects may turn the cell more robust to the SEUs, as shown in Table VI. It is interesting to notice that some defects may have distinct impacts when occurring in the inverter that suffers the SEU or during their occurrence in the opposite inverter. For example, if DFO2 occurs in the inverter hit by the ion, the bit-flip occurrence is facilitated, while, if it occurs in the opposite inverter, a higher collected charge is needed to turn the event into an SEU.

TABLE V. WEAK RESISTIVE DEFECTS THAT PREVENT BIT-FLIPS, CONSIDERING THE CRITICAL EXCESS CHARGE (SPICE)

Cell	Q_{exc_nom} (fC)	R_{crit} (Ω)
HD	1.01	DFO2* = 2.429, DFO3 = 5.623
		DFO4 = 1.603, DFO6 = 2.715
		DFB2 = 645.1k , DFB3&4* = 11.30k
		DFB6* = 645.1k
LV	5.28	DFO2* = 7.052, DFO3 = 2.044
		DFO4 = 4.128, DFO6* = 664
		DFB3&4* = 168.3k, DFB6* = 1.322M
HP	5.46	DFO2* = 310, DFO3 = 132
		DFO4 = 4.803, DFO5 = 157
		DFO6 = 351, DFB2 = 5.122M
		DFB3*&4* = 5.036M, DFB6* = 5.122M

V. CONCLUSION

This work analyzes the impact of SEEs on defective FinFET-based SRAM cell reliability. To accomplish this, three variants of an SRAM cell of 14 nm were modeled with a TCAD simulator. In a subsequent step, ion strikes were simulated in the modeled cells. As a contribution, the obtained current shapes and the corresponding excess charges for the different design variants (HD, LV, and HP) were modeled.

This work also remarks that physical (TCAD) simulations may be mandatory if the goal is to evaluate the design sensitivity to a given energy spectrum of incident particles. This is due to a specific SRAM circuit dynamic: a particle with lower LET may result in a higher value of excess charge, as demonstrated in this work. Therefore, SPICE simulations that consider this value as a comparison parameter (or considering it as critical charge), maybe not accurately representing the actual reliability of the memory against single events in real radiation environments.

In this work, considering the TCAD simulation data, the HD cell demonstrated to be more robust than HP and LV cells, since a higher LET was necessary to trigger a bit-flip. After a discussion on the suitability of applying the double exponential model to simulate SEE in this technology, the obtained current shapes observed in TCAD, while simulating ion strikes, were modeled in SPICE. For certain cell configurations and particle energy conditions, the double exponential is still a satisfyingly accurate model, while for other cases different current modeling had to be proposed.

Finally, this paper shows that weak resistive defects may indeed affect the behavior of the cell under single events. In fact, some weak defects may turn the cell more prone to SEUs. However, some defects may prevent bit-flips to occur, considering the LET_{th} observed for a defect-free cell, making a higher particle LET necessary in order to generate an SEU. This ambiguous behavior is explained by the fact that the amount of excess charge due to a single event in SRAMs is highly dependent on the circuit's dynamic response, which indeed may be significantly modified by the occurrence of resistive defects.

ACKNOWLEDGMENT

This study was financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior – Brasil (CAPES) - Finance Code 001, the Programa de Doutorado Sanduíche no Exterior (PDSE) 2017/2018, process nº 88881.188720/2018-01, and European Union's Horizon 2020 under grant 722325.

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