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Exploring on-line RF performance monitoring based on the indirect test strategy

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***Abstract*—This paper deals with the general domain of IC reliability and targets more specifically RF circuit. It investigates the feasibility of implementing on-line RF performance monitoring based on the indirect test strategy. The principle of the proposed solution is introduced and the essential requirements needed to adapt the indirect test strategy are discussed. The proposed solution is then applied to a wireless microcontroller with the objective to monitor the power level delivered by the RF transmitter. Hardware measurement results are presented, which demonstrate the potential of this approach and establish a proof-of-concept.**

Keywords— RF integrated circuits, reliability, on-line monitoring, indirect test, machine-learning

I. INTRODUCTION

RF devices are nowadays used in an increasing number of applications and they are produced in very high volume. It is a very competitive market and it is therefore essential to verify the quality of devices shipped to the customers, which is the role of production test. However, the quality of the devices at the time of their production is not sufficient and their reliability once deployed in the application is becoming a real concern, especially for devices used in critical-safety applications such as fire detection, entrance access control, smart metering, … In this context, there is a need for methods allowing on-line performance monitoring in order to warn the user if the device experiences a degradation; the user can then take proper actions before a complete failure of the system occurs.

Reliability issues have been extensively studied for digital devices and a number of on-line monitoring solutions have been proposed. In contrast, research is scarcer for analog/RF circuits. The design of an adaptive checker for concurrent error detection based on common mode signal analysis is investigated in [1]. Authors in [2] proposed a real time estimation to monitor a performance accurately by capturing the distortion performance variation. The use of an embedded temperature sensor [3] or a current-based monitor circuit [4] has been proposed to implement RF performance monitoring. Our objective is to explore a different approach which is based on an adaptation of the indirect test strategy.

For the sake of comprehension, the basic principle of the indirect test strategy, which has been proposed to reduce the production testing costs of analog/RF circuits, is briefly recalled here. The objective is to replace the conventional and costly RF measurements usually performed during production test by some Indirect Measurements (IMs) that can be measured at low-cost. The underlying assumption is that process variations that affect the device RF performances also affect indirect parameters. So, if the correlation between these two spaces can be established, it is then possible to predict the RF performances using only the indirect measurements. The relation between these two sets of parameters is complex and cannot be simply identified with an analytic function; instead, machine-learning algorithms are used. The classical implementation of the indirect test strategy for production testing therefore involves two phases, as illustrated in Figure 1. There is first an initial learning phase in which both the conventional RF measurements and the low-cost IM measurements are performed on a set on training devices and machine-learning algorithms are used to build regression models that map the indirect measurements to the RF performances. These models are then exploited during the second phase, i.e. the production testing phase, in which the RF performances of every new device are predicted based only on the low-cost indirect measurements; the device is then binned as a good or bad circuit depending on the predicted values.

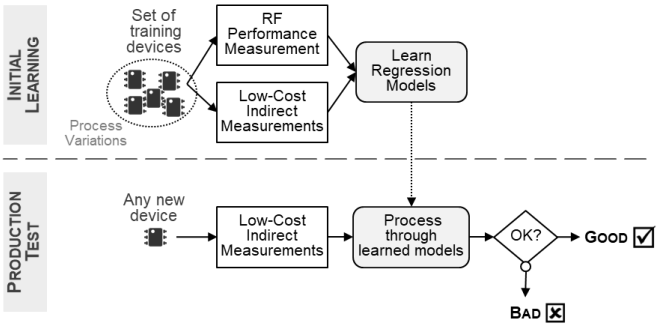

Fig.1: Indirect test synopsis

The efficiency of the indirect test strategy for production testing has been widely studied in the literature, including various aspects such as the choice of the regression model type, the selection of relevant indirect measurements, the use of embedded sensors, the adoption of an adaptive test flow... A comprehensive review of these works can be found in [5]. Some studies have also investigated the use of the indirect test strategy to implement Built-In Self-Test (BIST) [6,7] or to perform post-manufacturing calibration [8.9] of analog/RF circuits. However, to the best of our knowledge, the use of the indirect test strategy has never been investigated to implement on-line RF performance monitoring. It is the objective of this paper.

II. ADAPTATION OF THE INDIRECT TEST STRATEGY FOR ON-LINE PERFORMANCE MONITORING

A. Principle

The principle of the proposed strategy for on-line performance monitoring is illustrated in Figure 2. As in the

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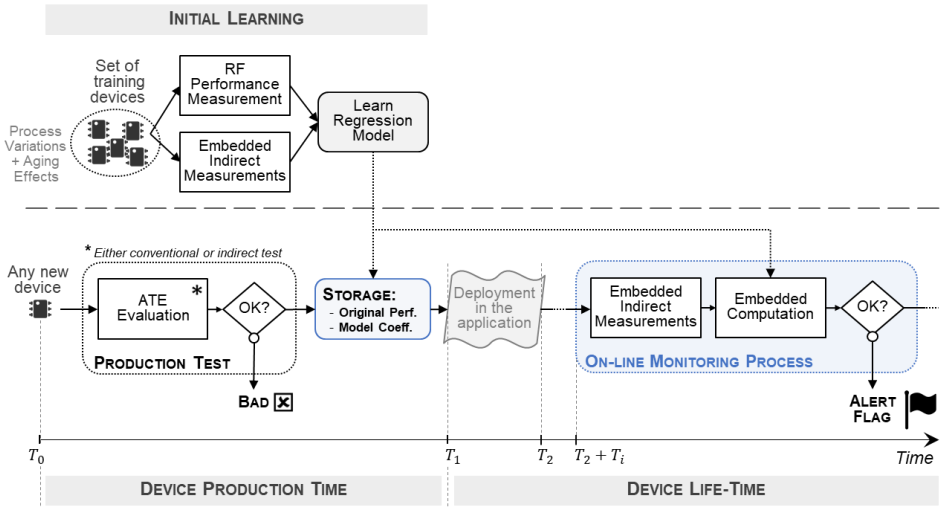

Fig.2: Principle of on-line RF performance monitoring based on the indirect test strategy

classical indirect test implementation, it involves a preliminary learning phase in which the mapping between a given circuit performance and some indirect measurements is established through the construction of a regression model. The main difference is that the learning set should include not only devices affected by process variations but also devices representative of the main wear-out failure mechanisms susceptible to occur during the circuit life. It is therefore recommended that the learning set includes devices that have been subjected to accelerated life tests or burn-in.

Once the learning phase is over, mass production can start. Every new manufactured device undergoes a production test; devices that do not comply with the specifications are rejected (this test can be implemented using either a conventional approach or an indirect test solution). Before shipping good devices to the customers, there is then an additional step which consists in storing within the IC the original value of the performance that will be monitored and the values of the model coefficients determined in the previous phase.

Finally, once the device is deployed in its application, the on-line monitoring process can be triggered at any time. It involves the embedded measurement of the selected IMs and the embedded computation of the performance value. In this process, the device predicts its own performance variation based on the model established during the learning phase and the values stored within the IC at production time; a flag alert is raised if the predicted performance variation exceeds a predefined threshold.

B. Hardware Requirements

To perform the embedded prediction, a number of hardware resources are obviously necessary: (i) a dedicated infrastructure in order to access to the internal nodes or structures involved in the indirect measurements, (ii) digitization resources to convert the measured analog values into the digital domain, (iii) a non-volatile memory to store and fetch the coefficients of the established regression model and finally, (iv) a processing unit to perform the computation of performance prediction. The main requirements on these resources are discussed hereafter. Note that all these resources do not necessarily have to be embedded within the circuit itself, some of them might be available within the system in the application.

1) Indirect Measurements

A specific requirement for an on-line monitoring process is that all the considered IMs must have the possibility to be measured on-chip, and preferably with a simple measurement infrastructure. In this context, the most natural candidates are DC voltages on internal nodes and DC signatures delivered by built-in sensors accessible through an internal analog test bus.

Furthermore, the main motivation behind the on-line performance monitoring strategy is to observe and detect any performance deterioration induced by aging effects. The most important aging phenomena observed today in nanometric technologies are hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), bias temperature instability (BTI) and electromigration (EM). These aging phenomena affect not only the digital parts but also the analog/RF parts [10]. It is highly desirable that the set of IM candidates include indirect measurements sensitive to these wear-out mechanisms. Due to practical constraints, this aspect is not considered for the case study used in this paper.

2) Digitization

Once the indirect measurements and the test infrastructure allowing to access these measurements are defined, the following step is the choice of the digitization resources. It is essential that the quantization error introduced by this analog-to-digital conversion does not significantly affect the accuracy of the computed prediction. The choice and the design of the digitization resources is therefore an important aspect.

The choice should take into consideration the characteristics of the different indirect measurements. Indeed, it is likely that they cover a large voltage range while the variation range of each indirect parameter might be small. The digitization resources have to cope with this diversity without comprising the conversion accuracy. Several options can be considered for the design of the required digitization resources, i.e. (i) a single high-resolution ADC with a large measurement range that covers the complete variation range of all indirect measurements, (ii) a single medium-resolution ADC with a programmable measurement range that can be adapted to

groups of indirect measurements with a similar order of magnitude in the variation range, or (iii) several low-resolution ADCs, each one with a fixed measurement range perfectly adapted to the variation range of one indirect measurement. The retained solution obviously strongly depends on the case study and will be a tradeoff between the required silicon area and the conversion accuracy.

3) Memory and Arithmetic Unit

A regression model is defined by (i) the function that relates the indirect measurements to the predicted performance and, (ii) a set of coefficient values that parametrizes the regression function. In order to implement an embedded prediction, it is therefore necessary to have memory as well as arithmetic resources. The memory resources are used to store the value of the coefficients established during the learning phase. These values obviously need to be permanently stored in the circuit or the system, which implies the use of a non-volatile memory. Alongside the memory, an arithmetic unit must be included in the circuit or system to perform the calculations defined by the established regression model.

It is important to highlight that performance monitoring of a device in the field is an auxiliary option to improve the reliability of the system, but is not the main core of the application. Therefore, the additional circuitry required to implement the embedded prediction must be minimized. Moreover, the processing time must be minimized in order to maintain the normal operation of the system without disruption. Hence, it is essential to reduce the number of required operations; the choice of the regression model type plays an important role in this aspect.

In the classical implementation of the indirect test strategy for production test, the model accuracy is crucial since binning of devices as good or bad circuits is realized based only on the results of the prediction. To achieve high accuracy, models usually implemented are non-linear models such as Multi-Adaptive Regression Spline (MARS) or Support Vector Machine (SVM) models, or even more sophisticated models based on ensemble methods [11]. However, the use of these types of model is problematic in the context of on-line performance prediction. Indeed, they involve the storage of a substantial number of coefficients as well as the computation of specific non-linear functions that cannot be easily implemented with a standard arithmetic unit. Embedded performance computation based on such models would therefore be consuming both in terms of memory resources and processing time, which is a strong drawback.

An alternative way is to lean on less accurate but easier to implement models, such as Multiple Linear Regression (MLR) models. Indeed, these models involve only basic arithmetic operation and a limited number of coefficients ($m + 1$ for a model with m parameters). Of course, the simplicity of implementation comes at the cost of lower model accuracy. However, in the context of on-line performance monitoring, the accuracy constraint is not as strong than in the context of production test since the objective is just to monitor whether the performance has experienced a degradation and to quantify the order of magnitude of this degradation. This is therefore the choice that is used in this study.

III. CASE STUDY

A. Test Vehicle: RF Transceiver (NXP JN518x)

The test vehicle considered as a case study is an ultra-low power wireless microcontroller supporting Zigbee 3.0 and Thread networking stacks to facilitate the development of home automation, smart lighting and wireless sensor network applications. It includes a 2.4GHz IEEE 802.15.4 compliant transceiver and a comprehensive mix of analog and digital peripherals, as well as an Arm Cortex-M4 core and embedded Flash and RAM memory. It also includes an embedded test infrastructure that involves an analog DC bus allowing to probe various internal nodes of the transceiver (11 nodes) and a 12-bit ADC. The internal nodes might be connected either to two General Purpose Input Output (GPIO) pins, or to the embedded ADC. The general architecture of this product is summarized in figure 3.

Our objective is to monitor the power level delivered by the transmitter, which is an essential performance of the system. This product has been selected for this study because it is equipped with all the necessary hardware to implement embedded performance prediction. Specifically, the indirect measurements (voltage on internal nodes of the transceiver) will be performed using the test infrastructure and digitized by the embedded ADC. They will be transferred to the CPU where they will be processed using the model equation determined during the initial learning phase along with the model coefficients stored in the Flash memory during the production. The result of the prediction will be compared to a predefined threshold and a flag alert will be issued on a GPIO pin if the predicted value is below the threshold.

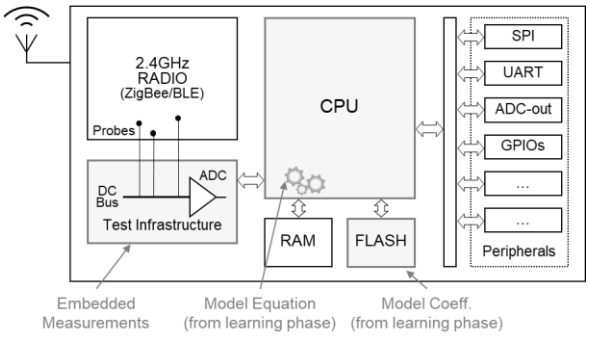

Fig.3: High-level block diagram of the test vehicle

At this point, it is important to highlight that the implementation of an on-line monitoring process was not considered during the design phase of this product. Hence, no specific structures were embedded in the product with respect to the prediction of the transmitted power level, nor with respect to the impact of aging effects. In the same way, the ADC available in the circuit has not been specifically designed for conversion of the embedded measurements. Our objective with this case study is therefore to study the feasibility of implementing on-line performance monitoring based on the indirect test strategy, and we do not expect a high accuracy from the prediction model. The case study should be considered as a proof-of-concept rather than a validation of the efficiency that can be achieved with this approach.

B. Dataset Collection: Measurement Campaign

A measurement campaign has been performed to collect data in order to build a regression model that maps indirect measurements to the level of transmitted power. Ideally, data should be collected on circuits that present a degradation of the power level due to aging effect. However, because it is a new product and the mass-production is not yet launched, we do not have this opportunity. In this context, the solution retained to collect data representative of a power level degradation was to act on two internal configuration registers of the transmitter. Each one of these registers has four configuration bits (16 configurations). By playing on both registers, we therefore have 256 possibilities to operate the transmission block of the device under a different configuration. One of these configurations corresponds to the nominal configuration (C172), and the others are used to emulate a variation of the transmitted power level.

Practically, test data were collected from four ICs on Advantest V93K ATE. Each IC has been operated under the 256 possible configurations and the transmitted power level has been measured using the ATE RF resources, for each configuration. The DC voltage on the 11 internal nodes that can be accessed through the analog test bus have also been measured by the ATE (DC30 to DC40 indirect measurements). In total, the dataset contains 12,288 measurements resulting from 1,024 observations.

Again, it is important to keep in mind that the available IMs have not been specifically defined for the context of this study. Hence, they are not necessarily relevant and it is likely that more pertinent IMs could have been defined during the design phase. Despite the weakness of this dataset, the expectation is that we can build a regression model that predicts the power level with a reasonable accuracy and establish a proof-of-concept for an on-line performance monitoring scheme based on the indirect test strategy.

IV. Initial Learning: Model Elaboration

In this section, the choice of the model type is commented and the procedure for IM selection and model construction is detailed. Results on the accuracy of the retained model to predict the power level variation on IC4 using measurements performed on the ATE are also presented.

A. Choice of Model Type

As mentioned in section II, the choice of a simple MLR model allows to easily implement the required calculations and to minimize the number of coefficients that have to be stored within the circuit. A classical approach to build such a model is based on the use of Sequential Forward Selection (SFS) procedure in order to select the more pertinent IMs [12]. The procedure starts by building an MLR model for each available IM and selecting the IM that generates the model with the minimum prediction error (lowest *RMSE* score). At the second iteration, an MLR model is built for each pair of IMs that includes the previously selected IM; the pair that gives the best model is then selected. The process then continues with triplets and so on.

This procedure has been implemented in this work. However, in order to improve the accuracy of the MLR model, IM selection has been performed on an enriched space of candidates that includes not only the original IMs but also non-linear transformations of these IMs as well as interactions between pairs of IMs, as suggested in [13].

Regarding the non-linear transformations, some transformations such as $1/x$ and x^2 can be implemented at low-cost because they require only a limited number of elementary arithmetic operations. In contrast, other transformations such as $\log(x)$, $\sqrt{x}$ and $\exp(x)$ would require much longer processing times. Indeed, their exact computation is not feasible with elementary arithmetic operations; instead, numerical algorithms that involve many elementary arithmetic operations have to be used to compute an approximation. In this study, we have considered only transformations that can be implemented at low-cost, i.e. $1/x$ and x^2. Regarding the interaction between IMs, all combinations of pairs of IMs using the four elementary operators $(+, -, *, /)$ can be easily implemented. Interactions using $(+)$ and $(-)$ operators are intrinsically present in the model; therefore, only interactions using $(*)$ and $(/)$ operators have been considered in this study.

Globally, with the considered non-linear transformations and interactions, an enriched space of 209 candidates has been generated from the original space of 11 IM candidates.

B. Model Construction

The full dataset of 1024 observations has been partitioned into training and validation sets: the training set includes data collected on IC1, IC2 and IC3 (768 observations) while the validation set is composed of data collected on IC4 (256 observations). The SFS procedure has been applied on the training set and models including between 1 and 10 features have been built to predict the transmitted power level $\hat{P}$. Results have shown that there is no significant improvement in the model accuracy by using more than three features. This is therefore the solution that has been retained:

$$\hat{P} = c_0 + c_1 * \left(\frac{DC39}{DC35}\right) + c_2 * \left(\frac{1}{DC37^2}\right) + c_3 * (DC30 * DC35) \quad (1)$$

where c_0, c_1, c_2, and c_3 are the model coefficients that have to be stored in the Flash memory of the circuit.

It can be observed that this model exploits both non-linear transformations and interactions between IMs. It involves the measurement of four IMs, i.e. $DC30$, $DC35$, $DC37$ and $DC39$.

Predicted power level variation $\widehat{\Delta P}_i^j$ is then simply computed with:

$$\widehat{\Delta P}_i^j = \hat{P}_i^j - P_{nom}^j \quad (2)$$

where $\hat{P}_i^j$ is the power level predicted for device j in configuration i and P_{nom}^j is the actual power level measured on the ATE for device j in the nominal configuration.

Prediction results obtained on both the training and validation sets are illustrated in Figure 4, which presents the predicted power level variation with respect to the actual one (power level variation measured on the ATE with RF resources). It can be observed that the regression model performs acceptably well considering the different shortcomings, i.e. the use of a simple linear regression model, the fact that the IMs were not specifically defined for power level prediction and the limited size of the dataset. It can also be observed that there is no discrepancy between prediction

results on the ICs of the training set and the IC of the validation set, which is an unseen IC for the model.

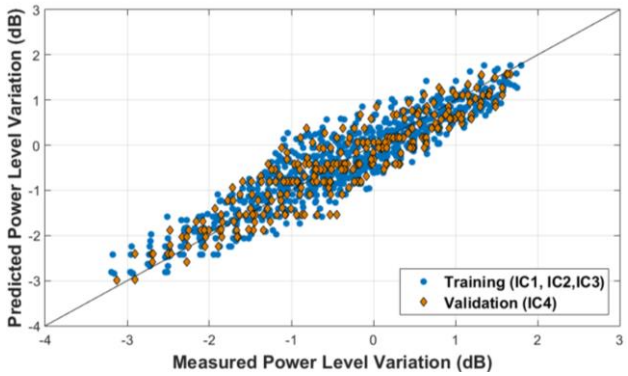

Fig.4: Predicted power level variation vs. measured power level variation

Regarding the prediction accuracy, results are illustrated in Figure 5, which gives the normalized distribution of the prediction error; numerical results are summarized in Table I. Results show that the prediction error is well-centered on 0 and that it follows a nearly Gaussian distribution. The standard deviation is around 0.42dB, which corresponds to a rms accuracy of about 3.7% and the maximum error is around 1.3dB. We can therefore expect that any power degradation stronger than this will be definitely detected by the on-line monitoring process. For lower degradation, detection might be possible but is not guaranteed since we are within the model uncertainty.

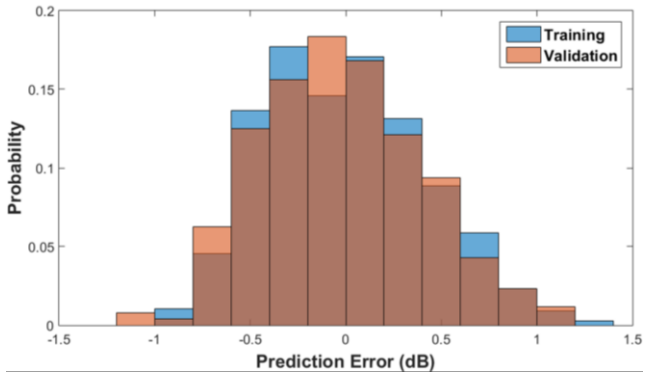

Fig.5: Normalized distribution of the prediction error

TABLE I. STATISTICS OF THE PREDICTION ERROR OVER THE 256 CONFIGURATIONS

	All configurations		
	Mean (dB)	Std. Dev. (dB)	Max (dB)
Prediction error -Training	0.00	0.42	1.30
Prediction error - Validation	-0.02	0.42	1.19

V. EMBEDDED PREDICTION

This section is dedicated to the practical implementation of the on-line monitoring process. More precisely, the regression model elaborated in the previous section from ATE measurements on IC1, IC2, and IC3 is exploited to perform embedded prediction of the power level variation on IC4. The experimental setup is first described and hardware measurement results are then presented.

A. *Experimental Setup and Product Programming*

To emulate the operation of the circuit within its application environment, the circuit is mounted on a development board provided by NXP Semiconductors. MCUXpresso Integrated Development Environment (IDE) is used to develop the software code on a PC. A stand-alone debug probe is then used to download the code within the product and debug the firmware through a JTAG interface. A specific code dedicated to the on-line performance monitoring process has been developed. The flowchart of this code is illustrated in Figure 6.

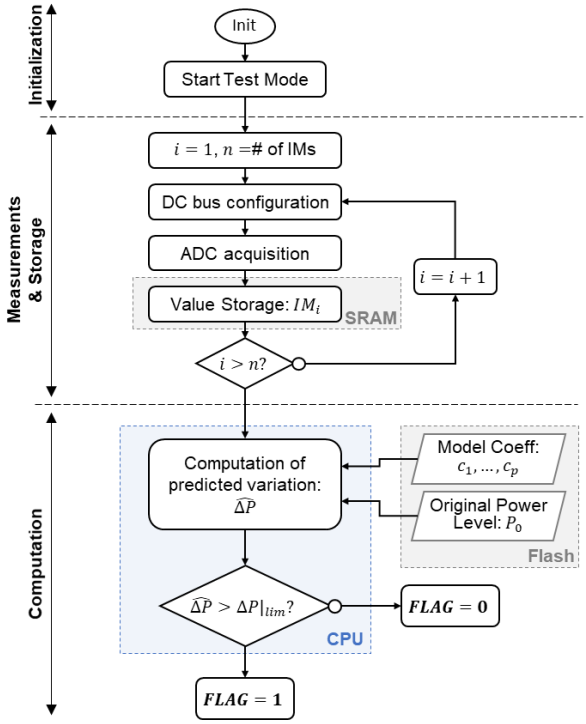

Fig.6: Flowchart of the on-line monitoring process

The code is divided in three main stages. In the first stage, the product is initialized and the Test Mode is started. In this mode, the transmitter is activated and delivers a modulated RF signal at 2.4GHz corresponding to internally-generated DSSS sequences. Once the circuit is ready, the second stage dedicated to the embedded measurements is launched. In this stage, we loop through the selected indirect measurements in order to measure and store their value. More precisely, for each selected indirect measurement, the DC bus is reconfigured, acquisition is realized by the ADC and the digitized value is stored in the SRAM memory. Finally, the last stage is dedicated to the embedded computation and the verification of the performance. In this stage, the predicted power level degradation is computed based on the model equation established during the learning, the measured IM values stored in the SRAM memory, the model coefficients and the original power level stored in the Flash memory. This value is then simply compared to a predefined threshold and a flag is raised if the value is below the threshold, indicating that the product has experienced a degradation.

Note that for validation purposes, a number of outputs that correspond to different stages have been included during the execution of the code, i.e. the digitized value of the embedded measurements, the predicted power level and the status of the

flag alert. These outputs can be transferred to the PC via the USB interface and extracted with the help of the IDE. In the final version of the code, the only output will be the alert flag. Also note that averaging has been implemented for the embedded measurements in order to improve the measurement resolution of the ADC, especially for IMs that exhibit a very small variation range.

B. Results

The specific code dedicated to the on-line performance monitoring process has been launched on IC4 under five different configurations of the device, i.e. the nominal configuration (C172) and 4 other configurations (C12, C132, C241, C246) spread across the power level variation range observed in the collected dataset.

Results are illustrated in Figure 7, which shows the power level variation predicted from the indirect measurements versus the actual power level variation (measured on the ATE with RF resources), for the five configurations. Two values have been computed in each configuration, using either the original indirect measurements collected on the ATE or the embedded measurements performed within the circuit. Numerical values of the prediction error observed for the five configurations are summarized in Table II.

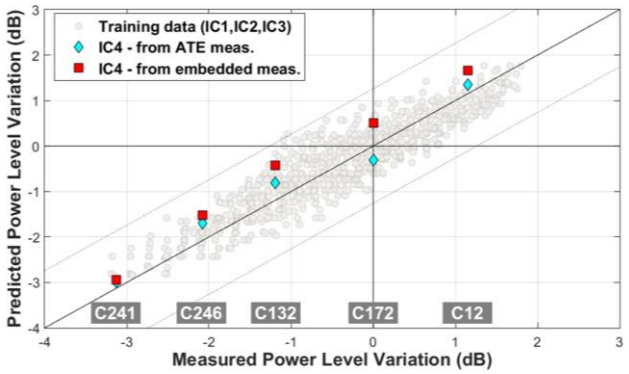

Fig.7: Predicted power level variation vs. measured power level variation for IC4 in five different configurations

TABLE II. SUMMARY OF PREDICTION ERRORS ON IC4 IN FIVE DIFFERENT CONFIGURATIONS

	Prediction Error	
	Using ATE meas. & computation on PC	Using embedded meas. & embedded computation
C172 (nom.)	-0.31 dB	+0.50 dB
C12	+0.20 dB	+0.52 dB
C132	+0.39 dB	+0.76dB
C241	+0.38 dB	+0.56 dB
C246	+0.15 dB	+0.18 dB

Looking at these results, it can be observed that the predicted power level variation is in good agreement with the actual one. It exists a difference between the values predicted using the original indirect measurements collected on the ATE and the one measured within the circuit, certainly related to a difference in the measurement accuracy, but the prediction error remains within the model uncertainty (symbolized by the dotted lines located at $\pm 3\sigma$ around the ideal line in figure 7). Overall, these results establish a proof-of-concept of the proposed on-line performance monitoring scheme.

VI. CONCLUSION

In this paper, we have explored an adaptation of the indirect test strategy for on-line RF performance monitoring. The principle involves an initial learning phase on a set of training devices in which a regression model is established between the RF performance to the monitored and some indirect measurements that can be measured on-chip. Then at production time, the model coefficients as well as the original performance value are stored within the circuit for any new fabricated device. Finally, once the device is deployed in its application, the on-line monitoring process can be launched at any time. It involves the embedded measurement of the selected IMs and the embedded computation of the performance variation.

The model and hardware requirements to implement this approach have been discussed. The approach has then been demonstrated on a practical case study and results have shown that on-chip monitoring of the transmitted power level is feasible. The main limitation of this investigation is that the indirect measurements available on this case study were not specifically defined for prediction of the transmitted power level, nor with respect to the impact of aging effects. Future work will address these aspects.

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