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Exploring an On-Chip Sensor to Detect Unique Faults in RRAMs

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***Abstract*—Memristive devices have become promising candidates to complement and/or replace the CMOS technology, due to their CMOS manufacturing process compatibility, zero standby power consumption, high scalability, as well as their capability to implement high-density memories and new computing paradigms. Despite these advantages, memristive devices are also susceptible to manufacturing defects that may cause different faulty behaviors not observed in CMOS technology, significantly increasing the manufacturing test complexity. This work proposes a Design-for-Testability (DfT) strategy based on the introduction of a on-chip sensor that measures the current consumption of Resistive Random Access Memories (RRAMs) cells to provide the detection of unique faults. The new On-Chip Sensor (ON_CS) was validated using a case study 3x3 RRAM cell array with peripheral circuitry implemented based on a 130 nm Predictive Technology Model (PTM) library. Experimental results show that the proposed DfT strategy is able to detect not only traditional faults, but also unique faults that can affect RRAM cells. Finally, this paper proposes an DfT strategy that can detect unique faults with an unique operation and can be used during the normal operation of a RRAM.**

***Index Terms*—RRAMs, Testing, Unique Faults, On-Chip Sensor**

I. Introduction

During the last five and a half decades, CMOS technology miniaturized according to Moore's law, which predicted that the number of transistors per silicon chip doubles every eighteen months [1]. However, this became a challenge to be continued, due to limitations on the continued transistor miniaturization and the increasing demand for emerging applications requiring high-performance systems with strict constraints posing significant challenges to device technologies and computer architectures. From the point of view of device technology, the reliability, leakage, and cost walls are identified [2], [3]. Moreover, the memory, power, and Instruction Level Parallelism (ILP) walls are affecting computer architectures. Thus, memristive devices represent one of the most promising candidates to complement and/or replace CMOS technology, in some applications such as Flash memory, mainly due to their CMOS manufacturing process compatibility, and zero standby power consumption, as well as high scalability and density [3]. In addition, these devices can be used not only as a memory but also as computing elements. However, the use of these devices depends on being able to guarantee their reliability after manufacturing, and during lifetime. Considering that new devices came with new materials, manufacturing process, and expected behavior, it leads new defects, which causes new faults, limiting the dependability of the device. In this context, it becomes mandatory to properly test these devices after manufacturing, and during lifetime. Despite the lack of information regarding realistic manufacturing deviations, literature already describes that Resistive Random Access Memories (RRAMs) can be affected by unique faults [4]–[6], consequently demanding the development of new manufacturing test procedures [7], [8]. In [9], the authors provide a review of the memristive device manufacturing process and a discussion related to the possible defects that may affect these novel devices, identifying the relation between manufacturing failure mechanisms and faulty behaviors. Also, in the last few years, some manufacturing test strategies were proposed in the literature. A Design-for-Testability (DfT) scheme that exploits the access time duration and supply voltage to facilitate the detection of unique faults in RRAMs was presented in [10]. Traditional March Tests that explore the execution of predefined read and write operations applied at each RRAM cell are extremely time-consuming and are also not able to guarantee the detection of all unique faults. In [11] the authors presented a scheme based on "sneak-path sensing" able to test multiple elements of Phase Change Memories (PCM) at the same time. The detection is based on a comparison between the output current related to a specific group of cells and the ideal current, accessed based on the execution of March elements. The main drawback of this scheme is that it only works for RRAMs that have sneak-paths. In short, there is no efficient test solution that can detect all unique fault in RRAMs.

This paper investigates the fault detection capability of a DfT strategy for testing RRAM cells after manufacturing. In more detail, the main contributions of this paper are: (1) Propose an optimized on-chip sensor able to detect unique faults in RRAMs. Note that this work is an evolution of the strategy presented in [12]; (2) Demonstrate the DfT strategy's effectiveness based on a case study composed of a 3x3 RRAM implemented using a 130nm Predictive Technology Model (PTM) library and a memristive model described in [13], [14]. The case study also helps to demonstrate the flexibility of the proposed strategy with respect to implementation granularity; and (3) Provides a discussion related to the main introduced overheads as well as the impact of process variation on the

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resolution of the on-chip sensor. Finally, it is important to mention that the validation of the proposed approach was performed by adopting a defect injection scheme called Defect Oriented (DO)model [8] [14].

The remaining of this paper is structured as follows. Section II presents the background related to memristive devices, defect injection schemes and fault models. Section III describes the proposed DfT strategy. In Section IV the description related to the experimental setup is provided and Section V summarizes the main obtained results including a discussion about overheads and process variation impact. Finally, in Section VI we draw the conclusions.

II. Background

This Section introduces the main concepts regarding memristive devices and describes the existing fault models and the defect injection scheme used in this work.

A. Memristive Devices

In 1971, Leon Chua postulated the fourth basic circuit element named memristive device, or memristor, while trying to establish a missing constitutive relationship between electrical charge and magnetic flux [15]. A memristive device is a passive element that can be described by the time integral of the current (charge q) through the time integral of the voltage (flux ϕ) across its two terminals [15]. The memristive device has at least two distinct states, the High Resistance State (HRS) and the Low Resistance State (LRS), and can switch from HRS (LRS) to LRS (HRS) by applying a voltage V_{SET} (V_{RESET}) with an absolute value larger than its threshold voltage (Vth). The essential fingerprint of memristive devices is the pinched current-voltage (I-V) hysteresis loop [15].

B. Fault Models

Like any other device, memristive devices are prone to manufacture deviations, including process variation and manufacturing defects, that can result in faults [16]. Note that the integration of CMOS-based circuits with memristive devices is performed during the Back-End-Of-Line (BEOF) manufacturing process. These defects need to be properly modeled in order to guarantee an accurate identification of possible faulty behaviors. A fault is defined as any deviation from the memristor's expected behavior due to process variations, manufacturing defects, or design-induced anomalies [16]. The fault size is related to the deviation's magnitude and can be categorized into three different classes. A deviation higher than the tolerance limit is classified as catastrophic. However, if the deviation only degrades the performance, it is categorized as parametric. Finally, if the deviation's magnitude is insignificant, the fault is called benign [16]. According to literature, an RRAM cell can be affected by faults that are also present in traditional fault models associated with classic memory cells [5]. In more detail, the fault models related to RRAMs can be initially classified into two categories: (a) Conventional and (b) Unique [17]. The unique faults that can affect RRAMs are: (1) Undefined Write Fault (UWF) [8], after a writing operation

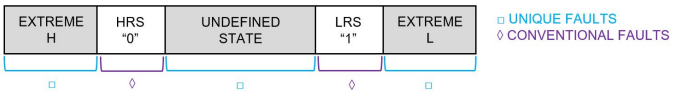

Fig. 1. Unique fault model: faulty resistance intervals of memristive devices [12].

the cell is brought into an undefined state 'U' between '0' and '1', HRS and LRS; (2) Deep State Fault (DeepF) [18], the resistance in the cell is beyond the boundaries for each state of the cell; and finally, (3) Unknown Read Fault (URF) [8], [19], the read operation results in unknown data, which means a random logic value at the output, independent from the reading conditions. A URF can occur when LRS and HRS are close to each other or when a state 'U' is stored in the cell. Note that the state 'U' needs to be detected because it indicates misbehavior in the memristor. Fig. 1 depicts the faulty resistance intervals of memristive devices, the regions highlighted in blue represent emerging faults associated with the unique fault model [12].

C. Defect Injection Scheme

To simulate these conventional and unique faults, methods for injecting a defect in a RRAM cell are needed. The closer the simulation is to the real behavior of the defect, the better the simulation results will match the final circuit. So a good defect injection scheme for an RRAM cell is the key to usable simulation results. At the moment two defect models are established, the Resistive Defect (RD) model and the Defect Oriented (DO) model. The RD model introduces a resistor at one point in the cell to simulate a proper defect, for example, a resistor in series to model the 'U' state during read '1' and a parallel resistor for read '0'. As mentioned in [8], this model is not able to simulate the nonlinear behavior of RRAM cells and will lead to imprecise simulation results. Note that the resistance values correspond to the strength of the defects [17]. In comparison, the DO model keeps the nonlinearity of the memristor device and is closer to the real behavior of a defective RRAM cell. The DO model focuses on changing parameters in the memristive device itself to simulate faulty behaviors [8]. Therefore a better understanding of the model's internal behavior and the memristor itself is needed. In this work, the faulty behavior of a RRAM cell will be modeled by changing the parameters for the oxygen vacancy concentration in the disk of the memristor model (*Nreal*). This method is proposed in [20]. By increasing the lowest possible concentration of oxygen vacancies (*Ndiscmin*) the resistance in the HRS is lowered because the current that can flow through the device is higher with a higher *Ndiscmin*. The same effect occurs when the highest possible concentration of oxygen vacancies in the disk (*Ndiscmax*) is decreased. The current flowing through the device will decrease leading to higher resistance in LRS. This method makes the simulation of a device in an undefined state, while keeping its memristor-like behavior possible.

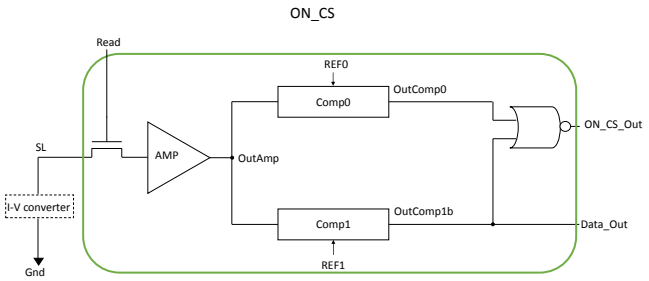

Fig. 2. Block diagram of the proposed ON-CS including the read circuitry.

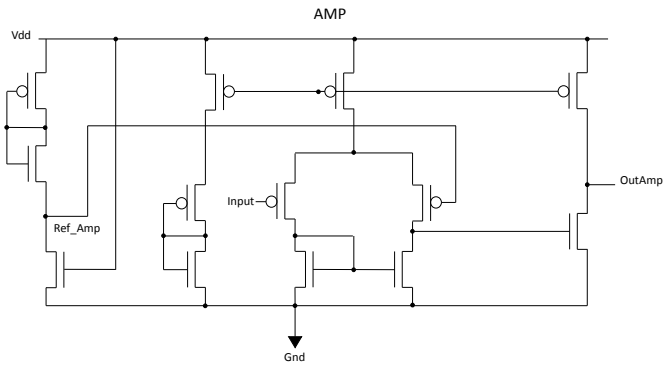

Fig. 3. Schematic view of the designed Amplifier (AMP).

III. The Proposed DFT Strategy

The DfT strategy proposed in this paper is based on the introduction of an On-Chip Sensor (ON_CS) able to measure the current that flows through the RRAM cells while performing a predefined operating sequence. Fig. 2 depicts the block diagram of the proposed ON_CS. In general terms, the ON_CS is composed of an access transistor, an operational amplifier (AMP), two comparators (*Comp0* and *Comp1*) and a NOR logic gate. Note that the I-V converter is part of the Select Line-driver (SL-driver) and generates the voltage variation related to the memristor's current. This voltage variation is amplified and used by *Comp0* and *Comp1*.

It is important to mention that a low current will flow through the memristive device if the RRAM cell stores a HRS and consequently a low voltage variation with respect to *Gnd* will be observed. This voltage variation will be compared to *Comp0* and *Comp1* in order to indicate a possible faulty behavior that will be indicated in *OutAmp*. The non-inverted output of the two comparators is '1' if the input voltage is higher than the reference voltage and '0', if the opposite situation occurs. For the detection of an UWF, the measured voltage has to assume a value between the two reference voltages (REF0 and REF1). In that case, *OutComp0* and *OutComp1b* will both generate a '0'. The output of the NOR logic gate will assume a '1', indicating the detection of an UWF. Note that *OutComp1b* is also used as *Data_Out*.

It is important to highlight that the implementation of the AMP is based on these references [21]–[24]. Fig. 3 shows the electrical schematic view of the implemented AMP. In general terms, AMP has three transistors on the left side that are forcing the *Ref_Amp* node to a small voltage that is used as an internal reference for one side of the differential amplifier. The *Input* signal of the AMP arrives from SL through the access transistor. The higher the voltage difference between the *Input* and the *Ref_Amp*, the bigger the voltage connected to the gate of the nMOS that is connected to the output. The voltage in the gate will open the transistor and pull the output node to the *Gnd*. The output voltage becomes smaller with higher differences between the input voltage and the reference voltage (*Ref_Amp*). To resume, the input signal is inverted and amplified.

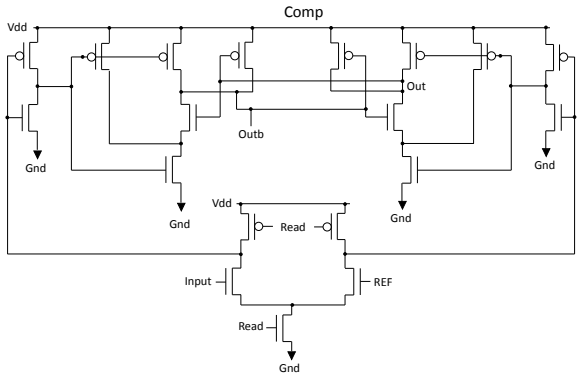

Fig. 4. Schematic view of the designed Comparator (*Comp0* and *Comp1*).

Finally, *Comp0* and *Comp1* are implemented based on a double-tail dynamic comparator [25]. Fig. 4 depicts the comparators' electrical schematic view. During the pre-charge phase, when the Read signal is low, the pMOS transistors of the input stage are opened and will pre-charge the node connected to the inverters' gates between the input and the output stage. When the Read signal is '1' the capacitance of the node is discharged to the ground through the input transistors. Depending on the input voltage, one of the nodes will be forced to (*Vdd-Vth*) faster, which will turn off the inverter's nMOS. If the voltage in the Input is bigger than REF, *Out* will be pulled to *Vdd*, and *Outb* is forced to *Gnd*. If the input voltage is smaller than REF the outputs will have the opposite behavior. Once the output decision is made, the outputs will keep their respective output values until Read becomes '0' again. At this point, the comparator is back to the pre-charge phase. Since the comparator works dynamically, the input voltage must be in full swing at the moment the Read signal activates the decision phase of the comparator.

IV. Experimental Setup

In order to validate the proposed DfT strategy and demonstrate the fault detection capability of the ON_CS, a case study composed of a 3x3 RRAM array, including peripheral circuitry, was adopted. The case study and the ON_CS were implemented using a 130nm Predictive Technology

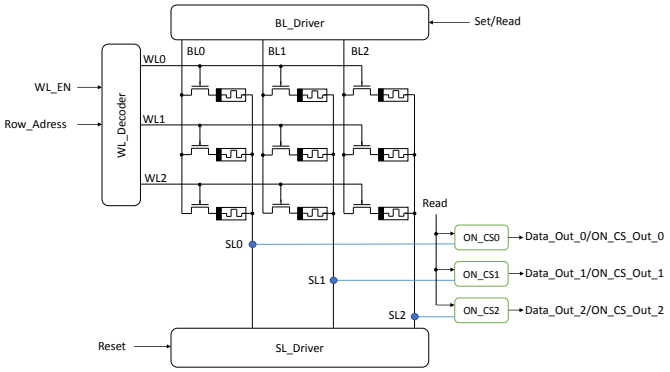

Fig. 5. Adopted case study: RRAM and ON_CS.

Model (PTM) for the CMOS-based circuits and the RRAM ($Pt/HfO_2/TiO_x/Pt$) compact model proposed in [13], [14]. Fig. 5 shows the block diagram of the adopted case study including one ON_CS per each RRAM column. Note that all words on one row share the Word Line (WL), while all words in one column share the Bit Line (BL) and the Select Line (SL). In this specific case study, every word consists of one single RRAM cell (1T1R), storing one bit of data each. Each BL is connected to a capacitance of 150 fF, emulating a larger RRAM for more realistic simulation results. The single RRAM cell is composed of one Transistor (1T) to control the current that flows through the memristor (1R), as shown in Fig. 6. The peripheral circuitry implements the read and write logic. The column address decoder selects the desired column, based on the column address (COL). Similarly, the WL-decoder selects the WL that corresponds to the desired row address, once the WL enable (WL_EN) signal is set. BL and SL drivers act to allow write and read operations on the block, varying its voltage accordingly with the target operation. When a write operation is performed, a RESET operation is performed first on the selected word. This RESET operation is performed by driving the SL to V_{reset} and the corresponding BL to *Gnd*. When the data to be written is a '1', a SET operation is performed subsequently on that cell only. This is done by setting the BL to V_{SET} and the SL to *Gnd*. This writing scheme ensures that the cells are not over-SET, which may lead to low-reliability [26]. For the read operation, the block works similarly with the SET operation, however, the BL is biased to V_{read} and the SL to *Gnd*. Finally, the adopted voltage for performing a *write '1'* operation, or in other words a SET operation, is equal to 1.6 V, which is the nominal voltage adopted in the entire circuit. The RESET operation (*write '0'*) is performed by applying a voltage of -1.7 V, and a read operation is performed applying a small voltage of 0.16 V. Note that one version of this block was presented in the previous work in [27], with the difference that the SL is connected via the rows instead of columns, because in the original circuit is not possible to read the memristor row by through the SL node.

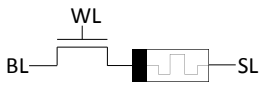

Fig. 6. 1T1R RRAM cell.

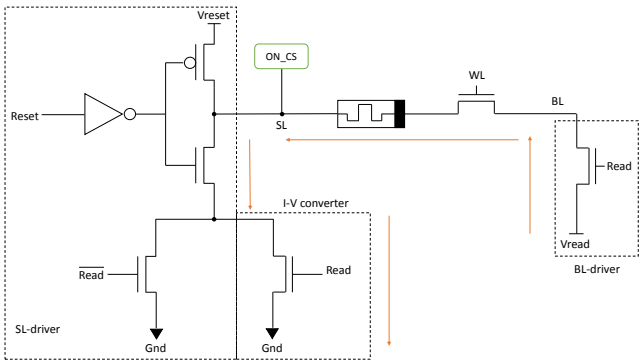

Fig. 7. Case Study: Current flow during the execution of read operations.

Regarding the proposed strategy's implementation granularity, an ON_CS per RRAM column was introduced and connected using SL. The ON_CS is activated by the *Read* signal and has two output signals, *Data_Out* and *ON_CS_Out*. It is important to mention that the original RRAM block's Sense Amplifier was modified since the ON_CS requires a special circuitry during a read operations [27]. During a read operation, the BL-driver applies the V_{read} on the selected RRAM cell and SL-driver set *Gnd* to SL. Fig. 7 shows the current that flows through the RRAM cell during the execution of a read operation. The *Reset* signal is used in '0' and the WL in '1'. Note that the pull-down of the SL-driver has two nMOS transistors, a small transistor used during reading and a larger one during the execution of write operations. This difference between the two nMOS transistor sizes guarantees a strong '0' during SET operations and a weak '0' at SL during reading operations. Thus, the voltage in SL during the execution of reading operations is higher if the RRAM cell is in LRS because the current that flows through the circuit is bigger. The opposite behavior is observed when the RRAM cell stores a HRS. Note that the ON_CS's transistors assume an L of 130 nm and a W from 280 to 3120 nm, depending on their position.

V. Obtained Results and Discussion

The detection capability of the proposed DfT strategy was performed through electrical simulations using Spectre (Cadence). The defects were injected using the DO model, where *Ndiscmin* and *Ndiscmax* values were modified in order to put the RRAM cell in an undefined state, representing an UWF. For this work, the undefined state is represented by resistance values between 10 kΩ and 50 kΩ. Thus, the LRS is represented by a value smaller than 10 kΩ and the HRS by more than 50

TABLE I
BOUNDARIES OF STATES DETERMINED BY N_{real}.

States	Parameters	Upper Limit	Lower Limit
HRS	$N_{real}(\times 10^{26} m^{-3})$	0.008	0.014
	Resistance (kΩ)	112	54.4
'U' State	$N_{real}(\times 10^{26} m^{-3})$	0.015	0.065
	Resistance (kΩ)	49.9	10.1
LRS	$N_{real}(\times 10^{26} m^{-3})$	0.066	20.00
	Resistance (kΩ)	9.99	1.61

kΩ. These limits are represented by the N_{real} parameter that is limited by *Ndiscmin* and *Ndiscmax* parameters [14]. Table I summarizes the range of values of N_{real} parameter adopted to represent HRS, LRS, and the resulting value representing an undefined ('U') state in the RRAM cell. Table I also includes the range of resistance value equivalent to each N_{real} value adopted for indicating the three possible states. When it is intended to simulate an Undefined State, the *Ndiscmax* and *Ndiscmin* parameters can be modified to the Upper and Lower Limit from Table I. Observing Table I it is possible to see that the variation of N_{real} is not linear when compared with the resistance value. A variation of $0.007 \times 10^{26} m^{-3}$ is enough to cause a resistance variation from 112 kΩ to 54.4 kΩ. To resume, a small variation in the N_{disk_min} value makes the device not able to switch to HRS. A complete study about the impact of electrical parameters variation on the memristive device behavior is published in [27]. Moreover, REF0 was set to 1.3 V and REF1 to 0.70 V.

Fig. 8 demonstrates the detection capability of the proposed DfT strategy. In more detail, Fig. 8(a) and Fig. 8(b) depicts the current and the voltage on the SL node when performing the following read operations: *read0* (HRS) with equivalente resistance on memristor of 100 kΩ, *read1* (LRS) with equivalente resistance on memristor of 1.6 kΩ, and *readU* (undefined state) with equivalente resistance on memristor of 49 kΩ, representing an UWF. Fig. 8(c) shows the *OutAmp* signal considering HRS, LRS and undefined state with respect to the two predefined reference voltages (REF0 and REF1).

Fig. 9 depicts the ON_CS_Out. Observing this figure it is possible to see that when the RRAM cell presents a resistance value between 10 kΩ and 50 kΩ, which indicates an undefined state, the ON_CS_Out is high. However, when the RRAM cell works as expected, which means storing a HRS or a LRS, the ON_CS_Out is low. Thus, Fig. 9 demonstrates the detection capability of the DfT strategy with respect to UWF. Note that the resistance range for detection represents one possibility and consequently, the detection limits could be modified by changing the reference voltage values.

To provide a better evaluation of the DfT strategy, an analysis of the process variation impact on the ON_CS was performed through Monte Carlo (MC) simulations. Channel length and width as well as oxide thickness were varied adopting a 3σ Gaussian distribution with variation of 4%. The

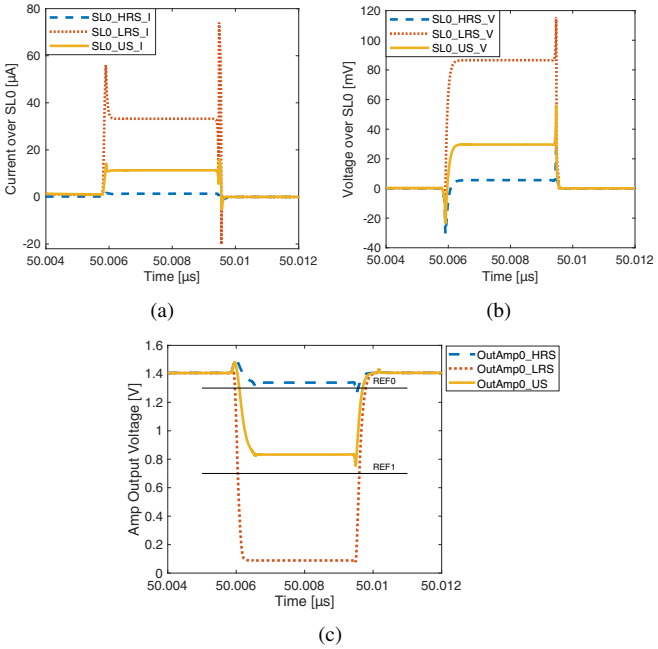

Fig. 8. Comparing a correct read-0 (HRS) and read-1 (LRS) operation with a faulty one (US): (a) Current on the SL0 node, (b) Voltage on the SL0 node (AMP input), and (c) Voltage on the *OutAmp0*, with respect to REF0 and REF1.

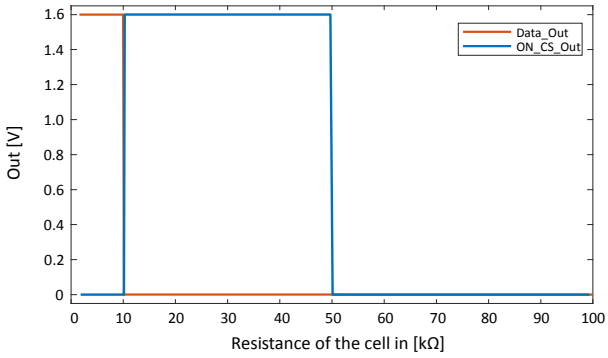

Fig. 9. Data_Out and ON_CS_Out in the presence of an UWF.

ON_CS worked properly in 90 of 100 simulations. Note that the most vulnerable part of the ON_CS is the AMP due to the fact that the calibration of this circuity poses significant challenges and consequently requires extra attention during the design phase.

Regarding the introduced overheads, the power consumption related to the ON_CS is around 1.24 μW, which is not relevant when compared to the power consumption of a RRAM cell, around 48.37 μW. To reduce the power consumption, a power gate transistor could be introduced in order to turn off the supply voltage when the ON_CS is not being used. When considering area overhead, the entire ON_CS requires the introduction of 56 extra transistors. Note that 13 transistors are used for implementing the AMP. Note that this overhead becomes insignificant depending on the number of RRAM

cells in a column. In addition, these overhead could also be minimized exploring the idea of having the SA for reading of the RRAM block also used by the ON_CS. Finally, the implementation granularity of the DfT strategy plays an important role related to overheads and consequently, different schemes can minimize the overheads. Other important aspect is that the proposed ON_CS could be optimized in order to also be used during lifetime to provide detection of in-field faults, increasing the reliability of RRAMs.

VI. Conclusion

This work proposed a DfT Strategy based on a new On-Chip Sensor (ON_CS) for providing the detection of unique faults in RRAMs. In more detail, the ON_CS measures the current that flows through the 1T1R RRAM cell and compares this value with two voltage references in order to provide fault detection capability. The strategy was validated using a case study composed of a 3x3 RRAM cell array, including peripheral circuitry. The obtained results demonstrated that the ON_CS is able to provide the detection of UWFs. Note that the detection of DeepFs can also be assured by adding more reference voltages. The introduction of a variable reference voltage could also be an interesting solution for guaranteeing the detection of all unique faults. As future works, we intend to optimize the AMP and the comparators aiming the reduction of the area overhead associated to the strategy. In addition, we also intend to provide a process variation-aware design of the ON_CS. Finally, we also intend to explore the ON_CS to also perform on-line fault detection during RRAM lifetime.

Acknowledgment

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