IJTAG Compatible Analogue Embedded Instruments for MPSoC Life-time Prediction

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***Abstract*—Decreasing reliability of nanometer CMOS technologies with each technology generation is a bottleneck for development of dependable Cyber Physical Systems. This paper presents two analogue health monitors, namely I_{DDT} and temperature along with their integration to the IJTAG network for MPSoC life-time prediction. The monitors are integrated as embedded instruments in a MPSoC. A technique for dynamic synthesis of the analogue front-end for the I_{DDT} instrument and an architecture for integrating analogue embedded instruments into an IJTAG network is introduced in this paper. The embedded instruments have been designed in TSMC 40nm CMOS technology.**

***Index Terms*—Health monitoring, Embedded Instruments, reliability, I_{DDT}, temperature, IJTAG, IEEE 1687, MPSoC.**

I. Introduction

Nanometer technologies enable the development of Cyber Physical Systems (CPS) with better performance and lower cost per functionality. However, it comes with decreased reliability which is a concern in applications such as automotive, space where the devices are subject to harsh environments for a long time. The decreased reliability due to aging is attributed to various mechanisms such as Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI) etc. which results in threshold voltage (V_{TH}) shift of transistors.

It has been shown [1] that there is a strong correlation between transient power-supply current (I_{DDT}) degradation for various functional units of a processor and NBTI degradation at the transistor level by employing off-chip monitors. Hence, I_{DDT} measurements are a good indicator for monitoring aging. Various on-chip I_{DDT} monitors have been proposed in literature for the purpose of testing digital circuits [2],[3]. The monitor in [2] employs PMOS transistor as the sensing element, whereas [3] uses parasitic resistance of the V_{DD} line for sensing. Temperature is one of the key parameters which accelerate the aging mechanisms and hence decreases the reliability. Therefore, monitoring the temperature in addition to I_{DDT} would give an accurate representation of the aging which can predict [4] the life-time of the system and take preventive action if required. Out of the various temperature sensing mechanisms compatible with CMOS technology, bandgap-based sensors are most popular due to their robust sensing mechanism. The IEEE 1687 standard or popularly known as IJTAG [5] standardizes the access to embedded instruments (EI) which used to be accessed in an ad-hoc manner. Integration of digtial instruments into the IJTAG network has been discussed in [6]. However, in the context of health monitoring of MPSoC, the parameters to be monitored such as temperature, I_{DDT} etc. are analogue in nature. Therefore, analogue monitors also has to be integrated as EIs for effective monitoring and improvement of reliability.

This paper presents the analogue front-ends of two monitors and proposes a methodology for their integration into a Multi-processor System-on-Chip (MPSoC) as EIs accessible via the IJTAG standard. The monitored parameters are temperature and I_{DDT}, which are very effective in life-time prediction. For the I_{DDT} EI, a dynamic technique for synthesis of the analogue front-end by generation of a I_{DDT} independent reference voltage in addition to a linear I_{DDT} dependent voltage signal from the same circuit is introduced. The remainder of the paper is organized as follows: Section II illustrates the schematic deisgn of the two EIs. Section III presents the simulation results and the layout while Section IV discusses the IJTAG integration scheme of the two EIs together with their operation descriptions.

II. Embedded Instrument Designs

The typical front-end of any analogue monitor which has a digital output consists of a parameter-dependent signal and a reference voltage which is independent of this parameter. Both these voltages are required as inputs to a data converter for digitization. In the context of EI designs, the parameters are temperature and the transient current, whereas the references are temperature independent and current independent voltages.

A. The I_{DDT} Monitor Front-end

The I_{DDT} monitor proposed here is based on the parasitic metal resistance of the power supply line [3] and an unbalanced current mirror [7]. The circuit in [3] is a detector circuit for test of open defects whereas [7] tests continuity of on-chip power supply distribution network. The proposed monitor advances the ideas in [3], [7] to enable the circuit for I_{DDT} measurement by generation of a linear output voltage

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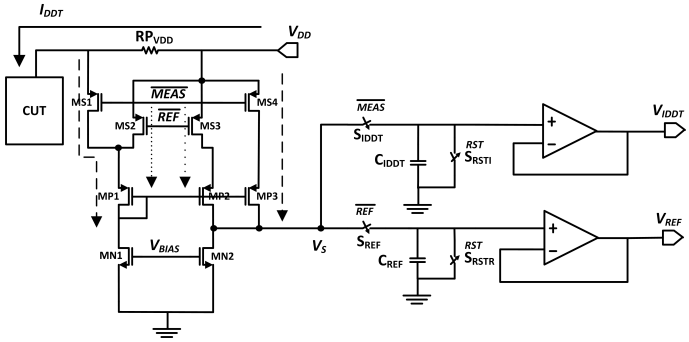


Fig. 1. Schematic of the I_{DDT} front-end

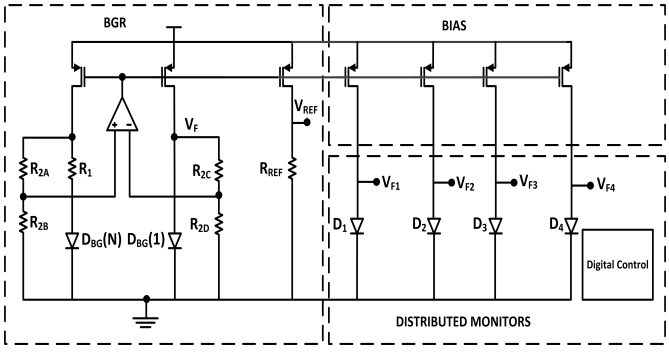


Fig. 2. Schematic of the temperature monitor front-end

and a current independent reference voltage from the same circuit for health monitoring purposes. The circuit can also detect the current shapes in addition to the peaks due to the continuous sampling operation. The circuit is shown in Fig. 1. The principle of operation is as follows. There are two modes of operation : the reference generation mode and the monitoring mode. Transistors MP1, MP2 and MP3 are current-mirror transistors. However, MP1 and MP2 are balanced meaning they have the same W/L ratio, whereas MP1 and MP3 are unbalanced meaning their W/L ratios are different (MP3 W/L less than MP1 W/L by a factor of K). MN1 and MN2 are current source transistors biased by V_{BIAS}. Transistors MS1-MS4 act as switches to change the mode of operation. In the reference generation mode, the switches MS2 and MS3 are closed and the CUT current does not affect the current mirror operation. Therefore, node voltage V_S remains constant irrespective of the CUT current and acts as the reference voltage. This voltage is sampled on to the capacitor C_{REF}. In the measurement mode, switches MS1 and MS4 are closed and hence the current mirror is unbalanced due the lower W/L ratio of MP3. This brings the voltage of node V_S to a value lower than the reference depending on how unbalanced the current mirror is. However, there is a difference in V_{GS} voltage of MP1 and MP3 due the CUT current. The CUT current brings the node V_S higher and closer to the reference volatage linearly as shown below:

$$v_s = g_m \left(I_{DDT} \cdot RP_{VDD}\right) \left(\frac{1}{K} \cdot \frac{W}{L}\right) rout \qquad (1)$$

where g_m is the transconductance of MP1, K is ratio of W/L of MP1 and MP3, RP_{VDD} is the parasitic resistance of the V_{DD} line and $rout$ is the output resistance at node V_S. The voltage V_S in measurement mode is sampled onto the capacitor C_{IDDT}. The dynamic range of the current sensed is set by the unbalance ratio K of the current mirror and the sensitivity is set by RP_{VDD}. Thus, with the reference voltage and I_{DDT} dependent voltage we have the complete front-end for the monitor.

B. Front-end of the Temperature Monitor

The temperature monitor we used is based on bandgap principle. Fig. 2 shows the EI schematic. The sensing devices D_1, D_2, D_3, D_4 are pdiff-nwell diodes which are available as parametric cells in our 40nm process. The devices are distributed at various locations of the core based on the thermal profile for typical workloads [8]. The reference voltage V_{REF} is generated by a bandgap reference (BGR) which is a low-voltage design [9] for sub-1V operation and does not use any special V_{TH} devices. The low voltage is enabled by a combination of a current mode approach and shifting the op-amp inputs between R_{2A}, R_{2B} and R_{2C}, R_{2D} respectively. $D_{BG}(N)$ and $D_{BG}(1)$ are diodes biased at different current densities by virtue of their area ratio of 1:N (N=8). The response of the diodes has a complementary to absolute temperature (CTAT) characteristic. The CTAT voltage V_F and the temperature independent reference voltage V_{REF} [9] are given by:

$$\begin{aligned} V_F &= \frac{kT}{q} ln(\frac{I}{I_S}) \\ V_{REF} &= \frac{R_{REF}}{R_1}\left[V_F + \frac{R_2}{R_1} \cdot \frac{kT}{q} \cdot ln(N)\right] \end{aligned} \qquad (2)$$

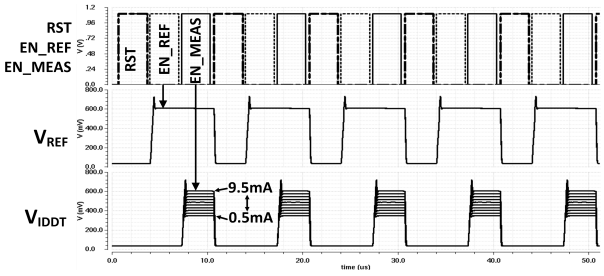
where I is the bias current for the diodes and $R_2 = R_{2A} + R_{2B} = R_{2C} + R_{2D}$. Thus, with V_F and V_{REF}, one has the complete front-end of the temperature monitor available.

III. Simulation Results and Layout

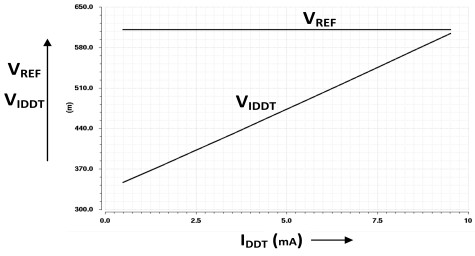
The health monitor front-ends are being implemented in 40nm TSMC CMOS process. For effective monitoring the design of health monitors must be robust to aging. Hence, the circuits are also simulated including aging models [10] which takes into account the NBTI effects. Unlike the MPSoC, the EIs are not in continuos operation and hence the impact of aging is considerably less. In additon, sensors are designed with calibration mechanisms to mitigiate the performance drift due to aging.

A. The I_{DDT} Embedded Instrument

Fig. 3a shows the transient simulation results of the I_{DDT} monitor for a range of currents from 0.5mA to 9.5mA superimposed . *EN_REF*, *EN_MEAS* and *RST* are the control signals for the monitor which are non-overlapping. *EN_REF* enables the reference generation mode by turning on the transitors MS2, MS3 and switch S_{REF}. *EN_MEAS* enables the reference



(a) I_{DDT} transient simulations



(b) Sampled reference and measured voltage of I_{DDT}

Fig. 3. I_{DDT} simulation results

generation mode by turning on the transitors MS1, MS4 and switch S_{IDDT}. *EN_REF* and *EN_MEAS* also act as sampling clock for the reference voltage and measurement voltage. The sampling frequency is 100kHz which is designed to be a sub-multiple of the processor frequency which is sufficient to obtain the I_{DDT} response as long as both are in phase. The *RST* signal resets the sampling capacitors C_{REF} and C_{IDDT} before each reference and measurement sampling operation. Fig. 3b shows the sampled measured (V_{IDDT}) and reference voltage (V_{REF}) from Fig. 3a for I_{DDT} currents from 0.5mA to 9.5mA. As can be seen from the figure, we have a linear response for the measured voltage (1) and the reference voltage is independent of the I_{DDT} current. For a reference voltage of 0.6V and a 10-bit ADC the calculated resolution is 17µA. The monitor is subject to process variation and hence requires calibration. A first-order correction can be accomplished by measuring the ouput voltages at two different DC currents and subsequently calculating the slope. The slope and the voltage at one of the currents are written in the on-chip memory as calibration parameters. These calibration parameters are then read for I_{DDT} computation in the measurement mode.

B. The Temperature Embedded Instrument

Fig. 4 shows the DC simulations of the temperature monitor from 25°C to 125°C. As seen from the figure, the forward voltages V_F and $V_{F[1:4]}$ (distributed monitors) has a CTAT linear characteristic and the reference voltage V_{REF} is independent of temperature; it shows that the temperature coefficient cancellation of PTAT and CTAT currents have taken place precisely. This has been achieved by the ratio of resistors R_2 and R_1 which cancels the temperature coefficient of V_F. The figure also shows V_{REF} with a scaled axis. The BGR achieves a box model TC of 6.15ppm/°C for the desired temperature range. For a BGR voltage of 0.65V and a 10-bit ADC the

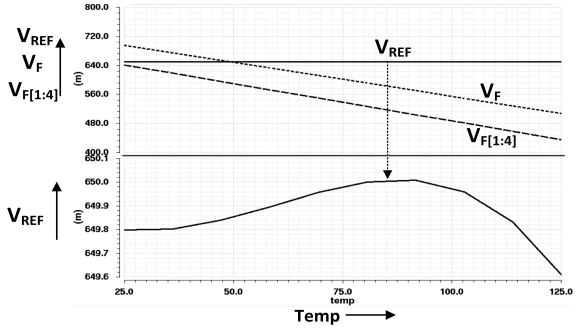


Fig. 4. Temperature monitor DC simulations

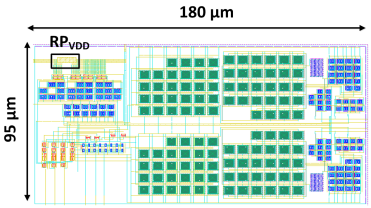
calculated resolution is 0.3°C. Unlike for I_{DDT}, the temperature monitor just requires a one-point calibration. This is due to the well known property that the process variation of the forward voltage drop or base-emitter voltage of a bipolar transistor has just one degree of freedom about the 0K point. Hence, calibration at room temperature is sufficient which reduces the test cost. For the temperature monitor, there is just one calibraton parameter which is the slope of the CTAT voltage.

C. Layouts of the embedded instruments

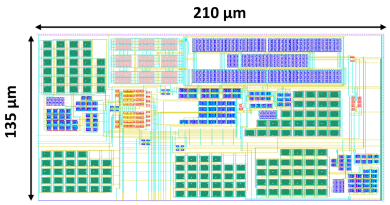
Fig. 5a shows the layout of the I_{DDT} monitor which occupies a die area of 0.017mm^2. Fig. 5b shows the layout of the temperature monitor which has an area of 0.028mm^2. The two monitors also include buffers for driving off-chip loads(for evaluation purposes), hence the core layout area is further less. Fig. 5c shows the layout of the distributed monitors which is an array of pdiff-nwell diodes. Four monitors are distributed in various parts of the core, each of which occupy an area of 0.0012mm^2. To minimize the error sources for temperature monitor layout design, particular emphasis has been taken to match the various components such as the bias current transistors and the BGR resistor ratios. Common-centroid layout technique has been employed to improve the matching. For I_{DDT} EI design, the parasitic metal line resistance labelled RP_{VDD} in Fig. 5a has a value of 1Ω. Kelvin connections have been implemented in the layout on either side of the monitoring resistor to mitigate the error due to IR drop.

IV. IJTAG Integration

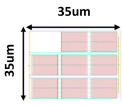
The interface between the health monitors and the IJTAG network is via Test Data Registers (TDR). Segment Insertion Bit (SIB)s are introduced in the standard to enable dynamic reconfiguration of the network depending on which instrument is accessed. A Write-Only TDR is used for configuring the EIs and Read-Only TDRs are the digital outputs and status bits of the EIs. Fig. 6 shows the proposed architecture for analogue monitor integration onto the IJTAG network along with various digital monitors. For the temperature EI, while the Write-Only TDR consists of select bits for the distributed PN-junction to be monitored, calibration and measurement enable bits; the Read-Only TDR consists of digtial output bits *DOUT_TEMP* and the End of Conversion (EOC) status bit *EOC_TEMP*.



(a) Layout of I_{DDT} EI



(b) Layout of temperature EI



(c) Distributed diode layout

Fig. 5. Layout of the I_{DDT} and temperature EIs

For the I_{DDT} monitor, the configuraton bits which enable the calibration and measurment modes are part of the Write-Only TDR, whereas the Read-Only TDR consists of digital output bits *DOUT_I$_{DDT}$* and the EOC bit *EOC_I$_{DDT}$*.

The IJTAG standard is currently only applicable for digital signals and hence direct integration of analogue monitors with voltage outputs is a bottleneck. Digitization of analogue signals could be achieved by sharing a multi-channel ADC which is ubiquitous in CPS. The analogue monitor front-ends share the multi-channel ADC which writes the digital output of each monitor to the respective TDRs. This approach makes the analogue monitor integration more efficient and optimizes the chip area. The inputs to the ADC (*AIN_TEMP*, *VREF_TEMP*, *AIN_I$_{DDT}$*, *VREF_I$_{DDT}$*) for both the instruments are the outputs of the analogue front-ends which are described in Section II. For the EI designs, TDRs have been daisy chained for simplicity. The instruments are designed to be operated in two modes of operation: measurement mode and calibration mode. The modes are set by the configuration bits *CONFIG_TEMP* and *CONFIG_I$_{DDT}$* for temperature and I_{DDT} EI respectively. When the measurement configuration bit is enabled for the instrument, the instrument asserts the start conversion signal (*SC_TEMP*, *SC_I$_{DDT}$*) to the ADC. The digital output (*DOUT_TEMP*, *DOUT_I$_{DDT}$*) is then written onto the corresponding TDR by the ADC and read out through the IJTAG network. The temperature and I_{DDT} measurements are computed from the calibration parameters and the digital outputs. The EIs have been integrated to a multicore plasma processor designed in the same 40nm technology. For this particular work, off-chip ADC is utilized for prototyping flexibility.

V. Conclusions

In this paper we have presented the design of analogue front-ends of temperature and I_{DDT} monitors in a TSMC 40nm CMOS technology with their integration to the IJTAG network. A design technique for dynamic synthesis of reference voltage and I_{DDT} dependent voltage for I_{DDT} front-end and a methodology for integration of the analogue monitors as embedded instruments into IJTAG networks has been introduced in this paper. The addition of analogue monitors into the IJTAG network would enable holistic health monitoring of the system. In additon, it will further enhance the adaptibility of the standard which has been mostly targeted at digital embedded instruments.

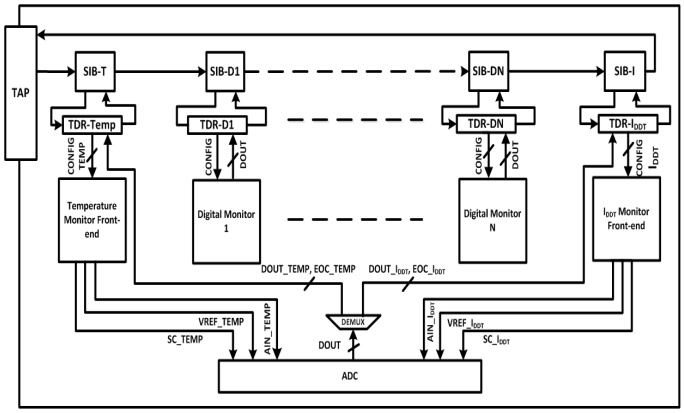


Fig. 6. The IJTAG integration network infrastructure

References

[1] Y. Zhao and H. G. Kerkhoff, "Unit-based functional iddt testing for aging degradation monitoring in a vliw processor," in *2015 Euromicro Conference on Digital System Design*, Aug 2015, pp. 353–358.

[2] G. Gyepes, D. Arbet, J. Brenkus, V. Stopjakova, and J. Mihalov, "An on-chip dynamic supply current monitor for testing of digital circuits," in *2013 23rd International Conference Radioelektronika (RADIOELEKTRONIKA)*, April 2013, pp. 156–161.

[3] V. Stopjaková, H. Manhaeve, and M. Sidiropulos, "On-chip transient current monitor for testing of low-voltage cmos ic," in *Proceedings of the Conference on Design, Automation and Test in Europe*, ser. DATE '99. New York, NY, USA: ACM, 1999. [Online]. Available: http://doi.acm.org/10.1145/307418.307560

[4] Y. Zhao and H. G. Kerkhoff, "Highly dependable multi-processor socs employing lifetime prediction based on health monitors," in *2016 IEEE 25th Asian Test Symposium (ATS)*, Nov 2016, pp. 228–233.

[5] "Ieee standard for access and control of instrumentation embedded within a semiconductor device," *IEEE Std 1687-2014*, pp. 1–283, Dec 2014.

[6] A. Ibrahim and H. G. Kerkhoff, "ijtag integration of complex digital embedded instruments," in *2014 9th International Design and Test Symposium (IDT)*, Dec 2014, pp. 18–23.

[7] H. Manhaeve and S. Kerckenaere, "An on-chip detection circuit for the verification of ic supply connections," in *Proceedings 2001 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, 2001, pp. 57–65.

[8] A. Rohani, H. Ebrahimi, and H. G. Kerkhoff, "A software framework to calculate local temperatures in cmos processors," in *2016 26th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, Sept 2016, pp. 183–188.

[9] K. N. Leung and P. K. T. Mok, "A sub-1-v 15-ppm/ °c cmos bandgap voltage reference without requiring low threshold voltage device," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, Apr 2002.

[10] J. Wan, H. G. Kerkhoff, and J. Bisschop, "Simulating nbti degradation in arbitrary stressed analog/ mixed-signal environments," *IEEE Transactions on Nanotechnology*, vol. 15, no. 2, pp. 137–148, March 2016.