X-ray: Discovering DRAM Internal Structure and Error Characteristics by Issuing Memory Commands

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Abstract—The demand for accurate information about the internal structure and characteristics of dynamic random-access memory (DRAM) has been on the rise. Recent studies have explored the structure and characteristics of DRAM to improve processing in memory, enhance reliability, and mitigate a vulnerability known as rowhammer. However, DRAM manufacturers only disclose limited information through official documents, making it difficult to find specific information about actual DRAM devices. This paper presents reliable findings on the internal structure and characteristics of DRAM using activate-induced bitflips (AIBs), retention time test, and row-copy operation. While previous studies have attempted to understand the internal behaviors of DRAM devices, they have only shown results without identifying the causes or have analyzed DRAM modules rather than individual chips. We first uncover the size, structure, and operation of DRAM subarrays and verify our findings on the characteristics of DRAM. Then, we correct misunderstood information related to AIBs and demonstrate experimental results supporting the cause of rowhammer. We expect that the information we uncover about the structure, behavior, and characteristics of DRAM will help future DRAM research.

Index Terms—DRAM, Rowhammer, Retention test, DRAM subarray

1 INTRODUCTION

The recent trend of exacerbating soft and hard error rates, the advent of processing in/using memory, and the discovery of the ever-worsened rowhammer vulnerability [8] have made it more important than ever to deeply understand the internal structure and error characteristics of DRAM. DRAM is a complex technology with decades of optimizations, and the design choices made by each DRAM manufacturer are proprietary. Prior studies have used creative reverse-engineering methodologies to disclose partial information about the internal structure and characteristics of DRAM [8], [10]. However, we have found some of this information to be misleading, outdated, or limited to a certain type of DRAM.

This paper provides a comprehensive study of internal structures and error characteristics of DDR4 and HBM2, utilizing the three known reverse-engineering techniques. We present new observations of previously undefined behaviors or structures such as asymmetric subarray size, coupled row, and coupled edge subarrays (§5). Moreover, we push the state-of-the-art understanding of the data-, cell structure-, and chip-dependent DRAM error characteristics, while also clarifying the common pitfall in the interpretations of experimental results (§6). We expect our study to guide future DRAM reliability studies to better fit the real-world DRAM, such as devising a worst-case error pattern aware rowhammer protection mechanism or chip-variation aware side-band/on-die ECC.

2 DRAM ORGANIZATION AND STRUCTURE

A DRAM module is hierarchically organized, from top to bottom, ranks, chips, banks, subarrays, and cells (see Figure 1). Each cell consists of a capacitor and access transistor, indexed by row/column address via the wordline (WL) and bitline (BL), respectively. A row decoder enables a WL, which turns on the access transistors that connect the cell capacitors to the sense amplifiers (SA) via BLs. SA is a cross-coupled inverter that senses and amplifies the differential signal of the BL and temporarily stores the value of the DRAM cell. A subarray can have either an open or folded bitline structure, depending on whether a single SA is connected to both the upper and lower



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Figure 1: DRAM organization and structure.

BLs (open) or not (folded). In the open BL case, half of the subarray shares the SA with the upper subarray and the other half with the lower subarray.

Recently, DRAM devices are primarily designed using a $6F^2$ structure [5] for higher cell density. The $6F^2$ DRAM cell adopts a saddle-fin transistor structure with a buried WL and has a capacitor connected to a storage node (SN), while a BL is connected to a bitline contact (BC) (see Figure 2(a) and (b)). Due to the structure of the $6F^2$, two cells sharing the same active region belong to different rows. Moreover, for each row, half of the cells share the active region with the upper row's cells and the other half with the lower row's cells.

As for the DRAM operation, the SAs and BLs are initially precharged to a voltage of $V_{dd}/2$. To access data, the host sends an activate (ACT) command to connect and charge-share a row of DRAM cells with BLs by enabling a WL. Charge-sharing causes a small deviation in the voltage level of the BL. The SA amplifies it to full V_{dd} or 0. When DRAM receives a read or write command, the sensed or to-be-written data pass through the local and global I/O, equipped with temporary buffers on its path (e.g., global dataline SA). After completing read or write operations, the host sends a precharge (PRE) command to disable the activated row's WL, disconnecting the BLs and cells. Prior to the precharge, the voltage level of the cell must be restored to full V_{dd} or 0. The required time to issue the PRE command after the ACT command is tRAS. Moreover, after issuing of PRE command, the SAs and BLs require tRP time to restore a voltage of $V_{dd}/2$.



Figure 2: 6F² DRAM cell structure and layout, mechanisms of activate-induced bitflips (AIBs), and test infrastructure of X-ray.

3 DRAM Reverse-engineering Techniques

on the design choice with the intention of reducing the noise or optimizing the data path from the SAs to the I/O [9].

We leverage three reverse-engineering techniques to identify and verify the DRAM internal structures and characteristics: 1) causing activate-induced bitflips, 2) executing row-copy operation, and 3) inducing retention errors.

Activate-induced bitflips (AIBs) are a DRAM error phenomenon in which the victim cell experiences bitflips when the neighboring aggressor is activated with certain conditions. There are two types of AIBs: 1) rowhammer and 2) passing gate effect [5]. *Rowhammer* is a phenomenon in which repetitive activation of the aggressor causes bitflip in the opposite victim cell that shares the active region (see Figure 2(c)). When an aggressor's WL is activated, (1) electrons accumulate around the WL due to a channel inversion. Upon deactivation, (2) the accumulated electrons are spread out and some are injected into the opposite victim cell. Passing gate effect conversely refers to the occurrence of a bitflip in a victim cell that is separated from the aggressor by a field oxide, due to the repetitive activation of the WL over an extended period of time (see Figure 2(d)). When the aggressor's WL is activated, ① electrons are continuously attracted from the victim cell toward the passing gate. After the row is precharged, 2) the electrons are spread out and some are injected into the active region, instead of returning to the victim cell. In both cases of rowhammer and passing gate effect, a repetition of such process results in a bitflip in the victim cell. As both are the processes of victim cells acquiring or losing electrons, their likelihoods are affected by the data written to the victim cells. Besides, it has been reported that rowhammer is more sensitive to the number of activation, whereas the passing gate effect is more affected by the activated time [5].

Row-copy [2], [11] is an out-of-specification in-memory operation that copies the value of one row to another row within the same subarray using charge-sharing through the BL. First, a source row is activated. After tRAS, the row is precharged. However, if the destination row is activated soon enough, the BL will not be fully precharged to $V_{dd}/2$. Because the capacitance of BL is much larger than the cell, the source row values are effectively copied to the destination row. Leveraging the fact that BL charge-sharing is the fundamental cause of the successful row-copy operation, we not only identify the size of the subarray, but also identify the type of subarray structure (open or folded bitline) for each tested DRAM.

Retention time test exploits the fact that DRAM cells naturally leak charge over time, which leads to retention failure unless periodically refreshed. The retention time of a cell is the length of time before it loses data. Exploiting the fact that leakage occurs from a charged state to a discharged state, we execute retention time testing to identify the true- and anti-cells. While some cells store the value 1 as a charged state (true-cell), others store it as a discharged state (anti-cell), which depends

4 EXPERIMENTAL SETUP

We modified SoftMC [4] to execute the three techniques on DDR4 and HBM2 (see Figure 2(e)). We tested 192 DDR4 chips (8Gb \times 4 chips) from two DRAM manufacturers A (manufactured in 2016 and 2018) and B (manufactured in 2018 and 2021), and two HBM2 cubes (4GB/cube) with undisclosed manufacturers. DDR4 and HBM2 are controlled at 1.25 ns and 2.50 ns, respectively, using Xilinx Alveo U280 FPGA boards [12]. We also employed a temperature controller and silicon rubber heaters to regulate the temperature of DRAM. We tested the DDR4 DIMMs at a temperature of 75°C and HBM2 at room temperature as we could not regulate the temperature of HBM2.

We emphasize that correctly interpreting *the physical address to DRAM address remapping* is essential in acquiring correct information from the reverse-engineering techniques. For example, row addresses are remapped in the row decoder, inverted at a registered clock driver (RCD) chip for half of the DRAM chips [7], and DQ pins are shuffled on a DIMM [6]. We will later clarify that some misconceptions of prior studies stem from the misinterpreted address remapping.

5 DISCOVERING DRAM STRUCTURES

Subarray sizes of each DRAM chip is verified using all three reverse-engineering techniques and cross-checked. First, because two different subarrays are separated by SAs, we look for row address boundaries where AIB occurs from only one aggressor row. Also, considering that only half of the cells share SAs with the upper/lower subarray in the case of open bitline structure, we look for row address boundaries where row-copy starts to work only for half the cells. Moreover, in the case of the manufacturer (mfr.) B, we can also look for boundaries of true- or anti-cells as it is known that a single subarray consists of only one type of cells [9].

As opposed to the common understanding of the size of a subarray, we discovered that the size of subarrays is not a power of 2 and also varies within even a single chip. The mfr. A's DDR4 chips manufactured in 2016 have a repeated pattern of 11 subarrays of 640 rows and two subarrays of 576 rows (a total of 8192). In the case of chips made in 2018, a pattern of four subarrays of 832 rows and one subarray of 768 rows (total of 4096) is repeated. By contrast, the mfr. B's DDR4 chips have a pattern of two subarrays with 688 rows and one subarray with 672 rows (a total of 2048). Lastly, HBM2 chips have a pattern that repeats in units of 4096 rows, with each pattern consisting of four subarrays of 832 rows and one subarray of 768 rows. We argue that the varying size of the subarray is a compromise between increasing timing parameters and higher cell density when the cell per BL (subarray size) increases. This concurs



Figure 3: Characteristics of subarray structures: (a) Activating a row could incur activating its coupled row. (b) An edge subarray physically consists of a pair of subarrays, each having dummy bitlines.

with the fact that the size of the subarray is on an increasing trend, following the DRAM process scaling.

Observation-1: The subarray sizes are not power of 2, and are different across different generations and within a chip.

Subarray structure types are verified by exploiting the rowcopy operation. Because adjacent subarrays share half of the SAs for open bitline structure and none for folded bitline structure, checking the copied data from the row-copy operation across different subarrays allows us to distinguish them. In the case of folded bitline, none of data is changed, whereas half of the row is copied in the case of an open bitline structure.

All the tested DRAM chips have an open bitline structure. However, while the row-copy on mfr. B's DDR4 resulted in half of the row being copied as is, DDR4 of mfr. A and HBM2 resulted in the copied values being inverted. While mfr. B's DDR4 consists of both true-/anti-cells, HBM2 consists only of true-cells. We believe that this is due to the design choice in the datapath, where the latter would employ a MUX to choose one of the differential local I/O signals.

Coupled rows activation is also identified for a portion of ×4 DRAM chips; when one row is activated, its coupled row is simultaneously activated. Both the row-copy operation and the AIBs indicate that when a row is activated (e.g., i^{th} row), its coupled row (e.g., $(i + N_{row}/2)^{th}$ row) is also activated, where N_{row} denotes the total number of rows in a bank. Such behavior was exhibited on mfr. A's ×4 DDR4 chips and HBM2. Thus, we speculate that this is a result of optimization to reduce the number of row address decoders or to maintain a uniform internal DRAM cell structure between the chips with different I/O widths (i.e., ×8 and ×4 chips). This behavior can serve as another vulnerability regarding AIBs unless the host is aware of this pairing and applies proper mitigation to both the victim row and its coupled row.

Observation-2: For some DRAM chips, activating a row can result in the unintended activation of the coupled row.

Edge subarrays of the open bitline structure were also identified to work in tandem to create a single full subarray. For some tested DRAM chips, when the row-copy operation was executed for 0^{th} row as a source and $(N_{row}/2 - 1)^{th}$ row as a destination, half of the cells were copied despite the large difference in the row address values. Because the 0^{th} row and the $(N_{row}/2 - 1)^{th}$ row belong to the subarrays of the bottom and top edge, respectively, we speculate that these two subarrays work together as a single subarray. Similarly, the DDR4 from mfr. A manufactured in 2016 and 2018 have edge subarrays at every $N_{row}/8$ and $N_{row}/4$ boundary, respectively. That of the DDR4 from mfr. B and manufacturer-unspecified HBM2 was $N_{row}/4$ and $N_{row}/2$, respectively. Such a structure



Figure 4: Aggregate bit error count from AIB of DDR4 and HBM2. Considering the recurring pattern, we only show the bit index up to 32.

Upper aggressor			/			
	+ +	+ +	+		ŧ	
Even/Odd victim 0 0 0 0	0 0 0 0	1 1 1 1	1	1	1	1
	<u>+</u>	† †		1		1
Lower aggressor						
(a) Eff _{discharge} , e	ven/odd victim	(b) Eff _{charge} , ev	/en/o	dd v	/ict	im

Figure 5: Exemplar Eff_{charge} and Eff_{discharge} for HBM2.

of the edge subarray is reasonable considering that only half of the cells are connected to SAs on either side of the edge (see Figure 3(b)). Also, this is an undefined behavior for the host and thus could be a source of vulnerability.

Observation-3: For some DRAM chips with open bitline structure, two edge subarrays work in tandem to create a single full subarray.

6 INVESTIGATING DRAM AIB CHARACTERISTICS

In this section, we demonstrate for the first time that the worstcase AIB aggressor pattern is defined by the $6F^2$ DRAM structure as well as the data dependence of rowhammer and passing gate effect. Also, we present the intra-/inter-chip AIB variation and clarify the commonly misperceived AIB characteristic.

First, we observed that when each DRAM cell is AIB victimized, it exhibited a particularly more vulnerable side of aggressor depending on the written data and its position. For example, half of the cells in a row were more vulnerable to the upper aggressor when in a charged state and to the lower aggressor when in a discharged state (see Figure 4). More specifically, there existed a pattern of such correlation for each cell depending on the cell index and whether they were in an even/odd row. We believe that such a pattern originates from the 6F² structure, where each cell has a neighboring gate (rowhammer vulnerable) on one side and a passing gate (passing gate effect vulnerable) on the other. Because both rowhammer and passing gate effect are affected by the written data of the victim cell, the correlation between the data and the vulnerable side can also be explained. While 6F² should expose a pattern repeating in a cell index of 2, some chips in Figure 4 demonstrate a pattern of 8 and 4 due to the difference in serialization inside the DRAM chip.

To further investigate the correlation of our observation with rowhammer and passing gate effect, we conducted a sensitivity study on the *activation count* (rowhammer sensitive) and *row activated time* (i.e., duration of a row staying active, which is passing-gate sensitive). We first categorized two types of AIB aggressor patterns; i) aggressor patterns that are effective



Figure 6: Relative BER (bit error rate) per row of Eff_{charge} and Eff_{discharge} when we vary activation counts and row activated time for the DDR4 and HBM2 devices.

when the victim data is in a charged state (Eff_{charge}) and ii) in a discharged state (Eff_{discharge}). As Figure 5 illustrates, both patterns have interleaving upper/lower sides depending on the victim data, whether the victim is an even/odd row, and the bit index. Each pattern should be correlated to the rowhammer or passing gate effect, respectively. Upon these two patterns, we changed the activation count from 200K to 400K with tRAS (35ns) activated time, and changed the activated time from 35ns to 175ns with a fixed activation count of 300K.

First, both patterns of Eff_{charge} and $Eff_{discharge}$ were highly sensitive to the activation count with Eff_{charge} reaching up to $146 \times$ increase in bit error rate (BER) per row (see Figure 6(a)). Second, while Eff_{charge} was also sensitive to the activated time, Eff_{discharge} was relatively less sensitive (see Figure 6(b)). The BER per row increase for Eff_{discharge} was limited to less than $1.52\times$. Based on these results, we conclude that Eff_{charge}, which is sensitive to activate time, is the result of the passing gate effect and Eff_{discharge}, which is only sensitive to activation count, is the result of the rowhammer. This contradicts the prior explanation [5] that states that rowhammer is effective on the charged state victim and vice versa for the passing gate, which requires further investigation in the future.

Observation-4: The worst-case AIB aggressor pattern is defined by the unique 6F² DRAM cell structure and data dependence of rowhammer and passing gate effect.

We also recognized that the AIB characteristics exhibit relatively small intra-chip and large inter-chip variations. Figure 7 demonstrates the box and whisker plot of the bit error count of each row for a fixed 300K number of activations, and the line plot of HC_{first} (the lowest activation count that incurs first bitflip anywhere on a chip). We identify that while there were some variations inside a single chip (intra-chip), chip-to-chip variation was more pronounced (inter-chip). This indicates that an AIB vulnerable chip can determine the overall vulnerability of the whole DRAM module.

Observation-5: AIB exhibits significant inter-chip variation while demonstrating a relatively restricted distribution within a single chip.

Finally, we verified that the direct non-adjacent rowhammer (AIB) effect¹ [8] and half row [1] are misguided interpretations which can be clarified when the RCD address inversion [7] is properly taken into account. Half of the DRAM chips in a registered DIMM experience address inversion at the RCD chip [7]. The direct non-adjacent AIB effect was able to be reproduced, yet only when such an address inversion by RCD chips was neglected. This concurs with the prior study that



Figure 7: The box and whisker plots of the bit error count per row for each chip of DDR4 and HBM2 and the line graphs of HC_{first} for each chip of DDR4.

could not reproduce the direct non-adjacent AIB effect [3]. The same was true for the half row observation [1]. We believe that our clarification further highlights the complexity and difficulty of correctly reverse-engineering the DRAM internals.

7 FUTURE WORK AND CONCLUSION

We have reliably revealed the DRAM's internal structure and activate-induced bitflip (AIB) characteristics through AIB tests, row-copy operation, and retention tests using commercial DRAM devices. We discovered the previously undisclosed subarray structure and behaviors, and also the worst-case AIB aggressor pattern that is determined by the 6F² structure and data dependence of rowhammer and passing gate effect. We also clarified the common misconceptions from prior DRAM studies such as direct non-adjacent AIB effect. We anticipate our new observations and clarifications, as well as the experimental methodology itself, to facilitate the future DRAM research.

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^{1.} A phenomenon where frequently activating N^{th} row can *directly* affect not only distance 1 (i.e., $N \pm 1^{th}$ rows) but also distance 3, 5 and further away rows [8].