INTEGRATED CIRCUITS FOR COMMUNICATIONS


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In this issue of the Integrated Circuits for Communications Series, we continue the theme of integrated circuit design for multi-standard radios. We have selected two papers covering this area, which is drawing significant attention from industry as well as research communities worldwide.

In the past 30 years, wireless technologies have dramatically penetrated into every aspect of our lives. Today, virtually everyone around the world carries a cell phone or a connectivity device to access multimedia services. As wireless standards diversify, such mobile devices have become increasingly complex in having multiple radios to support multiple standards. Current cell phones typically support six radios, including: cellular, Wi-Fi, Bluetooth, global position system (GPS), FM, and near-field communications (NFC). The use case has also become increasingly sophisticated with demands rising to support the concurrent use of multiple services, for instance, being able to use the GPS for navigation while speaking on the phone or browsing on the Internet. Such a concurrent use scenario requires multiple radios to be on at the same time, which stresses the power consumption as well as cost of the mobile device. While software defined radio (SDR) technologies have been touted for their flexibility and configurability to support multiple standards (see the April 2012 issue), concurrent use cases add to the already challenging SDR design the need to be programmable for not just one standard but multiple standards at the same time.

In past issues of our series (August 2005, August 2006, April 2012, and October 2012), we have seen a clear trend in advances made on circuits implementations for SDR's. However, the added challenge of supporting multiple wireless standards concurrently has not been addressed. In the first paper, entitled "Digital Transmitter Design for Mobile Devices," the authors present a digitally intensive multi-standard transmitter design that can be programmed to support the transmission of not only Wi-Fi but also Bluetooth waveforms. Moreover the authors give a broad birds eye view of major transmitter architectures and discuss the key trade-offs that drove them to select the RF digital quadrature architecture for their design, which has achieved a 37 percent drain efficiency at 24.7dBm peak power with a small die area of 0.7mm2 in 40nm complementary metal oxide semiconductor (CMOS) technology. Their chip achieves the error-vector magnitude (EVM) and adjacent channel leakage ratio (ACLR) requirements for long-term evolution (LTE), IEEE 802.11ac, and Bluetooth enhanced data rate mode.

On the receive side, to support most of the standards today, a SDR is required that can receive a broad spectrum spanning 500MHz to 3GHz. Conventional SDRs utilize flexible radio-frequency (RF) down conversion followed by Nyquist sampling to digitize an RF signal for reception in the digital domain. More sophisticated SDRs enable the concurrent reception of multiple radio signals compliant with different standards occupying anywhere within the 500MHz to 3GHz. Ultimately, the ability to digitize multi-GHz of spectrum and be able to not only receive predetermined but also unknown channels over a wide spectrum leads to the realization of cognitive radios — the holy grail that we have not yet realized.

To digitize multi-GHz spectrum, an ultra high speed and high dynamic range analog-to-digital converter is necessary, which results in an impractical implementation requiring expensive exoteric processing technology, as well as excessive power consumption. However, most of the time, the 3GHz spectrum is unoccupied, i.e. sparse. In this case, when the occupied spectrum is small RF bandwidth, compressive sensing promises an unambiguous recovery of the incoming signals even under significant under-sampling. The second paper, entitled "Compressive Samplers for RF Environments," discusses the application of compressive sensing theory to RF signal reception. The author provides an overview of compressive sensing and proposes a non-uniform sampling approach and compares computational complexity, as well as noise penalty with respect to Nyquist sampling for different spectrum occupancy levels. The compressive sampling concept has been demonstrated with a prototype implemented with an Indium Phosphide (InP) front-end together with two commercial off-the-shelf ADCs.

We would like to take this opportunity to thank all the authors and reviewers for their contributions to this Series. Future issues of this series will continue to cover circuit technologies that are enabling new emerging communication systems. If readers are interested in submitting a paper to this Series, please send your paper title and an abstract to any of the Series Editors for consideration.

BIOGRAPHIES

CHARLES CHIEN (charles.chien@creonexsystems.com) is the president and CTO of CreoNex Systems which focuses on technology development for next generation communication systems. Previously he has held various key roles at Conexant Systems, SST Communications, and Rockwell. In his career, he has architected several key products including CMOS/SiGe chip-set for Multimedia over Coax (MoCA), IEEE 802.11abg WLAN RF CMOS transceiver and GaAs PA/RF switches, wireless audio CMOS chip-set for home theatre in a box, digitally-assisted cellular transceivers, and low-power wireless networked sensors. He was also an Assistant Adjunct Professor at UCLA from 1998–2009. His interests focus mainly on the design of system on-chip solutions for wireless multimedia and networking applications. He has published in various journals and conferences, and has authored a book entitled Digital Radio Systems on a Chip. He received his B.S.E.E. from UC Berkeley and M.S. and Ph.D. from UCLA. He served as a member of the technical program committee of ISSCC from 1998 to 2006.

ZHIWEI XU received the B.S. and M.S. degree from Fudan University, Shanghai, China and Ph.D. from UCLA, all in electrical engineering. He held industry positions with G-Plus Inc., SST communications, Conexant Systems and NXP Inc., where he did development for wireless LAN and SoC solutions for proprietary wireless multimedia systems, CMOS cellular transceiver, Multimedia over Cable (MoCA) system and TV tuners. He is currently with HRL laboratories, working on software defined radios, high speed ADC and analog VLSI. He has published in various journals and conferences, one contribution to the encyclopedia of wireless and mobile communications, and five granted patents.