Guest Editors' Introduction: Speeding Up Analog Integration and Test for Mixed-Signal SoCs

Rubin Parekhji
Texas Instruments

Kenneth M. Butler
Texas Instruments

Gordon W. Roberts
McGill University

■ **Today's integrated circuits** with embedding processing capabilities have an ever increasing analog content. While this helps to build richer end applications easily, it significantly complicates the design process. A gamut of heterogeneous analog and digital functional modules must now be integrated across different voltage levels and interfaces. Analog integration and test is hence emerging as one of the biggest challenges in an otherwise standard system-on-chip (SoC) design flow.

While standard practices have been defined for design and reuse (in both integration and test) for digital intellectual property (IP) cores—the term is used interchangeably with specified functions and implemented modules—the same is not the case with analog IPs. This disparity is due to some major differences, namely 1) lack of adoption of standard interfaces to integrate such IPs in an SoC; 2) electrical challenges in integration and test due to undesired coupling between digital modules and the analog IPs themselves; 3) complex calibration and characterization procedures due to different functional, power management and test modes; 4) lack of a common metric for adequate coverage in verification and test; and 5) diverse design characteristics of these IPs themselves (voltage and frequency bands, with and without digital assistance and clocked logic, and noise tolerance and sensitivity) as can be found across pure analog functions, mixed-signal functions, and RF functions.

Although there is a lack of standardized methods, metrics, and tools to support mixed-signal design and integration, there are unique challenges associated with them. Examples include how to perform comprehensive verification, how to measure and ensure adequate analog test coverage (and also minimize redundant analog testing), and how to create and track a specification compliance matrix across the entire design-to-manufacturing flow. And as the level of integration increases, these questions loom ever larger.

These observations have been the motivation for compiling this special issue. It was conceived more than a year ago, keeping in mind the importance and impact of integration and test of analog IPs in mixed-signal SoCs. While the problems that they pose are not new, the solution space is vast and very often specific to the IP under consideration. Design and test engineers struggle to select and apply the right methods, and those used more often than not reflect what they are aware of through adoption on earlier designs, as against the right selection from those which are available.

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In this special issue, we have technical papers addressing many of the problems discussed above. There are seven papers in total, organized along the lines of the overall design-to-test flow, covering verification, selection of test content, defect level estimation, silicon validation, and data-driven test optimization and yield recovery.

The first paper, "Formal Interpretation of Assertion-Based Features on AMS Designs" by Bruto da Costa and Dasgupta, proposes the adoption of formal methods for modeling of analog functions. It explains how assertions can be overlaid onto the range of values of individual features in an analog function, and proceeds toward building a mathematical (hybrid automata) model to represent and analyze them. An LDO regulator and a battery charger are used as examples.

The second paper, "A Procedure for Alternate Test Feature Design and Selection" by Barragan and Leger, is a practical illustration of the adoption of alternate tests based upon the judicious selection of the set of parameters to be considered for design as well as to be observed subsequently. The notion of signatures is introduced, and their ability to predict design accuracy is analyzed. The application is demonstrated for an RF LNA circuit.

In the third article, "A Comparative Study of State-of-the-Art High-Performance Spectral Test Methods," Sudani et al. observe that a number of new methods have emerged for efficient and effective testing of data converters, but there is no work comparing their strengths and weaknesses. The authors describe four recent methods in detail, highlighting important aspects and contrasting their abilities to perform various test measurements.

The fourth paper, "Adaptive-Learning-Based Importance Sampling for Analog Circuit DPPM Estimation" by Yilmaz and Ozev, addresses the important problem of defect level estimation. For more than 30 years, there have been published models which are commonly used to estimate the time zero test escape rate of digital logic designs. However, estimating escape rate for analog circuits is much more challenging. This paper applies importance sampling techniques to this problem to arrive at a much more practical method of analog defect level computation.

The fifth paper, "Digital Analog Design: Enabling Mixed-Signal System Validation" by Lim et al., proposes a method to validate mixed-signal circuits and systems using procedures similar to those used for digital systems. By comparing the initial functional model at the block level with a corresponding model of the transistor implementation, the suitability of the design can be judged. The significance of this work is how these models are constructed and compared, and how this information is managed using existing digital CAD tools.

Since analog test program content is typically compiled based on the specifications in the data sheet for the analog circuit, often without the benefit of fault coverage information, there are frequent redundancies in the overall test process. To face this problem, in the sixth paper, "Low-Cost Analog/RF IC Testing Through Combined Intra- and Inter-Die Correlation Models," Huang et al. use powerful statistical methods to identify and take advantage of correlations in the test methods and wafer-level spatial correlations among devices. The result, shown for industrial designs, is a far more optimized test suite.

The seventh paper, "Yield Recovery of RF Transceiver Systems Using Iterative Tuning-Driven Power-Conscious Performance Optimization" by Natarajan et al., proposes a fast and low-cost method of calibrating RF transceiver systems using on-chip DSP resources and some additional circuit control points. Experimental results on a commercial power amplifier demonstrate significant increases in production yields using the proposed approach.

In "The Last Byte" column, Prof. Peng Li of Texas A&M University remarks on the increasing difficulty of analog verification in the face of technology scaling. He proposes some ideas on how to alter our thinking to meet this challenge.

We hope that the readers will find this special issue a valuable compilation for handy reference. *IEEE Design & Test* encourages readers to submit their recent work with a view to educating the design community at large as well as to provide a catalyst for new research. We look forward to more papers in these areas from other researchers and practitioners, in subsequent issues. In closing, we would like to thank all the authors and the reviewers for their contributions to this issue, and the Editor-in-Chief and the *IEEE D&T* publication team for supporting this special issue. We also welcome feedback and suggestions from the readers and others who would like to contribute to this magazine. ■

Rubin Parekhji is a Senior Member of Technical Staff in the Kilby Labs, Texas Instruments, Bangalore, India. His current research areas include extremely low-cost test of analog and embedded processing products for different end applications. Parekhji has a PhD in computer science and engineering from Indian Institute of Technology, Bombay, India.

Kenneth M. Butler is a TI Fellow in the Analog Engineering Operations Group, Texas Instruments, Dallas, TX, USA. His research interests include outlier techniques for quality and reliability and test-data-driven decision making. Butler has a PhD in electrical engineering from the University of Texas at Austin, Austin, TX, USA. He is a Fellow of the IEEE.

Gordon W. Roberts is the James McGill Professor of Electrical and Computer Engineering at McGill University, Montreal, QC, Canada. He has co-written seven textbooks related to analog IC design and mixed-signal test. His research interests include all aspects of design and test for analog and mixed-signal circuits. Roberts has a PhD in electrical engineering from the University of Toronto, Toronto, ON, Canada. He is a Fellow of the IEEE.

■ Direct questions and comments about this article to Rubin Parekhji, Texas Instruments, Bangalore, India; parekhji@ti.com.