From the EIC

A Look at Asynchronous Design and Photonic Network-on-a-Chip (PNoC)

Welcome to our May/June issue of *D&T*! This issue brings you a range of articles and columns on a wide set of topics. We hope you will enjoy the variety!

This month we kick things off by diving head first into a two-part article examining the links between historical and modern asynchronous design. S. Nowick from Colombia University and M. Singh from the University of North Carolina at Chapel Hill provide an overview of asynchronous design's history, from clockless techniques in the 1950s to the latest advances in design approaches and methods. The authors highlight new commercial opportunities for hybrid synchronous/asynchronous design for object-oriented hardware systems now amounting to multi-billion transistor scales. In part two of the article, the exciting benefits of a hybrid approach to power management, variability, and modular/extensible support, are described through powerful design and test methods.

Next, we move to an article by S. Chittamuru and S. Pasricha from Colorado State University. The article examines the potential for photonic network-on-chip (PNoC) architectures to address bandwidth and power-dissipation challenges in on-chip communication, and the specific issue of reliability impacted by PNoC micro-resonator crosstalk. The authors suggest an innovative solution through two encoding mechanisms to reduce crosstalk noise and improve worst-case signal-to-noise ratios in concrete PNoC examples.

Also included in this issue is another installment of our well-received panel discussions; this time extracted from the *IEEE D&T* ITC 2014 Roundtable covering "open problems" in today's design and EDA partnerships. Broadly, our summary of the panel, which included members from Texas Instruments, Mentor Graphics Corporation, Cadence Design Systems, Broadcom Corporation, IBM and Intel (organized by R. Parekhji and S. Mitra), highlights a multi-faceted discussion of the business perspective on how to better manage design-EDA partnerships in the face of evolving challenges in design, validation, test, and qualification of IP cores, SOCs, and end systems. We hope you will find this roundtable as enjoyable to read as it was to hear live!

We conclude the issue with another thought-provoking installment of *The Last Byte* by Scott Davidson.

We are thrilled to bring you what we believe is a captivating installment to kick off the summer months, from the perspective of our Northern Hemisphere readership! To all of our readers, thank you as always for your continued support, and we very much look forward to the next issue! Stay posted for several upcoming Special Issues, and send us your comments and suggestions on topics you would like to see presented in the future. ■

Andre Ivanov
Editor in Chief
IEEE Design & Test

Digital Object Identifier 10.1109/MDAT.2015.2417799
Date of current version: 04 June 2015.

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