From the EIC

Advances in 3-D Integrated Circuits, Systems, and CAD Tools

Exploiting the third or *z*-axis direction in microelectronic circuits has been highly sought-after in many instances, and with soaring increases and demand for chip performance at lower cost, the interest in 3-D integrated circuits (ICs) is seeing an unprecedented surge. In light of this, as well as the many recent breakthroughs and reported challenges of today's 3-D integration for improved IC performance, power consumption, integration density, and so on, we bring you here a Special Issue of *IEEE Design & Test* on Advances in 3-D Integrated Circuits, Systems, and CAD Tools. The collection of articles in this Special Issue highlight leading-edge research and methodologies that address nagging challenges persisting in today's 3-D integration, and the work being done to realize both 3-D and hybrid 2.5-D schemes for more fluid design and test platforms that can yield the most benefits at the least cost in the coming years. This set of specially written and selected articles examine both specific case studies of the most significant problems in 3-D ICs, while also providing a broader view on how such 3-D ICs can be deployed for mainstream applications. We hope you will find this collection both detailed and expansive enough to make your reading highly enjoyable!

With reference to the benefits of 3-D IC integration, our first article by Kim and Lim outlines residual performance and power restrictions that make 3-D integration still unsatisfactory for high-performance and low-power chip markets. Recognizing leading-edge prototypes and commercial products on the fringe of market availability, the authors discuss four specific 3-D integration examples, along with optimization problems and associated challenges for adoption in the mainstream semiconductor market.

Our second paper is a specialized article by Katti et al. that supplements our 3-D focus. This paper addresses Cu-RDL interconnects as an alluring alternative to bring 2.5-D low-cost through silicon interposer (TSI) to the fore. The authors' detailed analysis of 2.5-D TSI cost reduction brings readers through a steady, unhurried examination of industry challenges and solutions which rounds off the article's readability.

Our third article, by Han et al., brings the heat dissipation discussion to 3-D package-on-package (POP) technology in light of evolving embedded wafer-level packaging. The authors provide a detailed study on how multiple internal factors (materials and dimensions) and specifics, such as a thermal cap and special package lid developments, lead to improved cooling solutions. The authors support their findings through comprehensive simulated thermal analysis, and validate them with experimental results.

Next, we have included a magnified look at the automation of a 3-D design-for-test architecture using Cadence EDA tools. The authors, Papameletis et al., highlight developments in 3-D stacked ICs and mitigation of 3-D IC manufacturing defects, and constructively extend an analysis of what good design-for-testability infrastructure should do for large SoC designs.

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Revisiting the topic of 2.5-D, Xu et al. discuss the heat removal difficulty of 3-D compared to 2-D integration, supporting thermal-resilient 2.5-D integration by through silicon interposers. To counter the enormous memory-access demand from cores, the article proposes and verifies the improvements by a reconfigurable memory controller in the 2.5-D context.

Authors Chou et al. introduce a hierarchical test integration method for handling design-for-testability circuitry of 3-D ICs. The authors propose two test control interfaces, aiming their crosshairs on two types of dies in a 3-D IC (vertically connected by through silicon vias), as well as a hierarchical test control mechanism which reinforces the crucial need for standardized test control interfaces.

In our final article, Thakkar and Pasricha introduce us to 3-D WiRED, a new energy-efficient wide I/O DRAM architecture that uses a 3-D bank organization to aid in achieving amazing improvements in read/write energy and random access time, among many other impressive benefits.

To wrap up the issue, we bring you a welcome and thought-provoking "The Last Byte" by Scott Davidson.

In closing, I would like to express my sincere thanks to all those who have contributed to creating this Special Issue: authors, reviewers, the *D&T* editorial board, IEEE staff, Sara Dailey, and Ross Sheppard. Special thanks are owed to Sun Kyu Lim from Georgia Tech and Dae Hyun Kim from Cadence for coming up with the proposal that realized this Special Issue on Advances in 3-D Integrated Circuits, Systems, and CAD Tools. All of the above are closely working with me as the Editor-in-Chief, and the authors, reviewers, and the *D&T* editorial board members are all highly appreciated. We have more Special Issues to come, and we hope you enjoy this one to its fullest! ■

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