From the EIC

Time-Critical Systems Design, Part II

■ **THIS ISSUE FOCUSES** on the second part of the very successful special issue on designing and testing time-critical systems with six technical papers. Again, many thanks to Guest Editors Tulika Mitra, Jürgen Teich, and Lothar Thiele for their extraordinary work on this series of two special issues.

There are two general interest papers in this issue. In "Testable Design of Reversible Circuits Using Parity Preserving Gates," the authors, Hari Mohan Gaur, Ashutosh Kumar Singh, and Umesh Ghanekar, focus on reversible logic circuits with parity preserving gates to convert an arbitrary circuit into corresponding testable form. In "Adaptive Approximate Computing in Arithmetic Datapaths," the authors, Sana Mazahir, Osman Hasan, and Muhammad Shafique, present an automated mechanism to sense an error at the component level and adapt the subsequent operations of the datapath.

The Design, Automation, and Test in Europe (DATE) took place on 19–23 March 2018 in Dresden, Germany. Thanks to Jan Madsen and Ayse K. Coskun for providing us with a Conference Report of the event.

Many thanks also to Scott Davidson for "The Joy of Scheduling" in The Last Byte.

I hope you find this issue of *IEEE Design&Test* interesting. For any questions or inspirations, please contact me at henkel@kit.edu. ■

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Jörg Henkel
Editor-in-Chief
IEEE Design&Test