TTTC News

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PAST TTTC EVENTS

The 25th International Symposium on On-Line Testing and Robust System Design (IOLTS'19)

1–3 July 2019
Rhodes, Greece
http://tima.univ-grenoble-alpes.fr/conferences/iolts/iolts19/index.php

Issues related to on-line testing techniques, and more generally to design for robustness, are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low-cost products. There is a corresponding increase in the demand for a cost-effective design for robustness techniques. These needs have increased dramatically with the introduction of nanometer technologies, which adversely impact noise margins; process, voltage, and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating; and make mandatory the use of design for robustness techniques for extending, yield, reliability, and lifetime of modern SoCs. Design for reliability also becomes mandatory for reducing power dissipation, as voltage reduction, which is often used to reduce power, strongly affects reliability by reducing noise margins and thus the sensitivity to soft-errors and EMI as well as by increasing circuit delays and therefore the severity of timing faults. There is also a strong relation between design for reliability and design for security, as security attacks are often fault-based.

The International Symposium on On-Line Testing and Robust System Design (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The symposium is sponsored by the IEEE Council on Electronic Design Automation (CEDA) and the 2019 edition is organized by the IEEE Computer Society Test Technology Technical Council, the University of Athens, and the TIMA Laboratory.

The 32nd IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT'19)

2–4 October 2019
Delft, The Netherlands
http://www.dfts.org/

The IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) is an annual symposium providing an open forum for presentations in the field of defect and fault tolerance in very-large-scale integration (VLSI) and nanotechnology systems inclusive of emerging technologies. One of the unique features of this symposium is to combine new academic research with the state-of-the-art industrial data, which are necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. Topics include (but are not limited to) the following: yield analysis and modeling; testing techniques; design for testability in IC design; error detection, correction, and recovery; dependability analysis and validation; repair, restructuring, and reconfiguration; defect and fault tolerance; radiation effects; aging and lifetime reliability; dependable applications and case studies; emerging technologies; and design for security.

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UPCOMING TTTC EVENTS

The IEEE International Test Conference (ITC 2019)
12–14 November 2019
Washington, D.C., USA
http://www.itctestweek.org/about-itc/

The International Test Conference (ITC) is the world's premier venue dedicated to the electronic test of devices, boards, and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability, and failure analysis, and back to process and design improvement. At ITC, design, test, and yield professionals can confront challenges faced by the industry and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers. ITC, the cornerstone of the Test Week event, offers a wide variety of technical activities targeted at the test and design theoreticians and practitioners, including formal paper sessions, tutorials, panel sessions, case studies, invited lectures, commercial exhibits and presentations, and a host of ancillary professional meetings.

The 4th Automotive Reliability and Test Workshop
12–14 November 2019
Washington, D.C., USA
http://cas.polito.it/ART2019/

The Automotive Reliability and Test (ART) Workshop focuses exclusively on test and reliability of automotive and mission-critical electronics, including design, manufacturing, burn-in, system-level integration, and in-field test, diagnosis, and repair solutions, as well as architectures and methods for reliable and safe operations under different environmental conditions. With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable operation of electronics in safety-critical domains is still a major challenge. The ART Workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.

ART will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

The 1st International Workshop on Emerging Memories: Technology, Design, Testing
12–14 November 2019
Washington, D.C., USA
http://users-tima.imag.fr/amfors/vatajeli/emtdt2019/index.html

The International Workshop on Emerging Memories: Technology, Design, and Testing (EMTDT) focuses on emerging memory technologies that are triggering intense interdisciplinary activity; they have the potential to provide many benefits, such as energy efficiency, density, reconfigurability, nonvolatility, novel computational structures and approaches, massive parallelism, and so on. This workshop will provide a forum to discuss challenges, trends, solutions, and applications of these rapidly evolving memory technologies by gathering researchers and engineers from academia and industry by creating a unique network of competence and experts.

NEWSLETTER EDITOR'S INVITATION

I would appreciate input and suggestions about the newsletter from the test community. Please forward your ideas, contributions, and information on awards, conferences, and workshops to Theocharis (Theo) Theocharides, Department of Electrical and Computer Engineering, University of Cyprus, 75 Kallipoleos Avenue, PO Box 20537, Nicosia, 1678, Cyprus; ttheocharides@ucy.ac.cy.

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