TTTC News

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PAST TTTC EVENTS

The 25th IEEE European Test Symposium (ETS'20)

May 25–29, 2020
Tallinn, Estonia
http://ets2020.taltech.ee/

The IEEE European Test Symposium (ETS) is Europe's premier forum dedicated to presenting and discussing scientific results, emerging ideas, applications, hot topics, and new trends in the area of electronic-based circuits and system testing, reliability, security, and validation.

In 2020, ETS will take place in the Radisson Blu Sky Hotel in Tallinn. The city is known for the picturesque old town with its medieval architecture. It is organized by the Tallinn University of Technology (TalTech), which cosponsors the event jointly with the IEEE Council on Electronic Design Automation (CEDA). In addition to scientific paper submissions, ETS offers a track for informal contributions dedicated to early hot ideas and relevant case studies as well as a PhD forum. A Test Spring School and Fringe Workshops will be organized in conjunction with ETS'20.

The 26th International Symposium on On-Line Testing and Robust System Design (IOLTS'20)

July 13–15, 2020
Naples, Italy
http://tima.univ-grenoble-alpes.fr/conferences/iolts/iolts20/

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The International Symposium on On-Line Testing and Robust System Design (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The symposium is sponsored by the IEEE CEDA and the 2020 edition is organized by the IEEE Computer Society Test Technology Technical Council, the Politecnico di Torino, the University of Athens, the TIMA Laboratory, and iRoC Technologies.

Issues related to online testing techniques, and more generally to design for robustness, are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low-cost products. There is a corresponding increasing demand for a cost-effective design for robustness techniques. These needs have increased dramatically with the introduction of nanometer technologies, which impact adversely noise margins; process, voltage, and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating; and make the use of design for robustness techniques for extending, yield, reliability, and lifetime of modern SoCs mandatory. Design for reliability also becomes mandatory for reducing power dissipation, as voltage reduction, often used to reduce power, strongly affects reliability by reducing noise margins and thus the sensitivity to soft-errors and EMI, and by increasing circuit delays and thus the severity of timing faults. There is also a strong relationship between design for reliability and design for security, as security attacks are often fault-based.

UPCOMING TTTC EVENTS

The 33rd IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT'20)

October 19–21, 2020
Rome, Italy
http://www.dfts.org/

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DFT is an annual symposium providing an open forum for presentations in the field of defect and fault tolerance in VLSI and nanotechnology systems inclusive of emerging technologies. One of the unique features of this symposium is to combine new academic research with state-of-the-art industrial data, necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. Topics include (but are not limited to) the following: yield analysis and modeling; testing techniques; design for testability in IC design; error detection, correction, and recovery; dependability analysis and validation; repair, restructuring, and reconfiguration; defect and fault tolerance; radiation effects; aging and lifetime reliability; dependable applications and case studies; emerging technologies; design for security.

The IEEE International Test Conference (ITC 2020)

November 3–5, 2020
Washington, DC, USA
http://www.itctestweek.org/about-itc/

International Test Conference (ITC) is the world's premier venue dedicated to the electronic test of devices, boards, and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement. At ITC, design, test, and yield professionals can face challenges faced by the industry and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers. ITC, the cornerstone of the test week event, offers a wide variety of technical activities targeted at test and design theoreticians and practitioners, including formal paper sessions, tutorials, panel sessions, case studies, invited lectures, commercial exhibits and presentations, and a host of ancillary professional meetings.

NEWSLETTER EDITOR'S INVITATION

I would appreciate input and suggestions about the newsletter from the test community. Please forward your ideas, contributions, and information on awards, conferences, and workshops to Theocharis (Theo) Theocharides, Department of Electrical and Computer Engineering, University of Cyprus, 75 Kallipoleos Avenue, PO Box 20537, Nicosia 1678, Cyprus; ttheocharides@ucy.ac.cy.

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