

Guest Editors'

Introduction: SBCCI 2020

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■ **THE SYMPOSIUM ON INTEGRATED** Circuits and Systems Design (SBCCI) is an international forum dedicated to Integrated Circuits and Systems Design, Test and Electronic Design Automation (EDA), held annually in Brazil. The SBCCI has established itself as an important international forum for the presentation of advanced research results on leading-edge aspects of integrated circuits and systems design, such as analog circuits, mixed-signal and digital integrated circuits design, dedicated and reconfigurable architectures, EDA tools, design methods, embedded systems, SoC, and nanoarchitectures, as well as verification and test methods. This 33rd edition of SBCCI was initially planned to take place in Campinas, 100 km from São Paulo, but due to the COVID-19 pandemic, it was transformed into a virtual event.

This special section contains extended versions of the best papers presented at the SBCCI 2020. These papers have been again refereed along the usual refereeing process in force at the *IEEE Design & Test*. We are proud to offer these papers to the readers of this journal now. Five papers, covering a variety of topics related to the event, have been finally selected, as follows.

- “Dedicated Shapelet Distance Engine for Time-Series Classification” proposes a parameterizable parallel hardware accelerator for addressing the drastic computing requirements of current shapelet-based methods.

- “Expanding Column Line Code Adaptive (CLC-A) for Protecting 32- and 64-bit Data” discusses a solution for combining the strengths in terms of energy consumptions and error-correction capacity of the standard and extended CLC modes.
- “*Migortho*: A Design Automation Flow for QCA Circuits” presents an automatized synthesis flow for quantum-dot cellular automata (QCA) designs and, thus, provides an important step toward the applicability of this emerging technology.
- “Accuracy-Configurable 2-D Gaussian Filter Architecture for Energy-Efficient Image Processing” integrates the concepts of configurable architectures and approximate computing in the context of 2-D Gaussian filter to provide a solution that enables trading of energy consumption and accuracy.
- “Power-Quality Configurable Hardware Design for AV1 Directional Intraframe Prediction” introduces a configurable intraframe prediction architecture for the video coding format AV1 that trades off power and quality.

WE HOPE YOU enjoy these contributions as much as we did. ■

Fernando Gehm Moraes is with the Pontifícia Universidade Católica do Rio Grande do Sul (PUCRS), Porto Alegre, Brazil. His primary research interests include microelectronics, reconfigurable architectures, NoCs and MPSoCs (multiprocessor SoC), and security. Moraes has an MSc from the Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, and a PhD from the Laboratoire d'Informatique, Robotique et Microélectronique de Montpellier (LIRMM), Montpellier, France. He is a Senior Member of IEEE.

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