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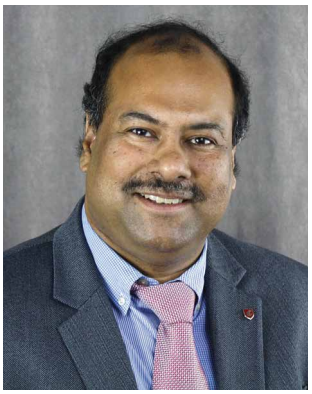

Special Issue on NOCS 2022

The articles in this issue are divided into three groups: 1) the first group consists of the papers from the 16th IEEE/ACM International Symposium on Networks-on-Chip (NOCS 2022); 2) the second group comprises selected articles from the 34th Symposium on Integrated Circuits and Systems Design (SBCCI 2021); and 3) the third group presents general interest articles.

The highlight of this issue is the journal-first model adopted for the articles accepted in the 16th edition of NOCS, which was held as a hybrid event. The on-site component was in Shanghai (China) and Phoenix (USA), on 13–14 October 2022, held in conjunction with the Embedded Systems Week (ESWEEK) 2022. NOCS is the premier event dedicated to interdisciplinary research on on-chip, package-scale, chip-to-chip, and datacenter rack-scale communication technology as well as architectures, design methods, applications, and systems. NOCS brings together scientists and engineers working on NoC innovations and applications from interdisciplinary research communities and areas, including discrete optimization and algorithms, computer architecture, networking, circuits and systems, packaging, embedded systems, and design automation. We thank the TPC chairs of NOCS 2022, Mahdi Nikdast and Miquel Moreto, for the timely delivery of all the accepted NOCS articles to the *IEEE Design&Test* submission system for further processing. This special issue consists of ten research articles.

In this issue of *IEEE Design&Test*, we also present five research articles from SBCCI 2021. SBCCI is an international forum dedicated to integrated circuits and systems design, test, and electronic design automation (EDA), held annually in Brazil. The Special Issue on SBCCI 2021 presents the extended versions of the best articles presented at SBCCI 2021. We thank the guest editors, Cláudio Machado Diniz and Bruno Zatt, for making this special issue possible.

In addition, we have, in this issue, three general interest articles, titled as follows: 1) "Secure Interposer-Based Heterogeneous Integration"; 2) "Large Power Division Ratio Branch-Line Coupler With Differential Through and Differential to Single-Ended Coupling"; and 3) "On Backside Probing Techniques and Their Emerging Security Threats."

Many thanks to Scott Davidson for the Last Byte titled "Small is Good."

I hope you enjoy reading this issue of *IEEE Design&Test*. ■

Partha Pratim Pande
Editor-in-Chief
IEEE Design&Test

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